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**3W STEREO CLASS-D AUDIO AMPLIFIER AND CLASS AB HEADPHONE DRIVER WITH DC VOLUME CONTROL, NON-CLIP POWER LIMIT AND UVP**
**NEW PRODUCT**

## Description

The PAM8019 is a Stereo 3W Class D audio power amplifier for driving bridged-tied speakers and includes a Stereo Class AB amplifier for driving headphones. The advanced 64 step DC volume control minimizes external components allowing simple and accurate volume control over the gain range of +20dB (Volume=0V) to -60dB (Volume=5V).

Integrated non-clip power limit technology suppresses output automatically with programmable power limit, improving the sound quality and helping to protect the speakers. Programmable under voltage protection (UVP) can be used to shut down the PAM8019 at a pre-determined voltage level helping to eliminate speaker pop by shutting down before the power supply collapses.

The PAM8019 is available in the power efficient and space saving U-QFN4040-20.

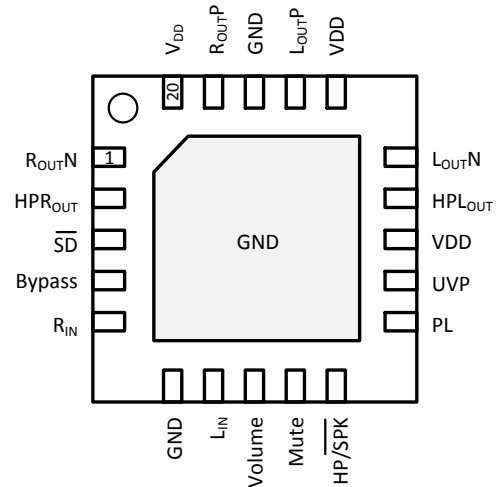
## Features

- 3W Stereo Class D Amplifier with Class AB Headphone Amplifier
- Filter Free and Low EMI Architecture
- Operating Voltage: 2.8V to 5.5V
- Low Quiescent Current of 7mA at a  $V_{DD}$  of 5V
- 64 Step DC Volume Control with Hysteresis from -60dB to +20dB
- Output Power
  - Class D Amplifier THD+N=1%  
 $V_{DD}=5V, Load =4\Omega; P_o=2.4W / Load =8\Omega; P_o=1.4W$
  - Class D Amplifier THD+N=10%  
 $V_{DD}=5V, Load =4\Omega; P_o=3.0W / Load =8\Omega; P_o=1.7W$
  - Class AB Headphone Amplifier  
 $V_{DD}=5V, Load=32\Omega; P_o=60mW$
- Speaker or Headphone Select
- Non Clip Power Limit (NCPL) Function
- OVP and Programmable UVP Protection
- Thermal and Over-Current Protection with Auto-Recovery
- Power Enhance Package U-QFN4040-20
- Lead Free and Green Devices Available (RoHS Compliant)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.  
 2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.  
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments

Top View

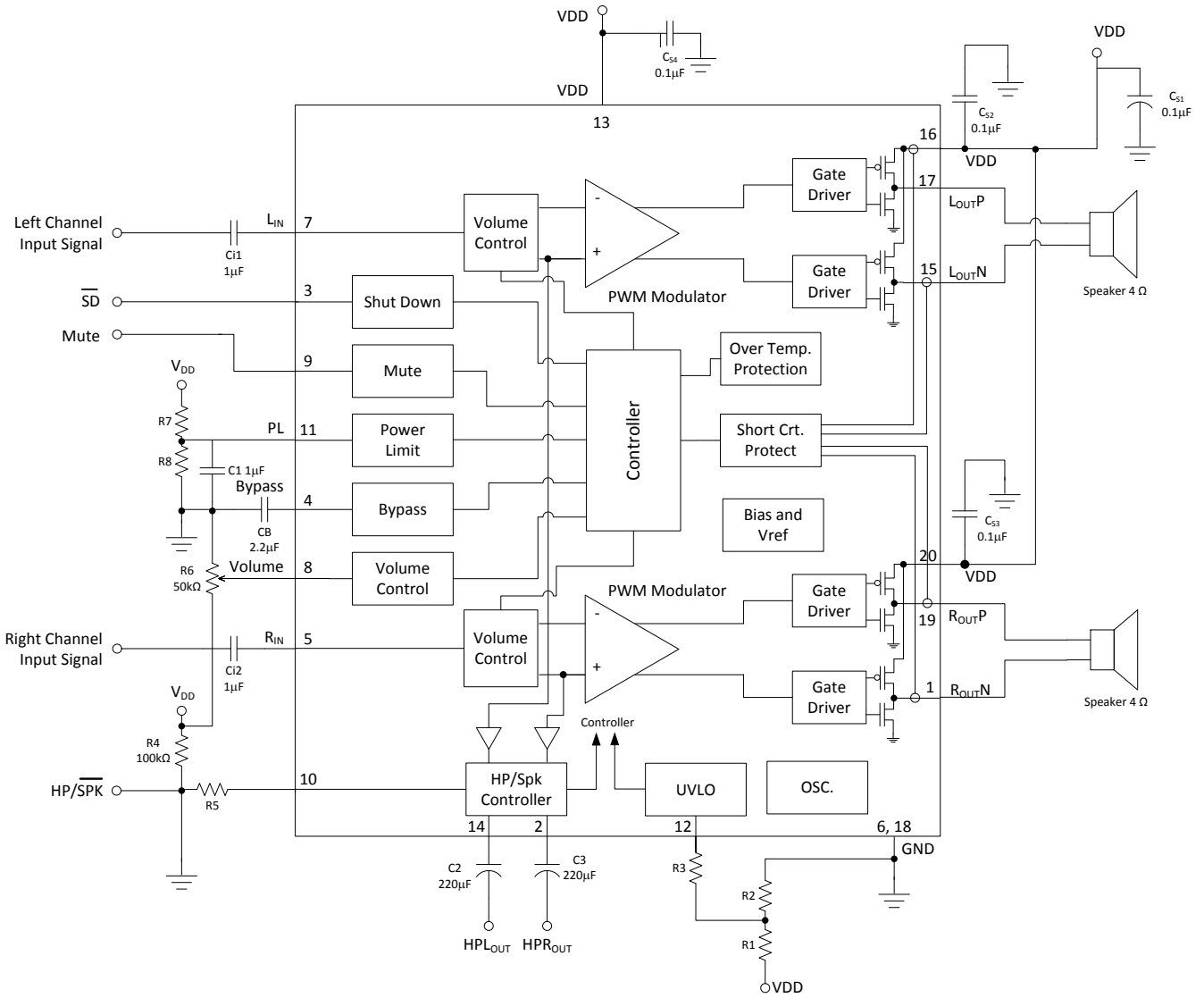


## Applications

- LCD Monitors and TVs
- Projectors / All-In-One Computers
- Portable / Active Speakers
- Portable DVD Players / Game Machines

**Typical Applications Circuit**

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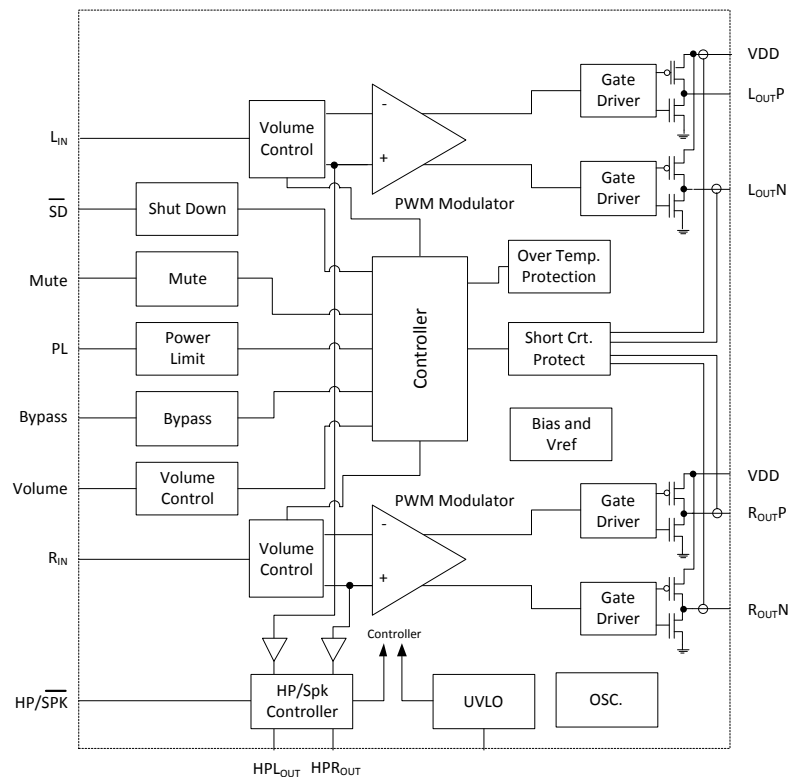


**Pin Descriptions**

Pin Number	Name	Function
3	$\overline{SD}$	Full Chip Shutdown Control Input (Active Low)
4	Bypass	Bias Voltage for Power Amplifier
5	R <sub>IN</sub>	Negative Input of Right Channel Power Amplifier
6, 18	GND	Ground Connection
7	L <sub>IN</sub>	Negative Input of Left Channel Power Amplifier
8	Volume	Internal Gain Setting Input Connect to VDD which Set Max. Gain = +20dB
9	Mute	Mute Control Signal Input (Active High)
10	HP/ $\overline{SPK}$	Output Mode Control Input High for Headphone Mode and Low for Speaker Mode
11	PL	Power limit reference voltage, see applications section for further details
12	UVP	Under Voltage Protection Input See applications section for further details
13,16,20	VDD	Supply Voltage
14	HPL <sub>OUT</sub>	Headphone - Left Channel Output
2	HPR <sub>OUT</sub>	Headphone - Right Channel Output
15	L <sub>OUTN</sub>	Power Amplifier - Left Channel Negative Output
17	L <sub>OUTP</sub>	Power Amplifier - Left Channel Positive Output
19	R <sub>OUTP</sub>	Power Amplifier - Right Channel Negative Output
1	R <sub>OUTN</sub>	Power Amplifier - Right Channel Positive Output
PAD	GND	Connect to ground (recommended) or No Connect.

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**Functional Block Diagram**



**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V <sub>DD</sub>	Supply Voltage V <sub>DD</sub>	-0.3 to 6.0	V
V <sub>IN</sub>	Input Voltage L <sub>IN</sub> , R <sub>IN</sub> , $\overline{SD}$ , Mute, HP/SPK	-0.3 to V <sub>DD</sub> + 0.3	
T <sub>J</sub>	Maximum Junction Temperature	+150	°C
T <sub>STG</sub>	Storage Temperature Range	- 65 to +150	
T <sub>SDR</sub>	Maximum Soldering Temperature Range, 5 Seconds	+300	

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

**Recommended Operating Conditions** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Max	Unit
V <sub>DD</sub>	Supply Voltage Range	2.8 to 5.5	V
V <sub>IH</sub>	High Level Threshold Voltage	$\overline{SD}$ , MUTE	2 to V <sub>DD</sub>
		HP/SPK	0.8 x V <sub>DD</sub> to V <sub>DD</sub>
V <sub>IL</sub>	Low Level Threshold Voltage	$\overline{SD}$ , MUTE	0 to 0.8
		HP/SPK	0 to 1.0
V <sub>ICM</sub>	Common Mode Input Voltage	1 to V <sub>DD</sub> - 1	V
T <sub>A</sub>	Ambient Operation Temperature Range	-40 to +85	°C
T <sub>J</sub>	Junction Temperature Range	-40 to +125	

**Thermal Information** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Typical Value	Unit
θ <sub>JA</sub>	Thermal Resistance – Junction to Ambient QFN4040-20	45	°C/W
θ <sub>JC</sub>	Ambient Operation Temperature Range QFN4040-20	7	°C/W

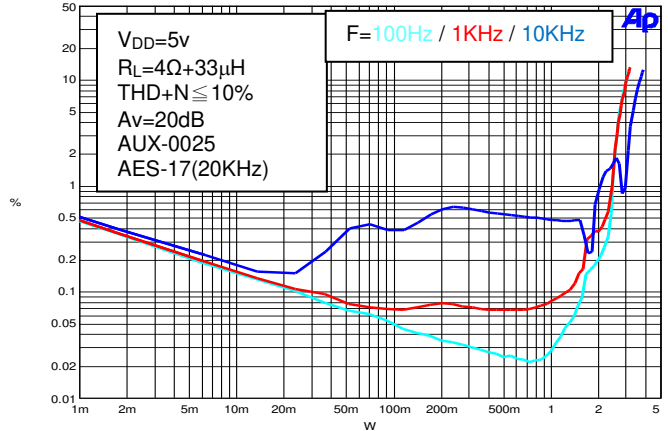
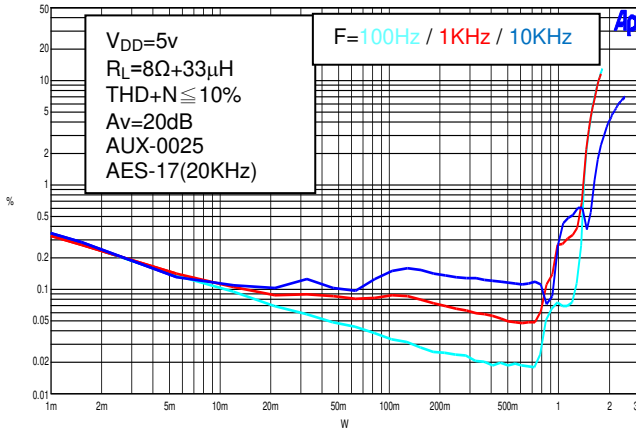
**Electrical Characteristics** (@T<sub>A</sub> = +25°C, V<sub>DD</sub> = 5V, Gain = Max., R<sub>L</sub>=8Ω, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage Range		2.8	-	5.5	V
<b>Speaker Mode</b>						
I <sub>Q</sub>	Quiescent Current (BTL)	V <sub>MUTE</sub> =0, V <sub>SD</sub> =5V, No Load	-	7	-	mA
I <sub>Q</sub>	Quiescent Current (SE)	V <sub>MUTE</sub> =0, V <sub>SD</sub> =5V, No Load	-	4	-	mA
I <sub>MUTE</sub>	Mute Current (BTL)	V <sub>MUTE</sub> =0, V <sub>SD</sub> =5V, No Load	-	3	-	mA
I <sub>MUTE</sub>	Mute Current (SE)	V <sub>MUTE</sub> =0, V <sub>SD</sub> =5V, No Load	-	4	-	mA
I <sub>SD</sub>	Shutdown Current	V <sub>MUTE</sub> =0, V <sub>SD</sub> =0V, No Load	-	-	1	μA
F <sub>OSC</sub>	Oscillator Frequency	-	200	250	300	KHz
R <sub>I</sub>	Input Resistance (BTL)	Gain=20dB	-	-	33	KΩ
R <sub>I</sub>	Input Resistance (SE)	Gain=3.5dB	-	-	56	KΩ
V <sub>OS</sub>	Output Offset Voltage	No load	-	10	-	mV
R <sub>DS(ON)</sub>	Drain – Source On-State Resistance	V <sub>DD</sub> =5.5V, I <sub>DS</sub> =0.8A P MOSFET	-	0.26	-	Ω
		V <sub>DD</sub> =5.5V, I <sub>DS</sub> =0.8A N MOSFET	-	0.19	-	
		V <sub>DD</sub> =4.5V, I <sub>DS</sub> =0.6A P MOSFET	-	0.28	-	
		V <sub>DD</sub> =4.5V, I <sub>DS</sub> =0.6A N MOSFET	-	0.21	-	
		V <sub>DD</sub> =3.6V, I <sub>DS</sub> =0.4A P MOSFET	-	0.29	-	
		V <sub>DD</sub> =3.6V, I <sub>DS</sub> =0.4A N MOSFET	-	0.21	-	
T <sub>START UP</sub>	Startup Time from Shutdown	Bypass Capacitor, C <sub>B</sub> =2.2μF	-	1.72	-	S
P <sub>O</sub>	Output Power	THD+N=10%, f=1KHz, R <sub>I</sub> =8Ω	1.5	1.7	-	W
		THD+N=10%, f=1KHz, R <sub>I</sub> =4Ω	2.8	3.0	-	
THD+N	Total Harmonic Distortion Plus Noise	R <sub>I</sub> =8Ω, P <sub>O</sub> =0.8W, f=1KHz	-	0.08	-	%
		R <sub>I</sub> =4Ω, P <sub>O</sub> =1.6W, f=1KHz	-	0.08	-	
PSRR	Power Supply Ripple Rejection	Input AC-GND, f=1KHz, V <sub>PP</sub> =200mV	-	- 61	-	dB
CS	Channel Separation	V <sub>DD</sub> =1W, f=1KHz	-	-82	-	dB
η	Efficiency	P <sub>O</sub> =1.7W, f=1KHz, R <sub>I</sub> =8Ω	85	90	-	%
		P <sub>O</sub> =3W, f=1KHz, R <sub>I</sub> =4Ω	80	88	-	
V <sub>N</sub>	Noise	Input AC-GND, A-weighting	-	180	-	μV
		Non A-weighting	-	270	-	
SNR	Signal Noise Ratio	F=20 ~ 20KHz, THD=1%	-	83	-	dB
<b>Head Phone Mode</b>						
V <sub>OS</sub>	Output Offset Voltage	No load	-	2.5	-	V
P <sub>O</sub>	Output Power	THD+N=1%, R <sub>I</sub> =32Ω, f=1KHz	-	60	-	mW
THD+N	Total Harmonic Distortion Plus Noise	R <sub>I</sub> =32Ω, P <sub>O</sub> =50mW, f=1KHz	-	0.02	-	%
PSRR	Power Supply Ripple Rejection	Input AC-GND, F=1KHz, V <sub>PP</sub> =200mV	-	75	-	dB
CS	Channel Separation	P <sub>O</sub> =1W, f=1KHz	-	-87	-	dB
V <sub>N</sub>	Noise	Input AC-GND, A-weighting	-	74	-	μV
		Non A-weighting	-	58	-	
SNR	Signal Noise Ratio	F=20 ~ 20KHz, THD=1%	-	89	-	dB
<b>Control Section</b>						
V <sub>IH</sub>	SD Input High	-	1.4	-	-	V
V <sub>IL</sub>	SD Input Low	-	-	-	0.6	V
V <sub>MH</sub>	Mute Input High	-	1.4	-	-	V
V <sub>ML</sub>	Mute Input Low	-	-	-	0.6	V
OTP	Over Temperature Protection	-	-	+150	-	°C
OTH	Over Temperature Hysteresis	-	-	+108	-	°C

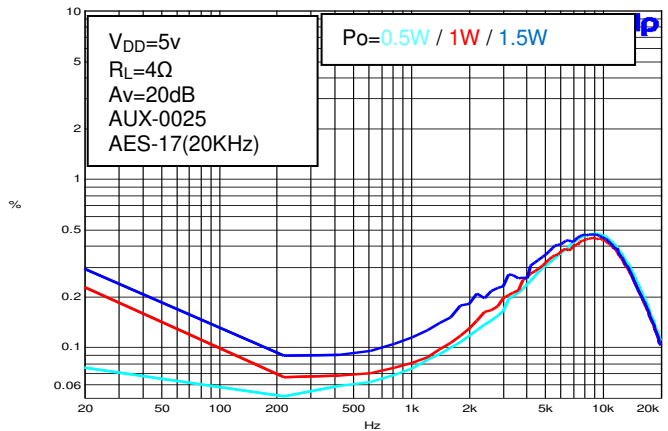
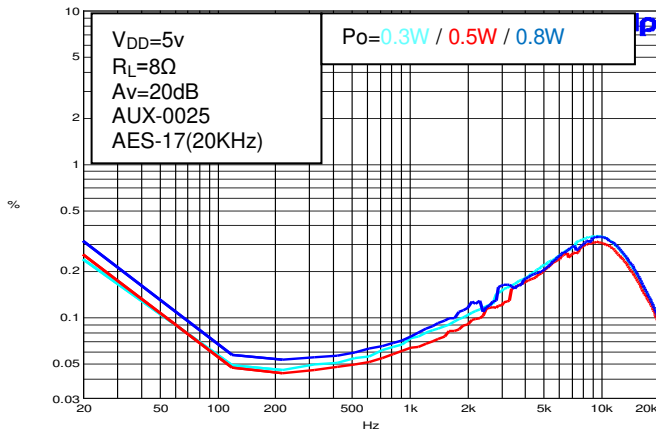
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**Typical Performance Characteristics**

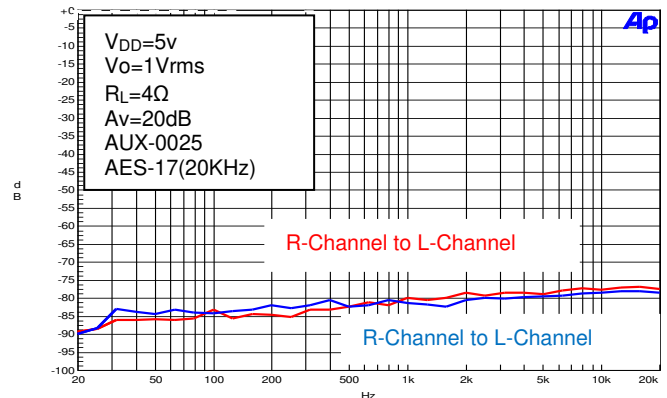
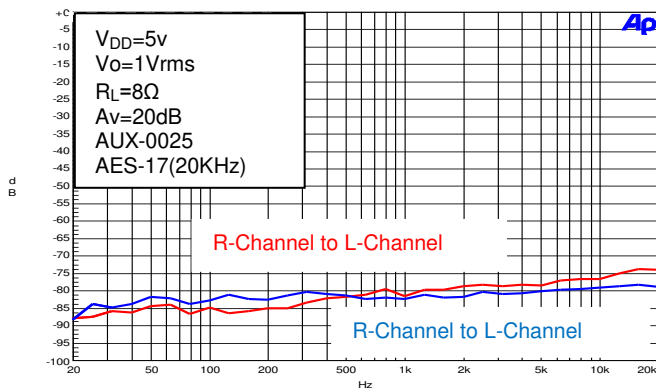
**THD+N vs. Output Power - Speaker**



**THD+N vs. Frequency - Speaker**



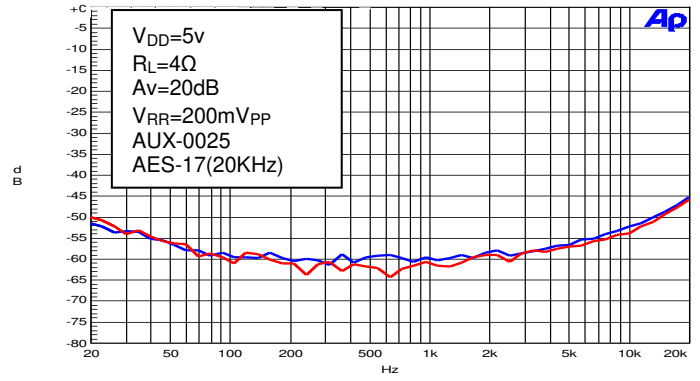
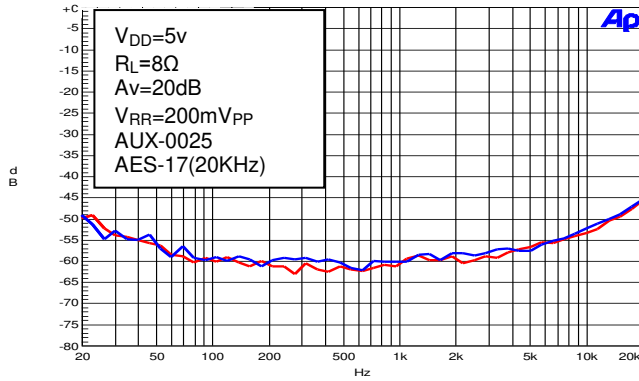
**Crosstalk vs. Frequency - Speaker**



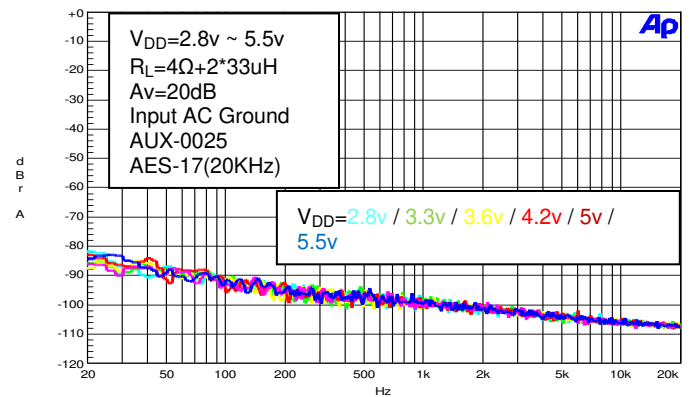
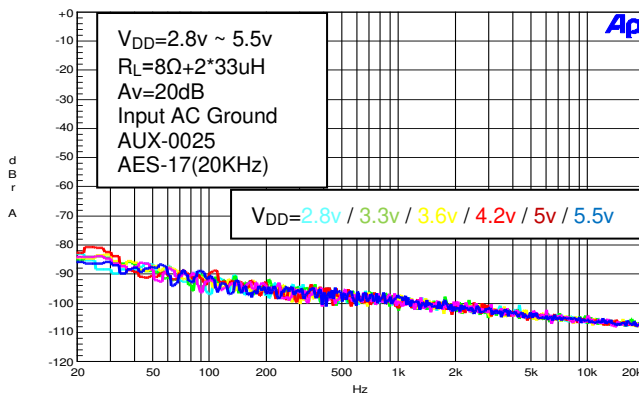
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Typical Performance Characteristics (Cont.)

PSRR vs. Frequency



Output Noise vs. Frequency – Speaker



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**Typical Performance Characteristics** (Cont.)

Table 1 DC Volume Control

Step	DC Volume (V)	Power Amp Gain (dB)	Head Phone Amp Gain (dB)	Step	DC Volume (V)	Power Amp Gain (dB)	Head Phone Amp Gain (dB)
1	0.000 to 0.201	20	3.51	33	2.462 to 2.533	6.7	-7.11
2	0.202 to 0.275	19.6	3.22	34	2.534 to 2.605	6.4	-7.43
3	0.276 to 0.347	19.2	2.94	35	2.606 to 2.678	6	-7.76
4	0.348 to 0.419	18.8	2.66	36	2.679 to 2.751	5.7	-8.09
5	0.420 to 0.491	18.4	2.39	37	2.752 to 2.823	5.3	-8.42
6	0.492 to 0.563	18	2.12	38	2.824 to 2.897	4.9	-8.76
7	0.564 to 0.633	17.6	1.85	39	2.898 to 2.969	4.6	-9.09
8	0.634 to 0.701	17.1	1.46	40	2.970 to 3.043	4.2	-9.43
9	0.702 to 0.771	16.6	1.07	41	3.044 to 3.114	3.8	-9.77
10	0.772 to 0.849	16.1	0.69	42	3.115 to 3.186	3.5	-10.1
11	0.850 to 0.929	15.6	0.32	43	3.187 to 3.259	3.1	-10.46
12	0.930 to 1.005	15.1	-0.05	44	3.260 to 3.332	2.7	-10.81
13	1.006 to 1.079	14.6	-0.41	45	3.333 to 3.403	2.3	-11.16
14	1.080 to 1.153	14.2	-0.77	46	3.404 to 3.476	2	-11.52
15	1.154 to 1.225	13.7	-1.12	47	3.477 to 3.551	1.6	-11.88
16	1.226 to 1.297	13.3	-1.47	48	3.552 to 3.621	1.2	-12.24
17	1.298 to 1.371	12.9	-1.82	49	3.622 to 3.695	0.8	-12.62
18	1.372 to 1.443	12.5	-2.16	50	3.696 to 3.767	0.4	-12.99
19	1.444 to 1.517	12	-2.5	51	3.768 to 3.839	0	-13.38
20	1.518 to 1.589	11.6	-2.84	52	3.840 to 3.909	-1	-14.37
21	1.590 to 1.661	11.2	-3.18	53	3.910 to 3.979	-2.1	-15.42
22	1.662 to 1.733	10.8	-3.51	54	3.980 to 4.045	-3	-16.3
23	1.734 to 1.807	10.5	-3.84	55	4.046 to 4.116	-5	-18.23
24	1.808 to 1.879	10.1	-4.17	56	4.117 to 4.195	-7	-20.16
25	1.880 to 1.951	9.7	-4.5	57	4.196 to 4.273	-9	-22.08
26	1.952 to 2.025	9.3	-4.82	58	4.274 to 4.347	-10.9	-23.96
27	2.026 to 2.097	8.9	-5.16	59	4.348 to 4.421	-17	-30.01
28	2.098 to 2.169	8.6	-5.48	60	4.422 to 4.493	-22.8	-35.83
29	2.170 to 2.243	8.2	-5.8	61	4.494 to 4.565	-29	-41.98
30	2.244 to 2.315	7.8	-6.13	62	4.566 to 4.637	-33.5	-46.46
31	2.316 to 2.389	7.5	-6.45	63	4.638 to 4.708	-39.5	-52.58
32	2.390 to 2.461	7.1	-6.78	64	4.709 to 5.000	-60	-92.95

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## Application Information

### Non Clip Power Limit (NCPL) Function

When output reaches the maximum power setting value, the NCLP circuits will decrease the gain to prevent the output waveform from clipping helping to prevent speaker damage and maximizing audio performance. The PL pin is used to set and control the NCPL function.

Table 1: NCPL Setting Threshold vs. Output

AGC Function	Output Power
$V_{DD}$ to $V_{DD} \times 0.45$ or PL pin floating	NCPL function disabled
$V_{DD} \times 0.45$ to $V_{DD} \times 0.27$	$P_O = \frac{[8(1/2 V_{DD} - V_{PL})^2]}{R_I} \times 0.95$
$V_{DD} \times 0.27$ to GND	$P_O = 2.3W$ (Max. output power $4\Omega$ ) $P_O = 1.2W$ (Max. output power $8\Omega$ )

### Mute Operation

The MUTE pin is an input for controlling the Class-D output state of the PAM8019. A logic low on this pin enables the outputs and logic high on this pin disables the outputs. This pin may be used to quickly disable or enable the outputs without a volume fade. Quiescent current is listed in the electrical characteristic table. The MUTE pin can be left floating due to the internal pull-down.

### Shutdown Operation

In order to reduce power consumption while not in use, the PAM8019 contains shutdown circuit to turn off the amplifier's bias circuit. The amplifier is turned off when logic low is placed on the  $\overline{SD}$  pin. The  $\overline{SD}$  pin can be left floating due to the internal pull-up.

### Under voltage Protection

External under voltage detection can be used to shut down the PAM8019 before an input device can generate a pop. The shutdown threshold at the UVP pin is 1.2V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application.

The threshold can be determined as below:

With the condition:  $R_3 \gg R_1/R_2$

$$V_{UVP} = [1.2 - (6\mu A \times R_3)] \times (R_1 + R_2) / R_2$$

$$\text{Hysteresis} = 5\mu A \times R_3 \times (R_1 + R_2) / R_2$$

### Power Supply Decoupling

The PAM8019 is a high performance CMOS audio-amplifier that requires adequate power supply decoupling to ensure the THD and PSRR are as low as possible. Power supply decoupling also prevents oscillation caused by long leads between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. A good Low-Equivalent-Series-Resistance (ESR) ceramic-capacitor of typically  $0.1\mu F$  is recommended to be placed as close as possible to the  $V_{DD}$  pin to filter the higher frequency transients, spikes or digital hash on the line. Filtering lower-frequency noise signals a large capacitor of  $10\mu F$  or greater should be placed near the audio amplifier.

## Application Information (Cont.)

### Input Capacitor (CI)

It is desirable to use a large input capacitor but in applications where the speaker lacks the ability to reproduce signals below 100Hz to 150Hz it may be possible to minimize CI without effecting system performance. Input Capacitor (CI) and Input Resistance (RI) of the amplifier form a high-pass filter with the corner frequency determined equation below:

$$F_c = 1 / 2\pi R_I \times C_I$$

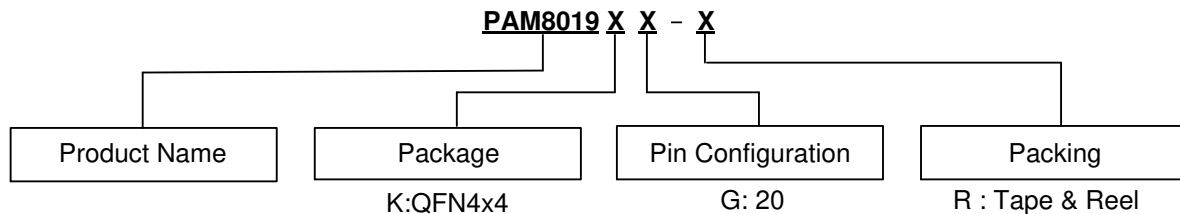
In addition to system cost and size, click and pop performance is affected by the size of the coupling capacitors. A larger in/out coupling capacitor requires more charge to reach its quiescent DC voltage (Normally 1/2 V<sub>DD</sub>). This charge comes from the internal circuit via the feedback and is more likely to create pops upon device enable. Minimizing the capacitor size based on necessary low frequency response can minimize the turn on pop.

### Bypass Capacitor (C<sub>BYP</sub>)

Bypass Capacitor (C<sub>BYP</sub>) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C<sub>BYP</sub> determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output signal. The noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N.

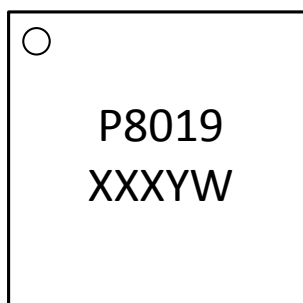
A ceramic bypass capacitor (C<sub>BYP</sub>) of 0.47µF to 1.0µF is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and when entering and leaving shutdown.

## Ordering Information



Part Number	Package	Standard Package
PAM8019KGR	U-QFN4040-20	3000 / Tape and Reel

## Marking Information

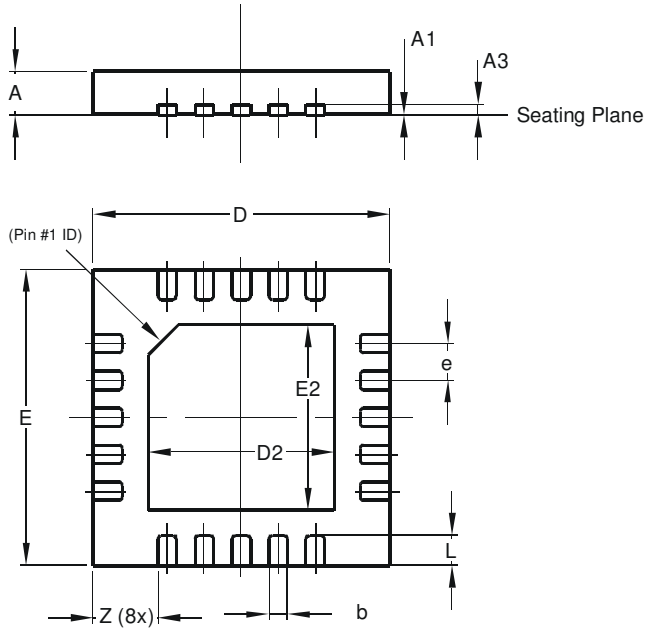


Y: Year  
W: Week  
X: Internal Code

**Package Outline Dimensions** (All dimensions in mm.)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**U-QFN4040-20**



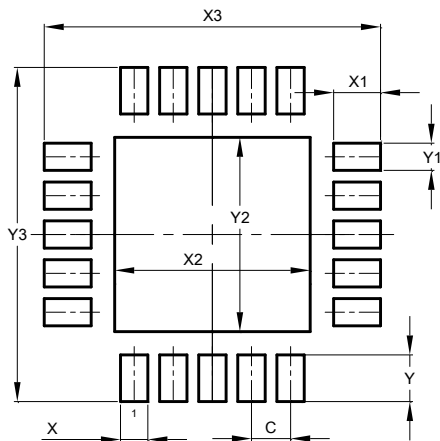
U-QFN4040-20			
Dim	Min	Max	Typ
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.40	2.60	2.50
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
L	0.35	0.45	0.40
Z	-	-	0.875
All Dimensions in mm			

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**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**U-QFN4040-20**



Dimensions	Value (in mm)
C	0.500
X	0.350
X1	0.600
X2	2.500
X3	4.300
Y	0.600
Y1	0.350
Y2	2.500
Y3	4.300

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