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Data Sheet, Rev. 2.0, Apr. 2005

FlexiSLIC™

Subscriber Line Interface Circuit

PBL 38620/2, Version 2

Wireline Communications

Never stop thinking.

Edition 2005-04-13

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Revision History: **2005-04-13** Rev. 2.0

Previous Version: **DS1**

Page	Subjects (major changes since last revision)
all	Package P-DSO-24-1 changed to P-/PG-DSO-24-8
all	Package type abbreviation SOIC changed to PDSO
all	Package P-LCC-28-2 changed to P-/PG-LCC-28-3
all	Package P-SSOP-24-1 changed to P-/PG-SSOP-24-1
Page 11	**Table 1**: Pin name DS changed to DR
Page 17	**Table 5**: Thermal resistance for 24-pin PDSO changed from 80.2 °C/W to 50.3 °C/W
Page 26	**Figure 8**: SLIC/codec circuitry changed
Page 27	**Table 6**: values of R_R, R_T, R_{RX}, R_{TX}, R_B changed, R_{FB} removed.
Page 32	**Figure 10** changed

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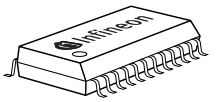
Version 2

1 Overview

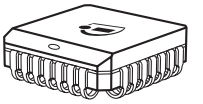
1.1 Features

- 24-pin SSOP package
- High and low battery with automatic switching
- 60 mW on-hook power dissipation in active state
- On-hook transmission
- Long loop battery feed tracks Vbat for maximum line voltage
- Selectable transmit gain (1x or 0.5x)
- No power-up sequence
- 44 V open loop voltage @ -48 V battery feed
- Close tolerance current feeding
- Full longitudinal current capability during on-hook state
- Analog overtemperature protection permits transmission while the protection circuits is active
- Integrated Ring Relay driver
- Ground key detector
- Programmable signal headroom

P-/PG-SSOP-24-1



P-/PG-DSO-24-8



P-/PG-LCC-28-3

1.2 Typical Applications

- Basic functionality Central Office Line card
- Private branch exchange (PABX)
- Digital added mainline (DAML)
- Terminal adapters (CPE)
- ISDN terminal adapters
- Other shortloop applications

Type	Package
PBL 38620/2 SH	P-/PG-SSOP-24-1
PBL 38620/2 SO	P-/PG-DSO-24-8
PBL 38620/2 QN	P-/PG-LCC-28-3

1.3 Description

The PBL 38620/2 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in PBX, Terminal adapters and other telecommunications equipment. The PBL 38620/2 SLIC has been optimized for low total line interface cost and for a high degree of flexibility in different applications.

The PBL 38620/2 SLIC has constant current feed, programmable to maximum 30 mA. A second lower battery voltage may be connected to the device to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external components or external control.

The SLIC incorporates loop current, ground key and ring-trip detection functions. The PBL 38620/2 is compatible with loop start signalling.

Two- to four-wire and four- to two-wire voice frequency (VF) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter, for example SiCoFi PEB 2466. The programmable two-wire impedance, complex or real, is set by a simple external network.

Longitudinal voltages are suppressed by a feedback loop in the SLIC and the longitudinal balance specifications meet Bellcore TR909 requirements.

The PBL 38620/2 SLIC package options are 24-pin SSOP, 24-pin PDSO or 28-pin PLCC.

1.4 Block Diagram

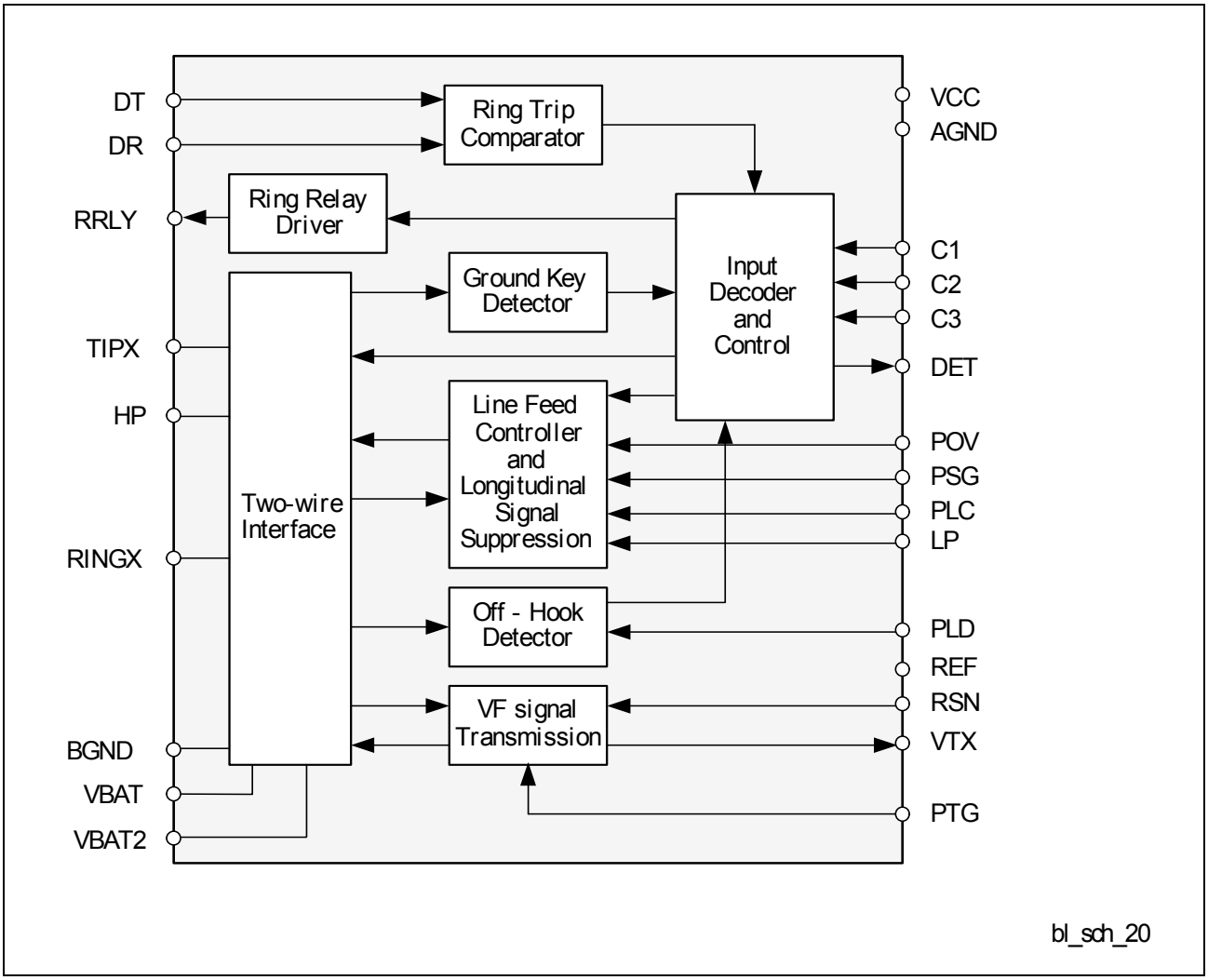


Figure 1 Block Diagram

2 Pin Configuration

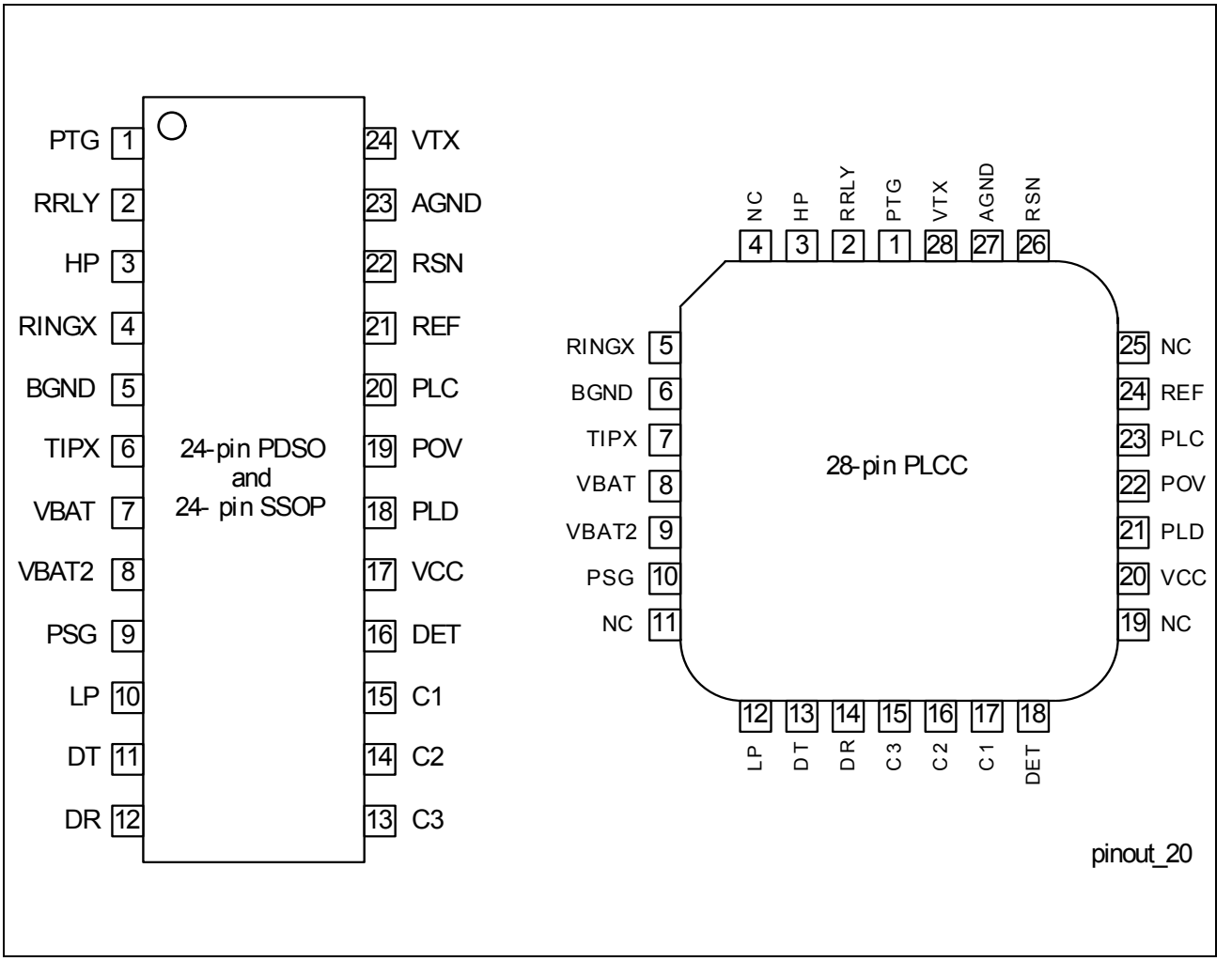


Figure 2 Pin Configuration, 24L-PDSO, 24L-SSOP and 28L-PLCC (top view).

Table 1 Pin Definition and Functions

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
1	1	PTG	–	Programmable transmit gain. Left open transmit gain = 0.0 dB, connected to AGND transmit gain = -6.02 dB.
2	2	RRLY	O	Ring relay driver output. The relay coil may be connected to maximum +14 V.
3	3	HP	–	Connection for high pass filter capacitor, C_{HP}. Other end of C_{HP} connects to TIPX.

Table 1 Pin Definition and Functions (cont'd)

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
4	5	RINGX	–	The RINGX pin connects to the ring lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
5	6	BGND	–	Battery ground, should be tied together with AGND.
6	7	TIPX	–	The TIPX pin connects to the tip lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
7	8	VBAT	–	Battery supply voltage. Negative with respect to GND.
8	9	VBAT2	–	An optional second (2) Battery Voltage connects to this pin via an external diode.
9	10	PSG	–	Programmable saturation guard. The resistive part of the DC feed characteristics is not used for PBL 38620/2, R_{SG} = 0 Ω
10	12	LP	–	Connection for low pass filter capacitor, C_{LP}. Other end of C_{LP} connects to VBAT.
11	13	DT	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
12	14	DR	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
13	15	C3	I	C1, C2, C3 are digital inputs (positive logic, internal pull-up), which control the SLIC operating states. Refer to **Table 2** for details.
14	16	C2	I	
15	17	C1	I	

Table 1 Pin Definition and Functions (cont'd)

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
16	18	DET	O	Detector output. Active low when indicating loop or ring-trip detection, active high when indicating ground key detection.
17	20	VCC	–	+5 V power supply.
18	21	PLD	–	Programmable loop detector threshold. The loop detection threshold is programmed by a resistor connected from this pin to AGND.
19	22	POV	–	Programmable overhead voltage. If pin is left open: The overhead voltage is internally set to min 1.0 V in off- and on-hook. If a resistor is connected between this pin and AGND: The overhead voltage can be set to higher values.
20	23	PLC	–	Programmable line current, the constant current part of the DC feed characteristic is programmed by a resistor connected from this pin to AGND.
21	24	REF	–	A reference, 49.9 kΩ, resistor should be connected from this pin to AGND.
22	26	RSN	–	Receive summing node. 200 times the AC current flowing into this pin equals the metallic (transversal) AC current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive node. A resistor should be connected from this pin to AGND.
23	27	AGND	–	Analog ground, should be tied together with BGND.

Table 1 Pin Definition and Functions (cont'd)

PDSO, SSOP Pin No.	PLCC Pin No.	Name	I/O	Function
24	28	VTX	O	Transmit vf output. The AC voltage difference between TIPX and RINGX, the AC metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one (or one half, see pin PTG). The two-wire impedance programming network connects between VTX and RSN.
-	4, 11, 19, 25	NC	–	Not Connected.

Table 2 SLIC Operating States

State	C3	C2	C1	SLIC Operating State	Active Detector (DET Response)
0	0	0	0	Open circuit	No active detector (DET is set high)
1	0	0	1	Ringing	Ring-trip detector (DET active low)
2	0	1	0	Active	Loop detector (DET active low)
3	0	1	1	Not applicable	–
4	1	0	0	Not applicable	–
5	1	0	1	Active	Ground key detector (DET active high)
6	1	1	0	Not applicable	–
7	1	1	1	Not applicable	–

3 Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature, Humidity						
Storage temperature range	T_{Stg}	-55	–	+150	°C	–
Operating temperature range	T_{Amb}	-40	–	+110	°C	–
Operating junction temperature range[1)]	T_J	-40	–	+140	°C	–
Power Supply (0 °C ≤ T_{Amb} ≤ +70 °C)						
V_{CC} with respect to A/BGND	V_{CC}	-0.4	–	6.5	V	–
V_{BAT2} with respect to A/BGND	V_{BAT2}	V_{BAT}	–	0.4	V	–
V_{BAT} with respect to A/BGND, continuous	V_{BAT}	-75	–	0.4	V	–
V_{BAT} with respect to A/BGND, 10 ms	V_{BAT}	-80	–	0.4	V	–
Power Dissipation						
Continuous power dissipation	P_D	–	–	1.5	W	T_{Amb} ≤ +70 °C
Ground						
Voltage between AGND and BGND	V_G	-0.3	–	0.3	V	–
Relay Driver						
Ring relay supply voltage	–	–	–	BGND +14	V	–
Ring Trip Comparator						
Input voltage	V_{DT}, V_{DR}	V_{BAT}	–	AGND	V	–
Input current	I_{DT}, I_{DR}	-5	–	5	mA	–
Digital Inputs, Outputs (C1, C2, C3, DET)						
Input voltage	V_{ID}	-0.4	–	V_{CC}	V	–
Output voltage	V_{OD}	-0.4	–	V_{CC}	V	–

Table 3 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
TIPX and RINGX Terminals (0 °C ≤ T_{Amb} ≤ +70 °C, V_{BAT} = -50 V)						
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-100	–	100	mA	–
TIPX or RINGX voltage, continuous (referenced to AGND)[2]	V_{TA}, V_{RA}	-80	–	2	V	–
TIPX or RINGX[2]	V_{TA}, V_{RA}	V_{BAT} - 10	–	5	V	Pulse < 10 ms, t_{Rep} > 10 s
TIPX or RINGX[2]	V_{TA}, V_{RA}	V_{BAT} - 25	–	10	V	Pulse < 1 µs, t_{Rep} > 10 s
TIP or RING[2)3)]	V_{TA}, V_{RA}	V_{BAT} - 35	–	15	V	Pulse < 250 ns, t_{Rep} > 10 s

1) The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.

2) With the diodes D_{VB} and D_{VB2} included, see **Figure 8**.

3) R_{F1} and R_{F2} > 20 Ω is also required. Pulse is supplied to RING and TIP outside R_{F1} and R_{F2}.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_{Amb}	0	–	+70	°C	–
V_{CC} with respect to AGND	V_{CC}	4.75	–	5.25	V	–
V_{BAT} with respect to AGND	V_{BAT}	-58	–	-8	V	–
AGND with respect to BGND	V_G	-100	–	100	mV	–

3.1 Characterictics

The specification is made with following setup: 0 °C ≤ T_{Amb} ≤ +70 °C, PTG = open (see pin description), V_{CC} = +5 V ± 5%, V_{BAT} = -58 V to -40 V, V_{BAT2} = -17 V, R_{LC} = 38.3 kΩ, I_L = 22 mA, R_L = 600 Ω, R_{F1} = R_{F2} = 0, R_{REF} = 49.9 kΩ, C_{HP} = 47 nF, C_{LP} = 0.15 µF, R_T = 120 kΩ, R_{SG} = 0 kΩ, R_{RX} = 60 kΩ, R_R = 52.3 kΩ, R_{OV} = infinite.
Current definition: current is positive if flowing into a pin unless stated otherwise.

Table 5 Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Two-Wire Port						
Overhead level[1], Active, 1% THD R_{OV} = infinite see **Figure 3**	V_{TRO}	1.0	–	–	V_{Peak}	–
		1.0	–	–	V_{Peak}	On-Hook, I_{LDC} ≤ 5 mA
Input impedance[2]	Z_{TRX}	–	Z_T/ 200	–	Ω	–
Longitudinal impedance	Z_{LOT}, Z_{LOR}	–	20	35	Ω/wire	0 < f < 100 Hz
Longitudinal current limit	I_{LOT}, I_{LOR}	10	–	–	mA_{rms}/ wire	Active
Longitudinal to metallic balance (IEEE standard 455-1984)	B_{LM}	53	–	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		53	–	–	dB	1.0 kHz < f < 3.4 kHz
Longitudinal to metallic balance $B_{LME} = 20 \times \log\lvert E_{LO}/V_{TR}\rvert$, see **Figure 4**	B_{LME}	53	75	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		53	70	–	dB	1.0 kHz < f < 3.4 kHz
Longitudinal to four-wire balance $B_{LFE} = 20 \times \log\lvert E_{LO}/V_{TX}\rvert$, see **Figure 4**	B_{LFE}	53	75	–	dB	0.2 kHz ≤ f ≤ 1.0 kHz
		53	70	–	dB	1.0 kHz < f < 3.4 kHz

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Metallic to longitudinal balance $B_{MLE} = 20 \times \log\lvert V_{TR}/V_{LO}\rvert$, E_{RX} = 0 V, see **Figure 5**	B_{MLE}	40	50	–	dB	0.2 kHz < f < 3.4 kHz
Four-wire to longitudinal balance $B_{FLE} = 20 \times \log\lvert E_{RX}/V_{LO}\rvert$, see **Figure 5**	B_{FLE}	40	50	–	dB	0.2 kHz < f < 3.4 kHz
Two-wire return loss[3] $r = 20 \times \log\frac{\lvert Z_{TRX} + Z_L\rvert}{\lvert Z_{TRX} - Z_L\rvert}$	r	30	35	–	dB	0.2 kHz < f <1.0 kHz
		20	22	–	dB	1.0 kHz < f < 3.4 kHz
TIPX idle voltage	V_{TI}	–	-1.1	–	V	Active, I_L = 0 mA
RINGX idle voltage	V_{RI}	–	V_{BAT}+ 2.5	–	V	Active, I_L = 0 mA
Open loop voltage	V_{TR}	–	V_{BAT}+ 3.6	–	V	Active, I_L = 0 mA
Four-Wire Transmit Port (VTX)						
Overhead level[4], Load imp. > 20 kΩ 1% THD see **Figure 6**	V_{TXO}	1.0	–	–	V_{Peak}	–
		1.0	–	–	V_{Peak}	On-Hook, $I_L \leq 5$ mA
Output offset voltage	ΔV_{TX}	-100	–	100	mV	–
Output impedance	Z_{TX}	–	15	50	Ω	0.2 kHz < f < 3.4 kHz
Four-Wire Receive Port (receive summing node = RSN)						
RSN DC voltage	V_{RSNdc}	1.15	1.25	1.35	V	I_{RSN} = -55 µA
RSN impedance		–	8	20	Ω	0.2 kHz < f < 3.4 kHz
RSN current (I_{RSN}) to metallic loop current (I_L) gain	α_{RSN}	–	200	–	ratio	0.3 kHz < f < 3.4 kHz

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Frequency Response						
Two-wire to four-wire, relative to 0 dBm, 1.0 kHz, E_{RX} = 0 V, see **Figure 7**	g_{2-4}	-0.20	–	0.10	dB	0.3 kHz < f < 3.4 kHz
		-1.0	–	0.1	dB	f = 8 kHz, 12 kHz, 16 kHz
Four-wire to two-wire, relative to 0 dBm, 1.0 kHz, E_L = 0 V, see **Figure 7**	g_{4-2}	-0.2	–	0.1	dB	0.3 kHz < f < 3.4 kHz
		-1.0	–	0	dB	f = 8 kHz, 12 kHz
		-2.0	–	0	dB	f = 16 kHz
Four-wire to four-wire, relative to 0 dBm, 1.0 kHz, E_L = 0 V, see **Figure 7**	g_{4-4}	-0.2	–	0.1	dB	0.3 kHz < f < 3.4 kHz
Insertion Loss						
Two-wire to four-wire[5], $G_{2-4} = 20 \times \log\lvert V_{TX}/V_{TR}\rvert$ 0 dBm, 1.0 kHz	G_{2-4}	-0.2	–	0.2	dB	E_{RX} = 0 V, PTG = Open see **Figure 7**
		-6.22	-6.02	-5.82	dB	PTG = AGND
Four-wire to two-wire[6], $G_{4-2} = 20 \times \log\lvert V_{TR}/E_{RX}\rvert$, E_L = 0 V, see **Figure 7**	G_{4-2}	-0.2	–	0.2	dB	0 dBm, 1.0 kHz

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gain Tracking						
Two-wire to four-wire[7], Ref. -10 dBm, 1.0 kHz, see **Figure 7**		-0.1	–	0.1	dB	-40 dBm to +0 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Four-wire to two-wire, Ref. -10 dBm, 1.0 kHz, see **Figure 7**		-0.1	–	0.1	dB	-40 dBm to +0 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Noise						
Idle channel noise at two-wire port[8] (TIPX-RINGX) or four-wire (VTX) output		–	–	12	dBrnC	C-message weighting
		–	–	-78	dBmp	Psophometrical weighting
Harmonic Distortion						
Two-wire to four-wire, see **Figure 7**		–	-67	-50	dB	0 dBm 0.3 kHz < f < 3.4 kHz
Four-wire to two-wire		–	-67	-50	dB	
Battery Feed Characteristics						
Constant loop current, R_{LC} in kΩ see **Figure 12**	I_{LProg}	0.92 × I_{LProg}	I_{LProg}	1.08 × I_{LProg}	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 4{,}0$
	I_{LProg} @ 30 mA	0.95 × I_{LProg}	I_{LProg}	1.05 × I_{LProg}	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 4{,}2$
	I_{LProg} @ 18 mA	0.94 × I_{LProg}	I_{LProg}	1.06 × I_{LProg}	mA	$I_{LProg} = \frac{1000}{R_{LC}} - 3{,}9$
Open circuit loop current	I_{LOC}	-100	0	100	µA	R_L = 0 Ω

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Loop Detector						
Programmable threshold, $I_{LTh} = 500/R_{LD}$	I_{LTh}	0.85 × I_{LTh}	I_{LTh}	1.15 × I_{LTh}	mA	R_{LD} in kW, 7 mA ≤ I_{LTh}
Ground Key Detector						
Ground key detector threshold		10	16	22	mA	I_{TIPX} and I_{RINGX} difference to trigger ground key detector.
Ring Trip Comparator						
Offset voltage	ΔV_{DTDR}	-20	0	20	mV	Source resistance, R_S = 0 Ω
Input bias current	I_B	-200	-20	200	nA	$I_B=(I_{DT}+I_{DR})/2$
Input common mode range	V_{DT}, V_{DR}	V_{BAT} +1	–	-1	V	–
Ring Relay Driver						
Saturation voltage	V_{OL}	–	0.2	0.5	V	I_{OL} = 50 mA
Off state leakage current	I_{LK}	–	–	10	µA	V_{OH} = 12 V
Digital Inputs (C1, C2, C3)						
Input low voltage	V_{IL}	0	–	0.5	V	–
Input high voltage	V_{IH}	2.5	–	V_{CC}	V	–
Input low current	I_{IL}	–	–	-50	µA	V_{IL} = 0.5 V
Input high current	I_{IH}	–	–	50	µA	V_{IH} = 2.5 V

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Detector Output (DET)						
Output low voltage	V_{OL}	–	–	0.7	V	I_{OL} = 0.5 mA
Internal pull-up resistor to V_{CC}		–	15	–	kΩ	–
Power Dissipation (V_{BAT} -48 V, V_{BAT2} = -17 V)						
Power Dissipation	P_1	–	10	15	mW	Open circuit (C1, C2, C3 = 0)
Power Dissipation	P_2	–	60	80	mW	Active (On-hook) Long current = 0 mA
Power Dissipation	P_3	–	290	–	mW	Active (Off-hook) R_L = 300 Ω
Power Dissipation	P_4	–	145	–	mW	Active (Off-hook) R_L = 500 Ω
Power Supply Currents (V_{BAT} = -48 V)						
V_{CC} current	I_{CC}	–	1.2	2.0	mA	Open circuit (C1, C2, C3 = 0)
V_{BAT} current	I_{BAT}	-0.1	-0.05	–	mA	Open circuit (C1, C2, C3 = 0)
V_{CC} current	I_{CC}	–	2.8	4.0	mA	Active, On-hook, Long current = 0 mA
V_{BAT} current	I_{BAT}	-1.5	-1.0	–	mA	Active, On-hook, Long current = 0 mA
Power Supply Rejection Ratios						
V_{CC} to 2- or 4-wire port		30	42	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{BAT2} to 2- or 4-wire port		40	60	–	dB	Active, f = 1 kHz, V_n = 100 mV
V_{BAT} to 2- or 4-wire port		36	45	–	dB	Active, f = 1 kHz, V_n = 100 mV

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature Guard						
Junction threshold temperature	T_{JG}	–	145	–	°C	–
Thermal Resistance						
24-pin SSOP	$\Theta_{JP24SSOP}$	–	55	–	°C/W	–
	$R_{th, jA}$	–	66.9	–	°C/W	P-/PG-SSOP-24-1, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
24-pin PDSO	$\Theta_{JP24PDSO}$	–	43	–	°C/W	–
	$R_{th, jA}$	–	50.3	–	°C/W	P-/PG-DSO-24-8, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
28-pin PLCC	$\Theta_{JP28PLCC}$	–	39	–	°C/W	–
	$R_{th, jA}$	–	50.4	–	°C/W	P-/PG-LCC-28-3, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber

1) The overhead level can be adjusted with the resistor R_{OV} for higher levels, for example min 3.1 V_{Peak}, and is specified at the two-wire port with the signal source at the four-wire receive port.

2) The two-wire impedance is programmable by selection of external component values according to:
$Z_{TRX} = Z_T/(|G_{2\text{-}4S} \times \alpha_{RSN}|)$ where:
Z_{TRX} = impedance between the TIPX and RINGX terminals
Z_T = programming network between the VTX and RSN terminals
$G_{2\text{-}4S}$ = transmit gain, nominally = 1 (or 0.5, see pin PTG)
α_{RSN} = receive current gain, nominally 200 (current defined as positive flowing into the receive summing node, RSN, and when flowing from ring to tip).

3) Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, for example by dividing R_T into two equal halves and connecting a capacitor from the common point to ground.

4) The overhead level can be adjusted with the resistor R_{OV} for higher levels, for example min 3.1 V_{Peak}, and is specified at the four-wire transmit port, (VTX) with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2\text{-}4S}$ = 1 (or 0.5, see pin PTG).

5) Pin PTG = Open sets transmit gain to nom. 0.0 dB.
Pin PTG = AGND sets transmit gain to nom. -6.02 dB
Secondary resistor R_F (see **Figure 8**) impacts the insertion loss as explained in **Chapter 5**. The specified insertion loss is valid for R_F = 0.

6) The specified insertion loss tolerance does not include errors caused by external components.

7) The level is specified at the two-wire port.

8) The two-wire idle noise is specified with the port terminated in 600 Ω (R_L), and with the four-wire receive port grounded (E_{RX} = 0; see **Figure 7**). The four-wire idle noise at V_{TX} is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is referenced to a 600 Ω programmed two-wire impedance level at V_{TX}. The four-wire receive port is grounded (E_{RX} = 0).

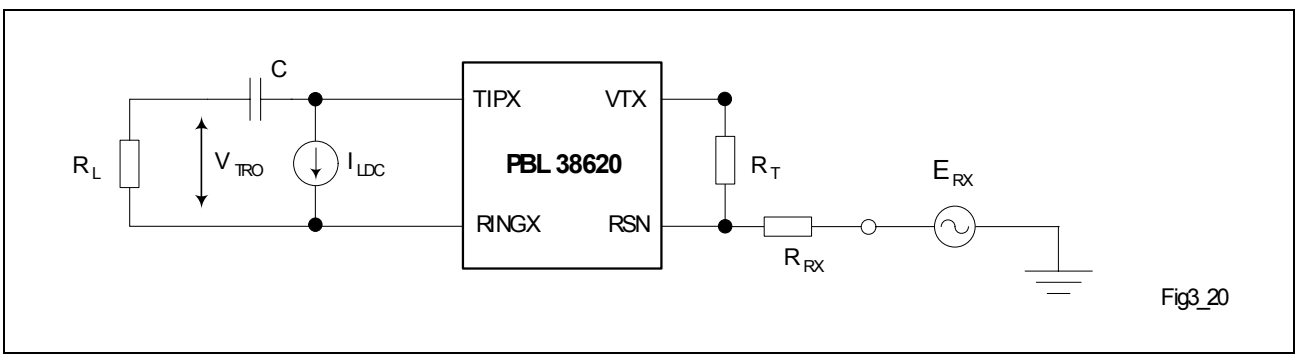


Figure 3 Overhead Level, V_{TRO}, Two-Wire Port

$1/\omega C$ << R_L, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

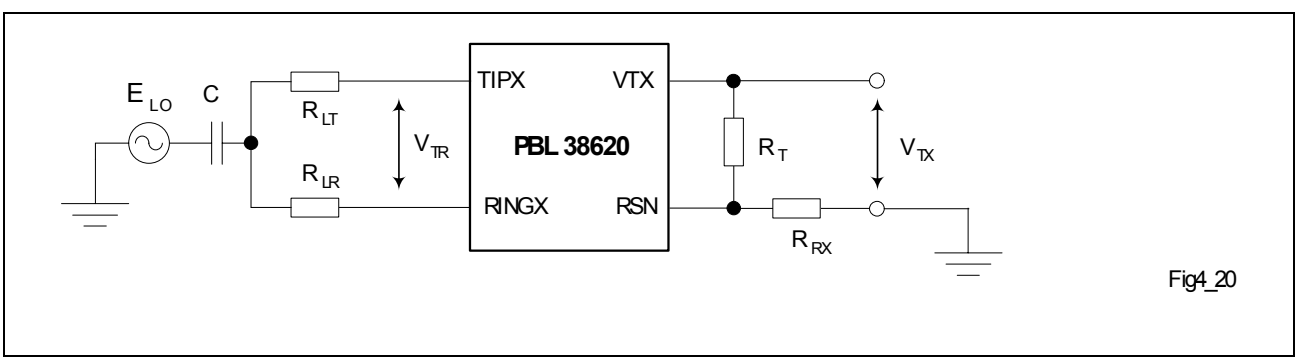


Figure 4 Longit. to Metallic, B_{LME} and Longit. to Four-Wire, B_{LFE} Balance

$1/\omega C$ << 150 Ω, R_{LT} = R_{LR} = R_L /2 = 300 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

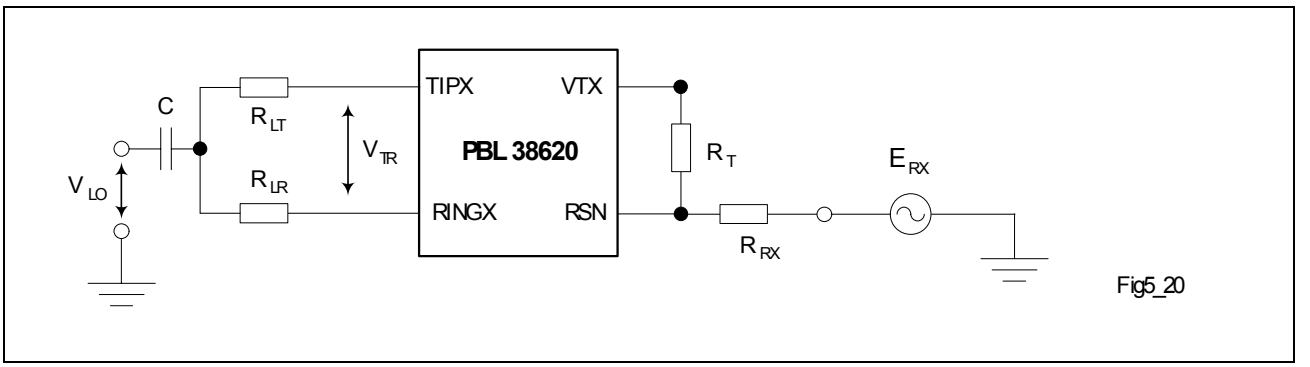


Figure 5 Metallic to Longit., B_{MLE} and Four-Wire to Longit. Balance, B_{FLE}

$1/\omega C$ << 150 Ω, $R_{LT} = R_{LR} = R_L$ /2 = 300 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

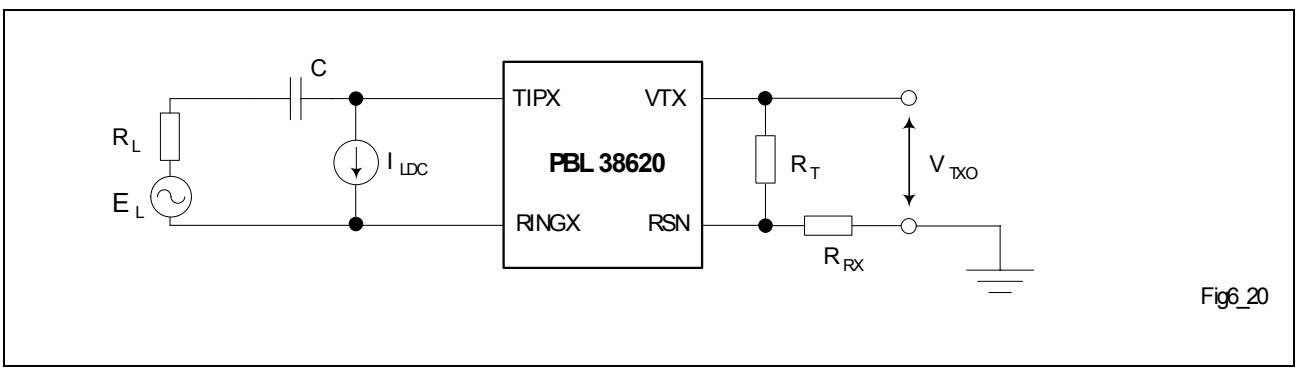


Figure 6 Overhead Level, V_{TXO}, Four-Wire Transmit Port

$1/\omega C$ << R_L, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ

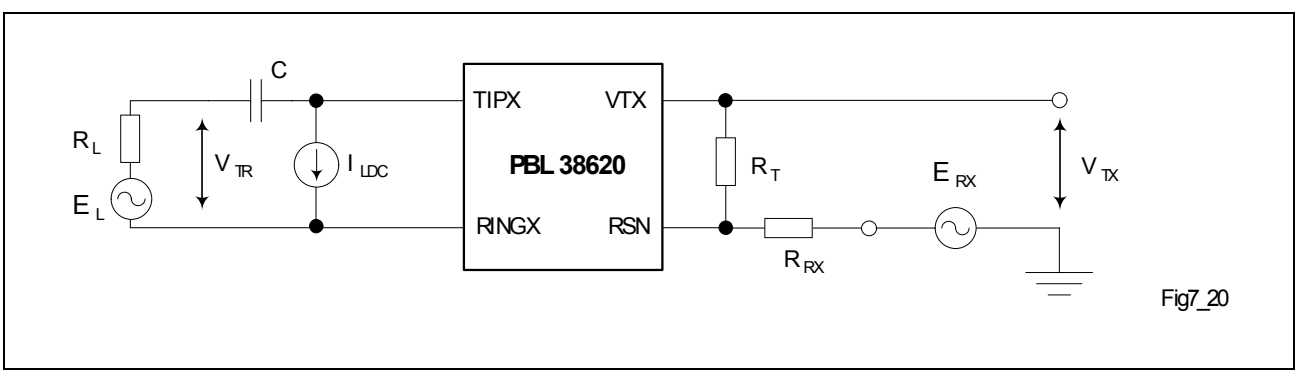


Figure 7 Frequency Response, Insertion Loss, Gain Tracking

$1/\omega C$ << R_L, R_L = 600 Ω, R_T = 120 kΩ, R_{RX} = 60 kΩ