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Kind regards,

Team Nexperia



PBSS5230PAP

30 V, 2 A PNP/PNP low V_{CEsat} (BISS) transistor

11 January 2013

Product data sheet

1. General description

PNP/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PBSS4230PANP. NPN/NPN complement: PBSS4230PAN.

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- High energy efficiency due to less heat generation
- AEC-Q101 qualified

3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

4. Quick reference data

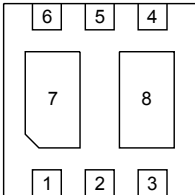
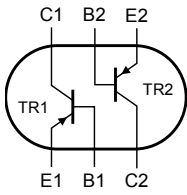
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---|---|-----|-----|-----|------------|
| Per transistor | | | | | | |
| V_{CEO} | collector-emitter voltage | open base | - | - | -30 | V |
| I_C | collector current | | - | - | -2 | A |
| I_{CM} | peak collector current | single pulse; $t_p \leq 1$ ms | - | - | -3 | A |
| Per transistor | | | | | | |
| R_{CEsat} | collector-emitter saturation resistance | $I_C = -1$ A; $I_B = -0.1$ A; pulsed; $t_p \leq 300$ μ s; $\delta \leq 0.02$; $T_{amb} = 25$ °C | - | - | 195 | m Ω |



5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|---------------|--|---|
| 1 | E1 | emitter TR1 |  <p>Transparent top view DFN2020-6 (SOT1118)</p> |  <p>sym138</p> |
| 2 | B1 | base TR1 | | |
| 3 | C2 | collector TR2 | | |
| 4 | E2 | emitter TR2 | | |
| 5 | B2 | base TR2 | | |
| 6 | C1 | collector TR1 | | |
| 7 | C1 | collector TR1 | | |
| 8 | C2 | collector TR2 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|-----------|--|---------|
| | Name | Description | Version |
| PBSS5230PAP | DFN2020-6 | plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm | SOT1118 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PBSS5230PAP | 2H |

8. Limiting values

Table 5. Limiting values

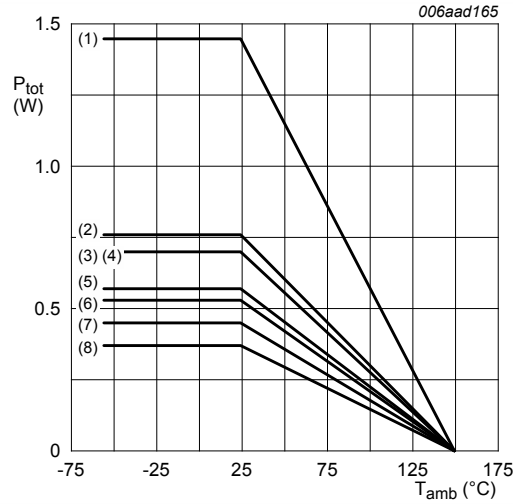
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------|---------------------------|-------------------------------------|-----|------|------|
| Per transistor | | | | | |
| V _{CBO} | collector-base voltage | open emitter | - | -30 | V |
| V _{CEO} | collector-emitter voltage | open base | - | -30 | V |
| V _{EBO} | emitter-base voltage | open collector | - | -7 | V |
| I _C | collector current | | - | -2 | A |
| I _{CM} | peak collector current | single pulse; t _p ≤ 1 ms | - | -3 | A |
| I _B | base current | | - | -0.3 | A |

30 V, 2 A PNP/PNP low VCEsat (BISS) transistor

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-------------------|-------------------------|-------------------------------|-----|-----|------|------|
| I_{BM} | peak base current | single pulse; $t_p \leq 1$ ms | | - | -1 | A |
| P_{tot} | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 370 | mW |
| | | | [2] | - | 570 | mW |
| | | | [3] | - | 530 | mW |
| | | | [4] | - | 700 | mW |
| | | | [5] | - | 450 | mW |
| | | | [6] | - | 760 | mW |
| | | | [7] | - | 700 | mW |
| | | | [8] | - | 1450 | mW |
| Per device | | | | | | |
| P_{tot} | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 510 | mW |
| | | | [2] | - | 780 | mW |
| | | | [3] | - | 730 | mW |
| | | | [4] | - | 960 | mW |
| | | | [5] | - | 620 | mW |
| | | | [6] | - | 1040 | mW |
| | | | [7] | - | 960 | mW |
| | | | [8] | - | 2000 | mW |
| T_j | junction temperature | | | - | 150 | °C |
| T_{amb} | ambient temperature | | | -55 | 150 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |

- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².



- (1) 4-layer PCB 70 μm, mounting pad for collector 1 cm²
- (2) FR4 PCB 70 μm, mounting pad for collector 1 cm²
- (3) 4-layer PCB 70 μm, standard footprint
- (4) 4-layer PCB 35 μm, mounting pad for collector 1 cm²
- (5) FR4 PCB 35 μm, mounting pad for collector 1 cm²
- (6) 4-layer PCB 35 μm, standard footprint
- (7) FR4 PCB 70 μm, standard footprint
- (8) FR4 PCB 35 μm, standard footprint

Fig. 1. Per transistor: power derating curves

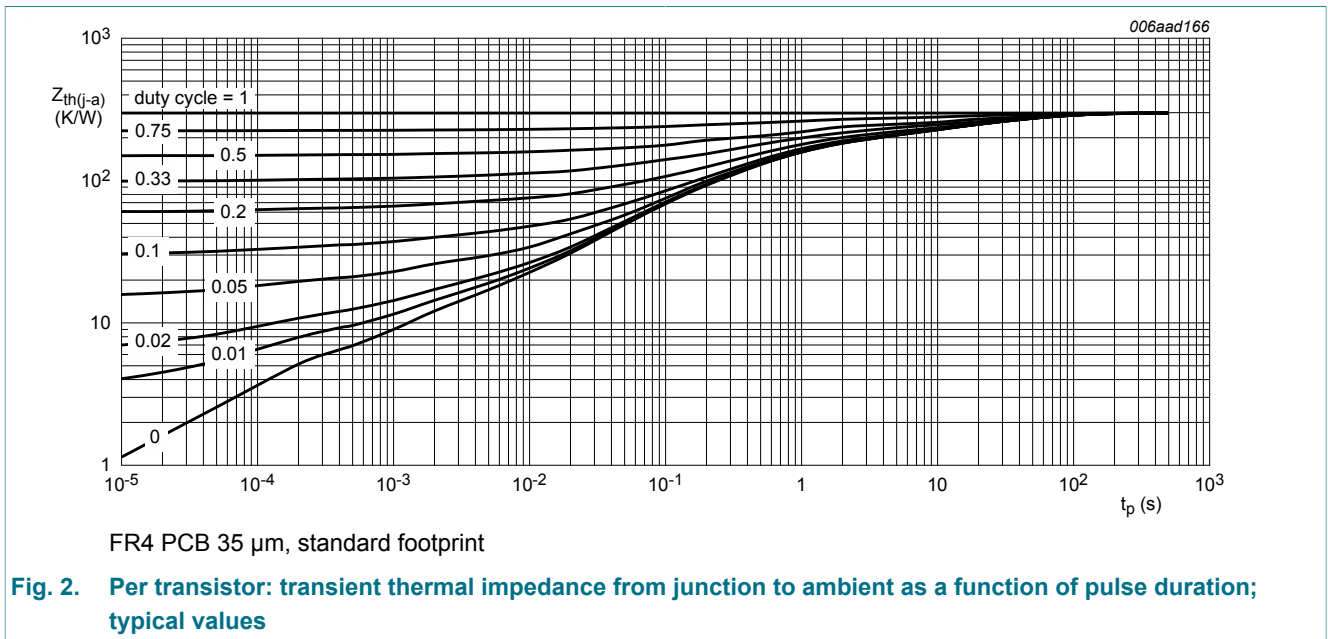
9. Thermal characteristics

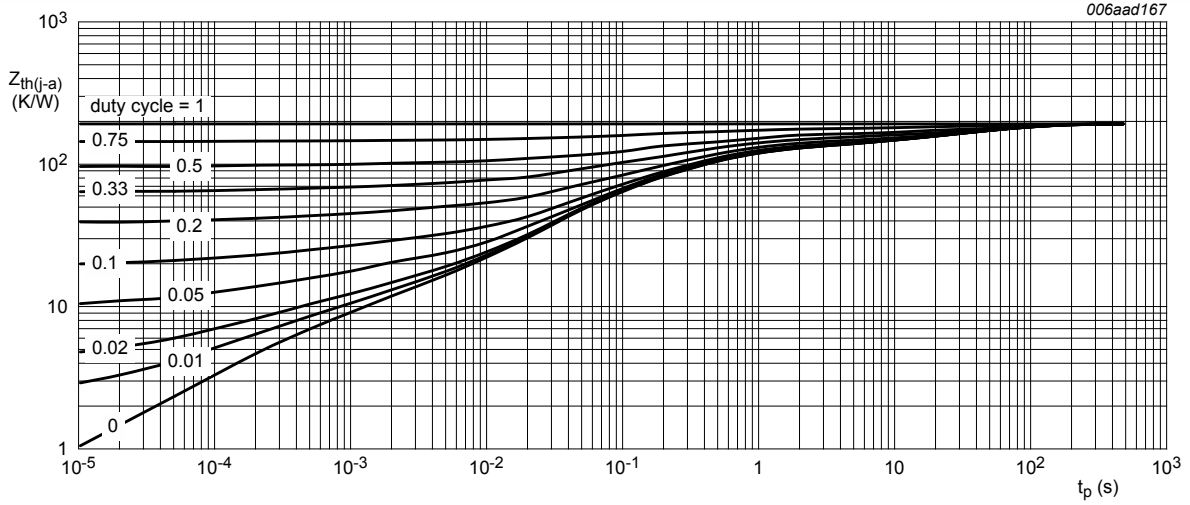
Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------------------|--|-------------|-----|-----|-----|-----|------|
| Per transistor | | | | | | | |
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | [1] | - | - | 338 | K/W |
| | | | [2] | - | - | 219 | K/W |
| | | | [3] | - | - | 236 | K/W |
| | | | [4] | - | - | 179 | K/W |
| | | | [5] | - | - | 278 | K/W |
| | | | [6] | - | - | 164 | K/W |
| | | | [7] | - | - | 179 | K/W |
| | | | [8] | - | - | 86 | K/W |
| R _{th(j-sp)} | thermal resistance from junction to solder point | | | - | - | 30 | K/W |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|----------------------|---|-------------|-----|-----|-----|-----|------|
| Per device | | | | | | | |
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | [1] | - | - | 245 | K/W |
| | | | [2] | - | - | 160 | K/W |
| | | | [3] | - | - | 171 | K/W |
| | | | [4] | - | - | 130 | K/W |
| | | | [5] | - | - | 202 | K/W |
| | | | [6] | - | - | 120 | K/W |
| | | | [7] | - | - | 130 | K/W |
| | | | [8] | - | - | 63 | K/W |

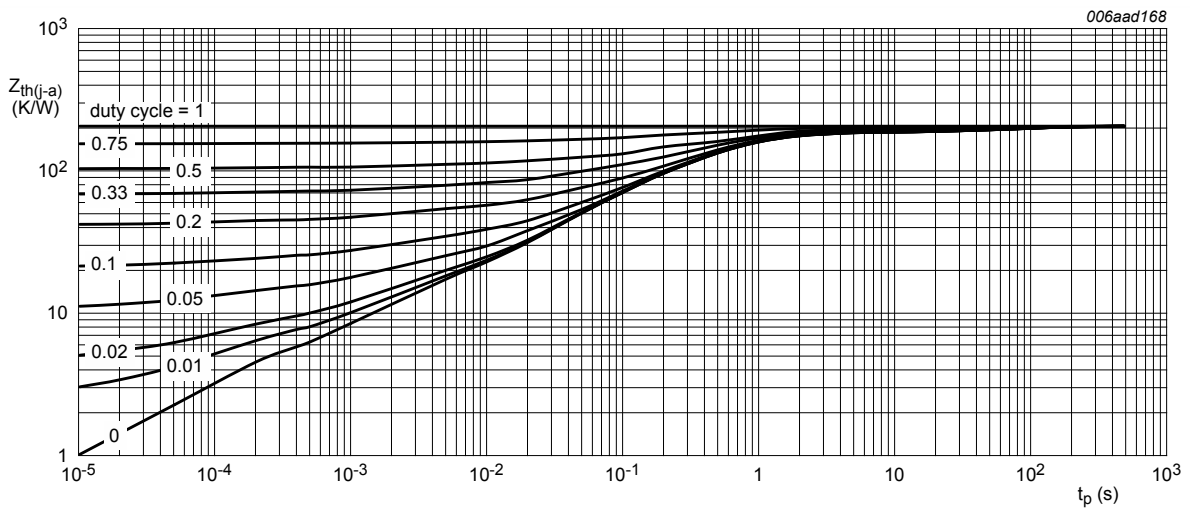
- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².





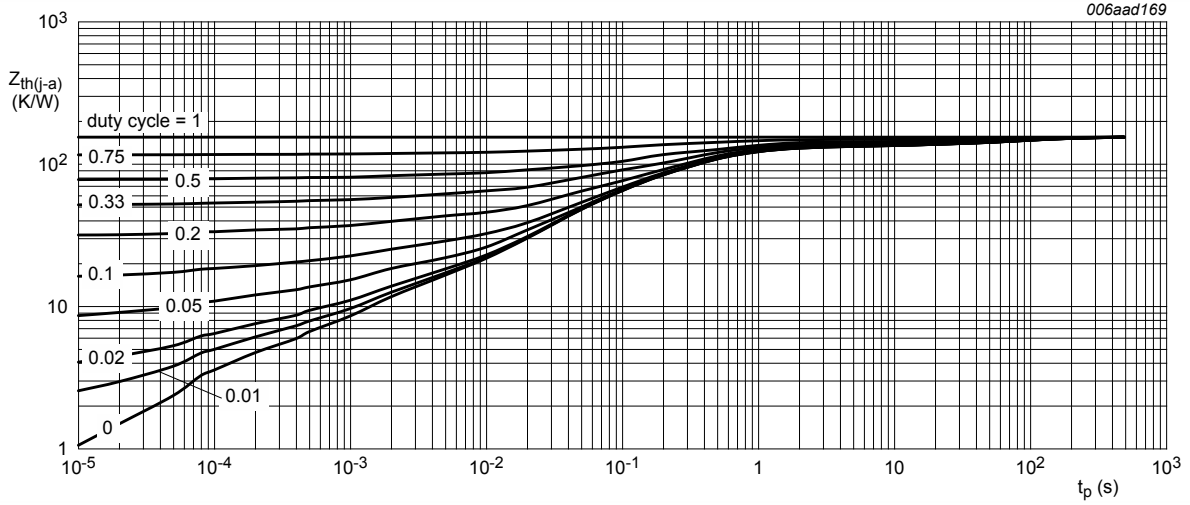
FR4 PCB 35 μ m, mounting pad for collector 1 cm²

Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



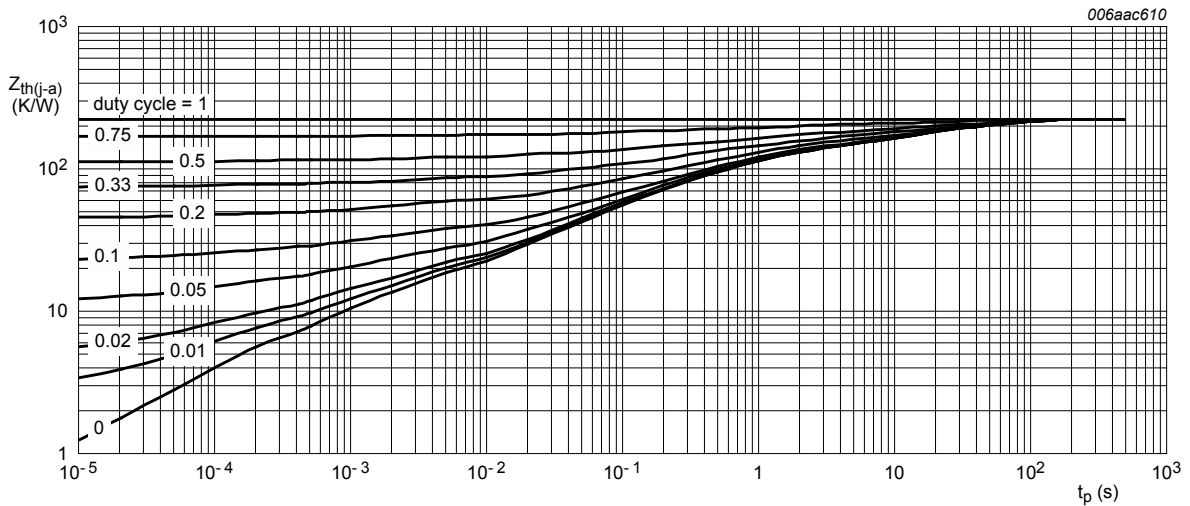
4-layer PCB 35 μ m, standard footprint

Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



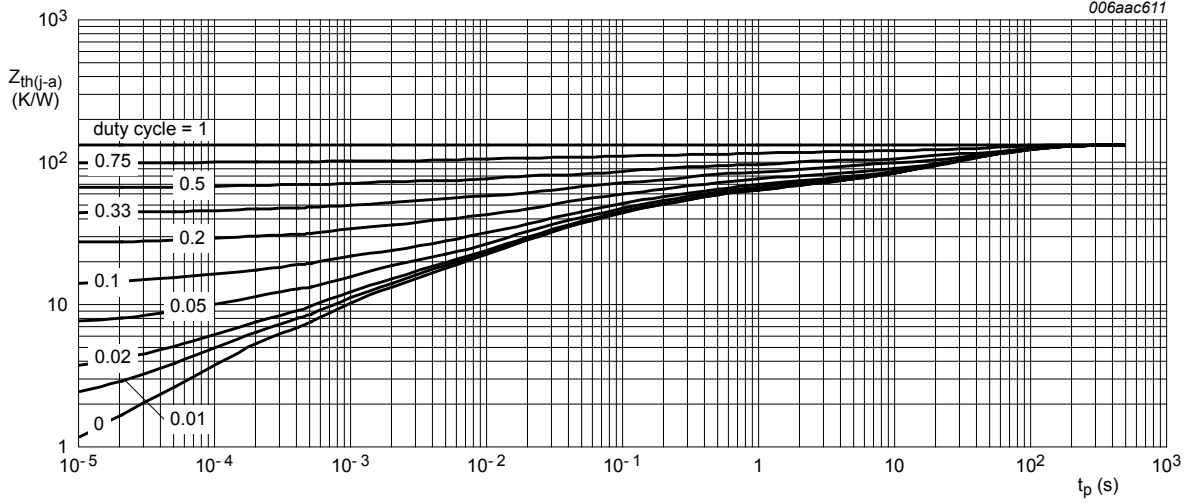
4-layer PCB 35 μ m, mounting pad for collector 1 cm²

Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



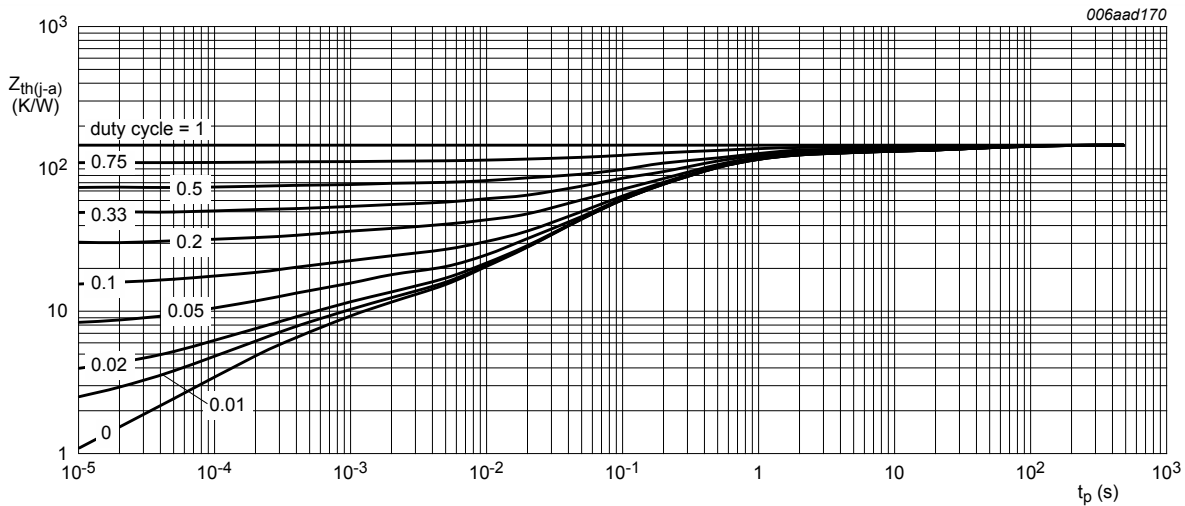
FR4 PCB 70 μ m, standard footprint

Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



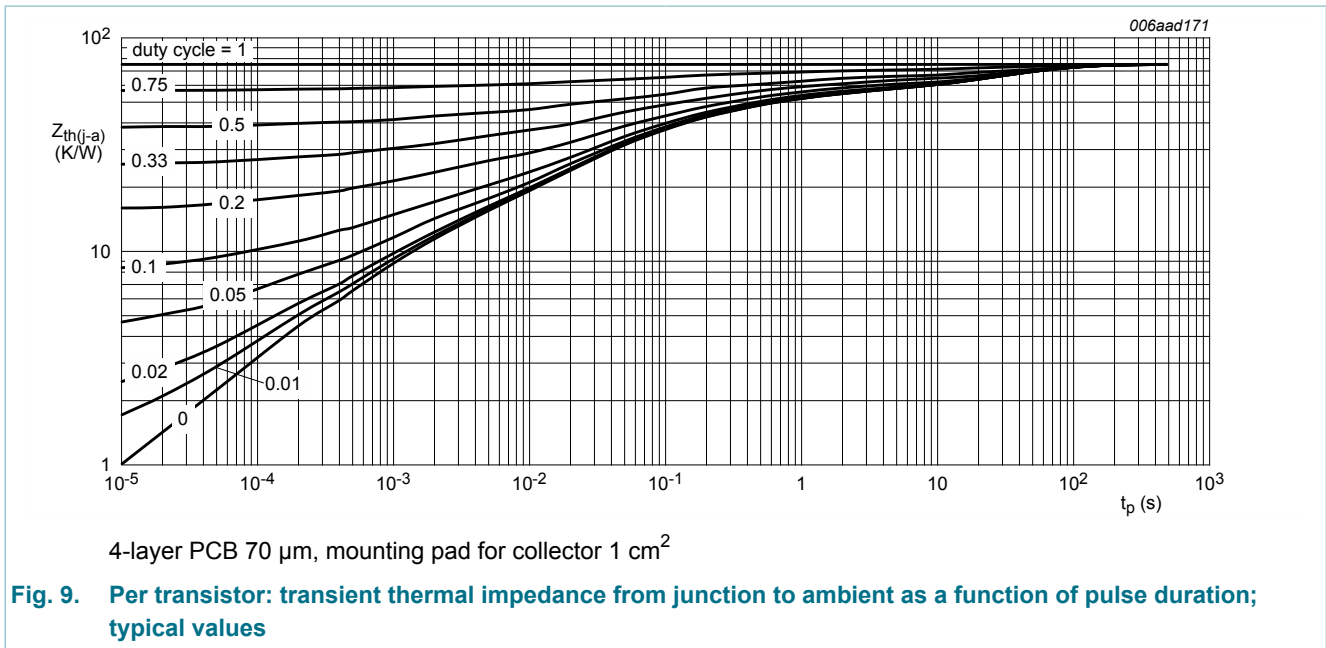
FR4 PCB 70 μm , mounting pad for collector 1 cm^2

Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



4-layer PCB 70 μm , standard footprint

Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|---|-----|------|------|---------------|
| Per transistor | | | | | | |
| I_{CBO} | collector-base cut-off current | $V_{CB} = -24 \text{ V}; I_E = 0 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$ | - | - | -100 | nA |
| | | $V_{CB} = -24 \text{ V}; I_E = 0 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$ | - | - | -50 | μA |
| I_{EBO} | emitter-base cut-off current | $V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$ | - | - | -100 | nA |
| h_{FE} | DC current gain | $V_{CE} = -2 \text{ V}; I_C = -100 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$ | 260 | 370 | - | |
| | | $V_{CE} = -2 \text{ V}; I_C = -500 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$ | 210 | 290 | - | |
| | | $V_{CE} = -2 \text{ V}; I_C = -1 \text{ A}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$ | 160 | 230 | - | |
| | | $V_{CE} = -2 \text{ V}; I_C = -2 \text{ A}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$ | 100 | 145 | - | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = -500 \text{ mA}; I_B = -50 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$ | - | -75 | -110 | mV |
| | | $I_C = -1 \text{ A}; I_B = -50 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$ | - | -155 | -220 | mV |
| | | $I_C = -2 \text{ A}; I_B = -100 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$ | - | -295 | -420 | mV |

30 V, 2 A PNP/PNP low VCEsat (BISS) transistor

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|---|---|------|------|------------|
| | | $I_C = -2\text{ A}; I_B = -200\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | -275 | -390 | mV |
| R_{CEsat} | collector-emitter saturation resistance | $I_C = -1\text{ A}; I_B = -0.1\text{ A};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | - | 195 | m Ω |
| V_{BEsat} | base-emitter saturation voltage | $I_C = -500\text{ mA}; I_B = -50\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | - | -1 | V |
| | | $I_C = -1\text{ A}; I_B = -50\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | - | -1 | V |
| | | $I_C = -2\text{ A}; I_B = -100\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | - | -1.1 | V |
| | | $I_C = -2\text{ A}; I_B = -200\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | - | -1.2 | V |
| V_{BEon} | base-emitter turn-on voltage | $V_{\text{CE}} = -2\text{ V}; I_C = -0.5\text{ A};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | - | -0.9 | V |
| t_d | delay time | $V_{\text{CC}} = -12.5\text{ V}; I_C = -1\text{ A}; I_{\text{Bon}} = -50\text{ mA};$ $I_{\text{Boff}} = 50\text{ mA}; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | 10 | - | ns |
| t_r | rise time | | - | 50 | - | ns |
| t_{on} | turn-on time | | - | 60 | - | ns |
| t_s | storage time | | - | 200 | - | ns |
| t_f | fall time | | - | 45 | - | ns |
| t_{off} | turn-off time | | - | 245 | - | ns |
| f_T | transition frequency | | $V_{\text{CE}} = -10\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz};$ $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | 50 | 95 | - |
| C_c | collector capacitance | $V_{\text{CB}} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | - | 22 | 29 | pF |

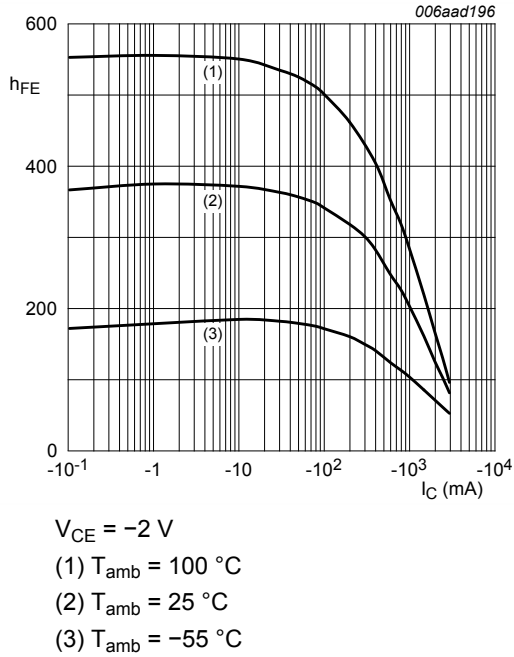


Fig. 10. DC current gain as a function of collector current; typical values

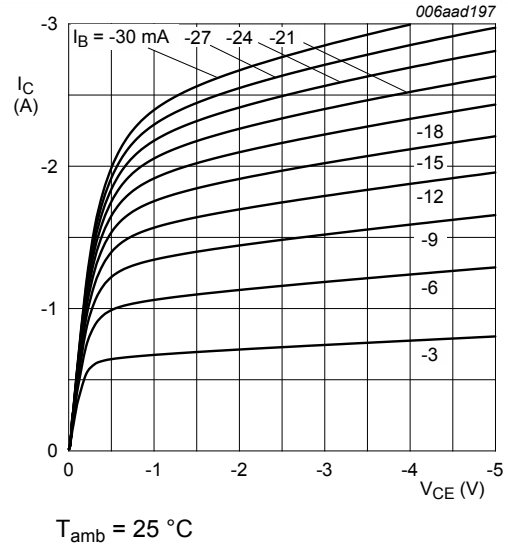


Fig. 11. Collector current as a function of collector-emitter voltage; typical values

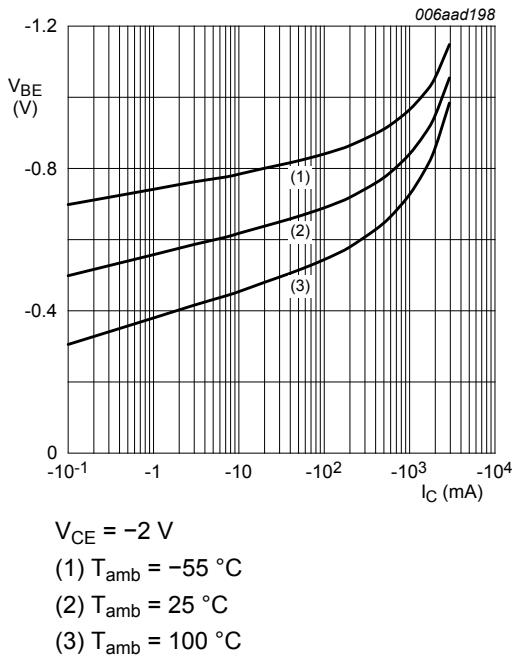


Fig. 12. Base-emitter voltage as a function of collector current; typical values

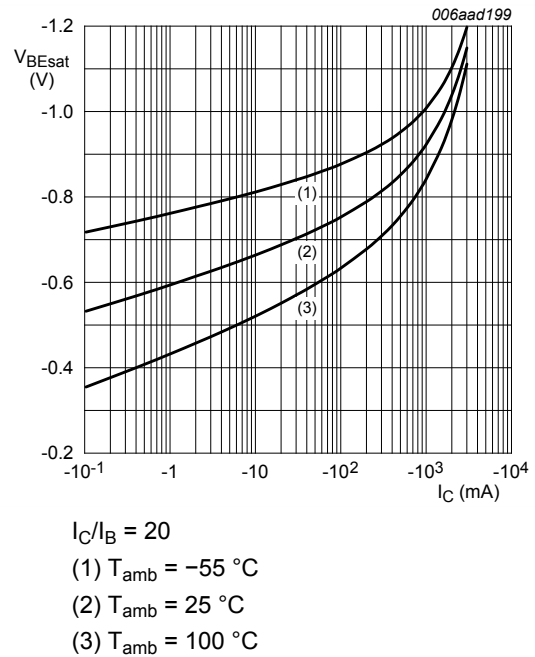
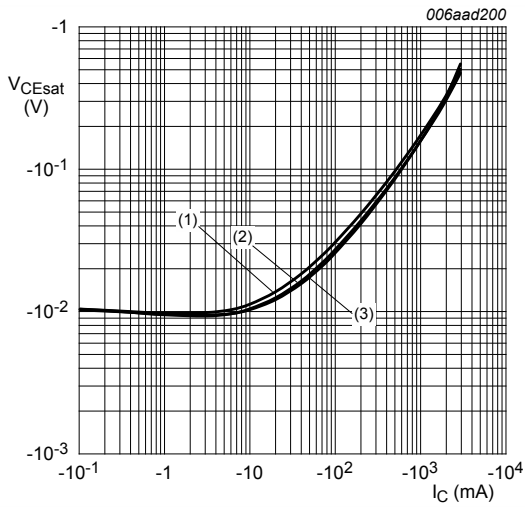
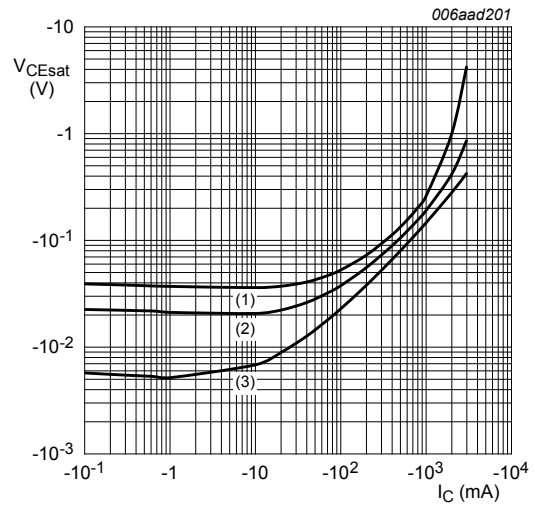


Fig. 13. Base-emitter saturation voltage as a function of collector current; typical values



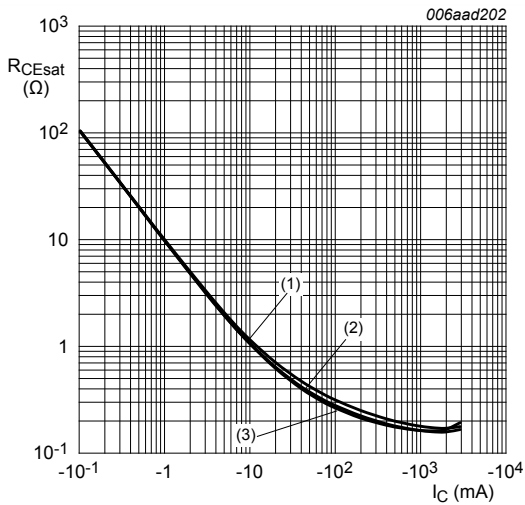
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = -55\text{ }^\circ\text{C}$

Fig. 14. Collector-emitter saturation voltage as a function of collector current; typical values



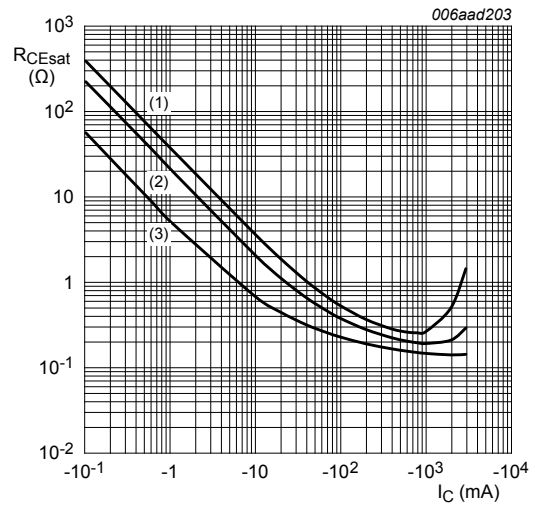
$T_{amb} = 25\text{ }^\circ\text{C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig. 15. Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = -55\text{ }^\circ\text{C}$

Fig. 16. Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25\text{ }^\circ\text{C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig. 17. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

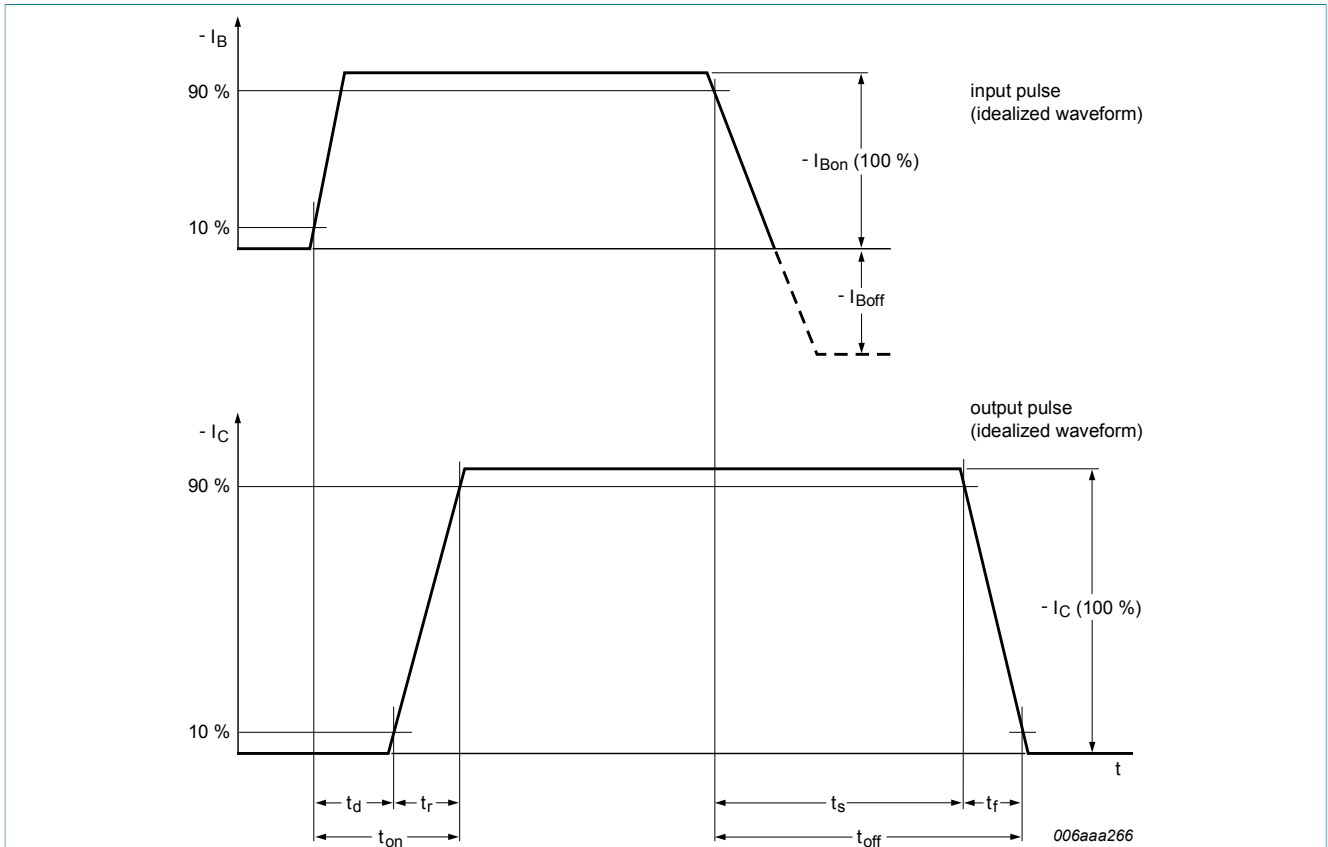


Fig. 18. BISS transistor switching time definition

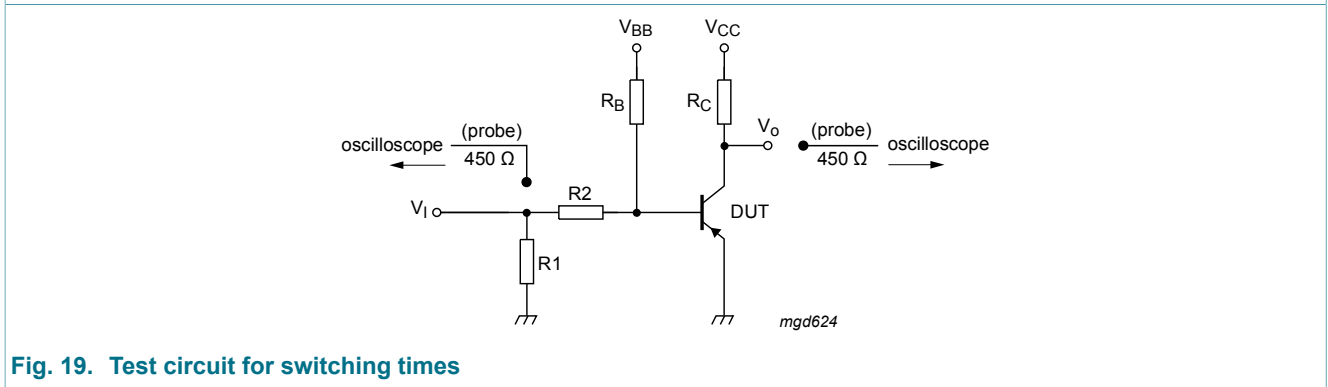


Fig. 19. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

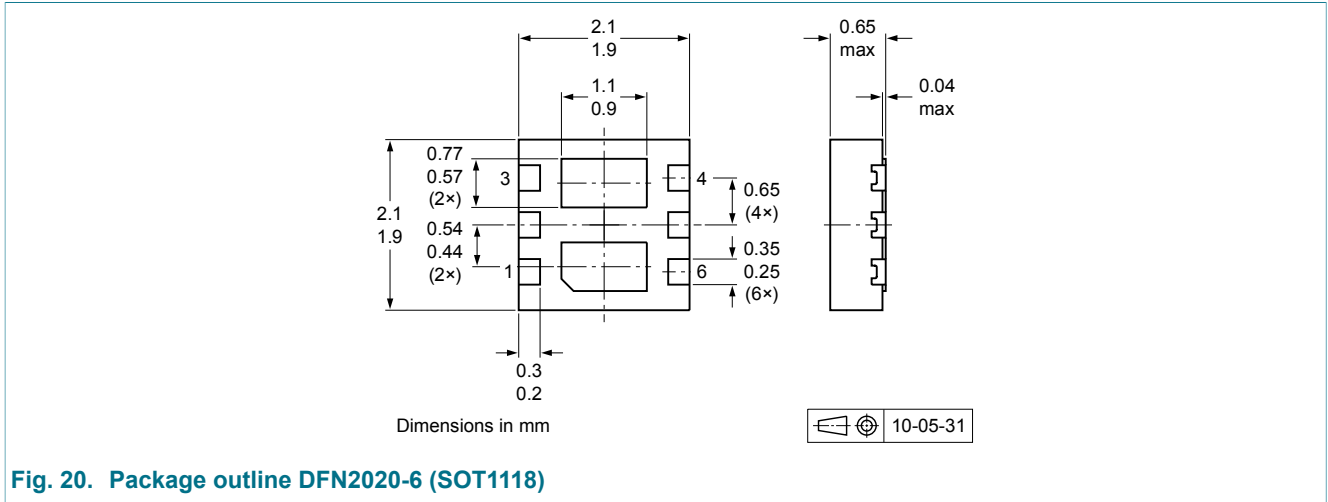


Fig. 20. Package outline DFN2020-6 (SOT1118)

13. Soldering

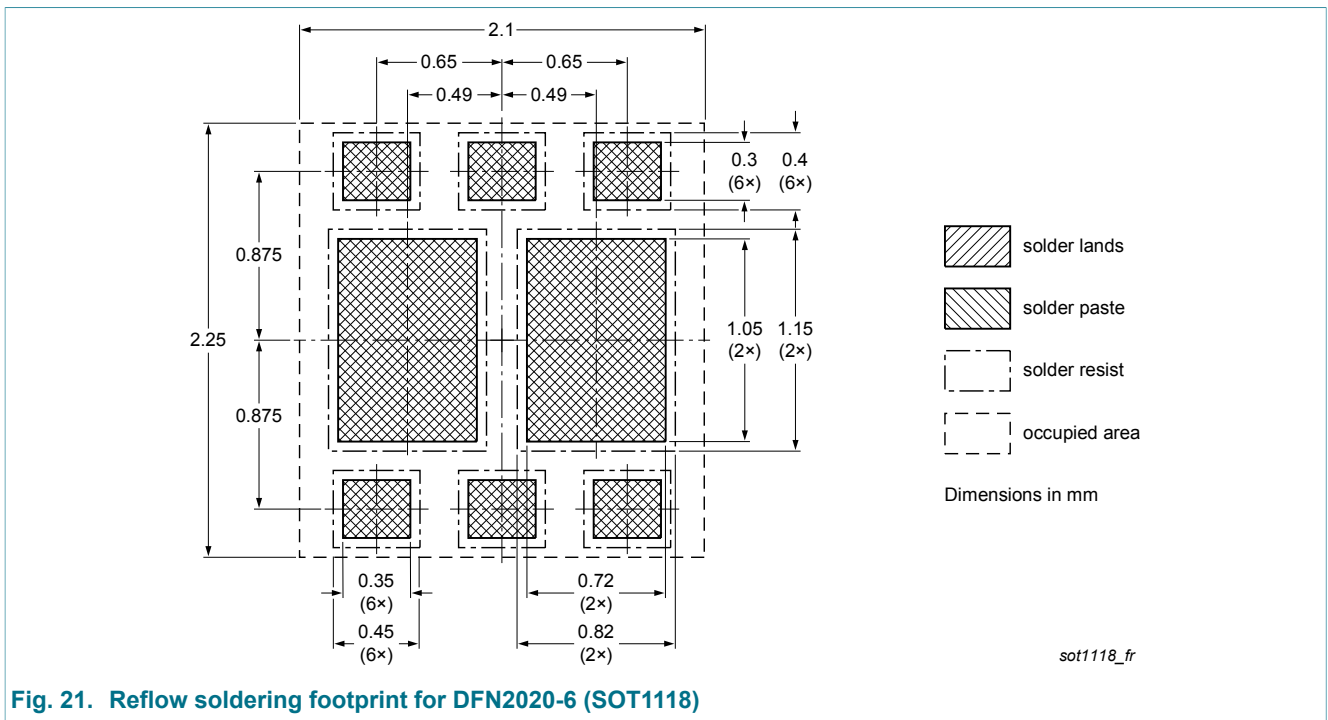


Fig. 21. Reflow soldering footprint for DFN2020-6 (SOT1118)

14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| PBSS5230PAP v.1 | 20130111 | Product data sheet | - | - |

15. Legal information

15.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
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16. Contents

| | | |
|------|-------------------------------|----|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Applications | 1 |
| 4 | Quick reference data | 1 |
| 5 | Pinning information | 2 |
| 6 | Ordering information | 2 |
| 7 | Marking | 2 |
| 8 | Limiting values | 2 |
| 9 | Thermal characteristics | 4 |
| 10 | Characteristics | 9 |
| 11 | Test information | 13 |
| 11.1 | Quality information | |
| 12 | Package outline | 14 |
| 13 | Soldering | 14 |
| 14 | Revision history | 14 |
| 15 | Legal information | 15 |
| 15.1 | Data sheet status | 15 |
| 15.2 | Definitions | 15 |
| 15.3 | Disclaimers | 15 |
| 15.4 | Trademarks | 16 |

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