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Team Nexperia



PBSS5260PAPS

60 V, 2 A PNP/PNP low V_{CEsat} (BISS) double transistor

15 December 2015

Product data sheet

1. General description

PNP/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) double transistor in a leadless medium power DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

NPN/NPN complement: PBSS4260PANS

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- Exposed heat sink for excellent thermal and electrical conductivity
- High energy efficiency due to less heat generation
- Suitable for Automatic Optical Inspection (AOI) of solder joints
- AEC-Q101 qualified

3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- LED lighting
- Power switches (e.g. motors, fans)

4. Quick reference data

Table 1. Quick reference data

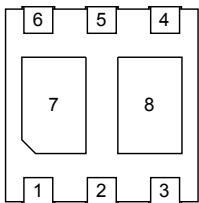
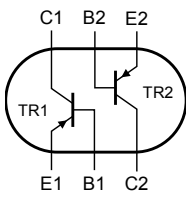
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-60	V
I_C	collector current		-	-	-2	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-3	A



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R _{CEsat}	collector-emitter saturation resistance	I _C = -1 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	-	310	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view DFN2020D-6 (SOT1118D)</p>	 <p><i>sym138</i></p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS5260PAPS	DFN2020D-6	DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118D

7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS5260PAPS	3H

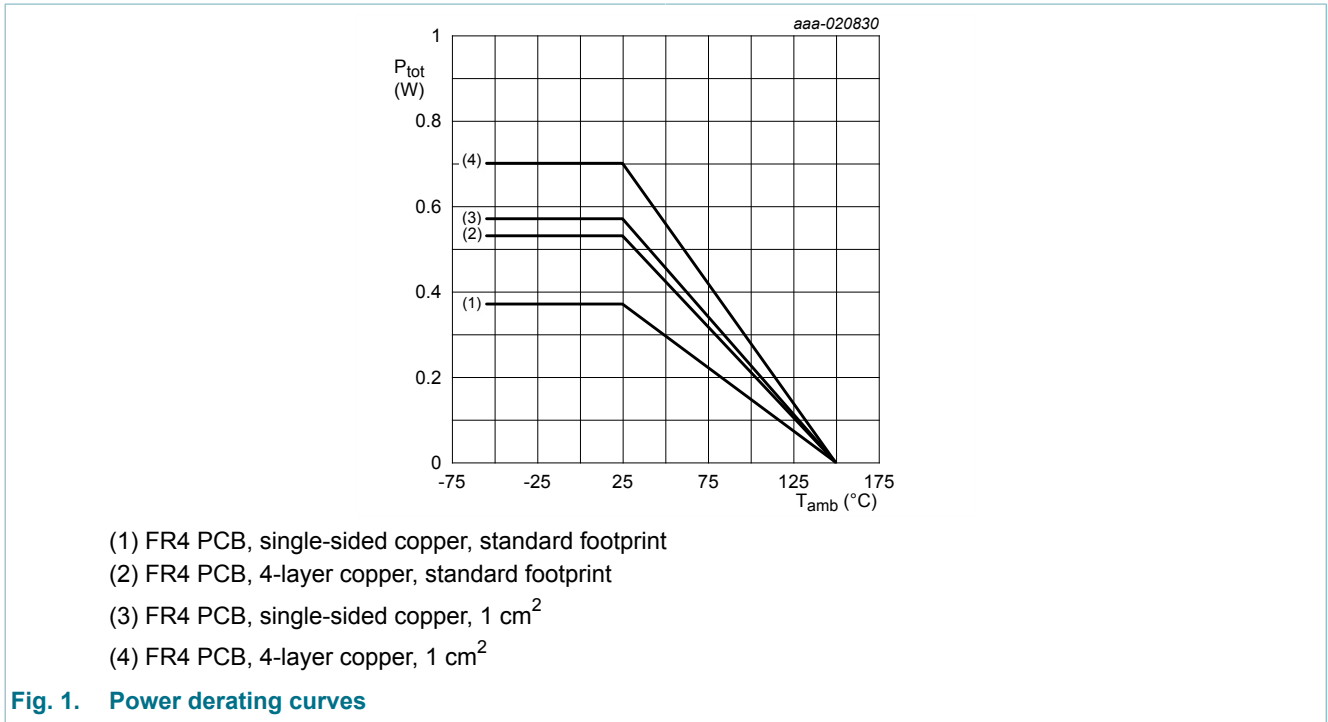
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CB0}	collector-base voltage	open emitter		-	-60	V
V _{CEO}	collector-emitter voltage	open base		-	-60	V
V _{EBO}	emitter-base voltage	open collector		-	-7	V
I _C	collector current			-	-2	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	-3	A
I _B	base current			-	-0.3	A
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	-1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated; mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated; mounting pad for collector 1 cm².



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	246	K/W
			[2]	-	-	161	K/W
			[3]	-	-	172	K/W
			[4]	-	-	131	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated, mounting pad for collector 1 cm².

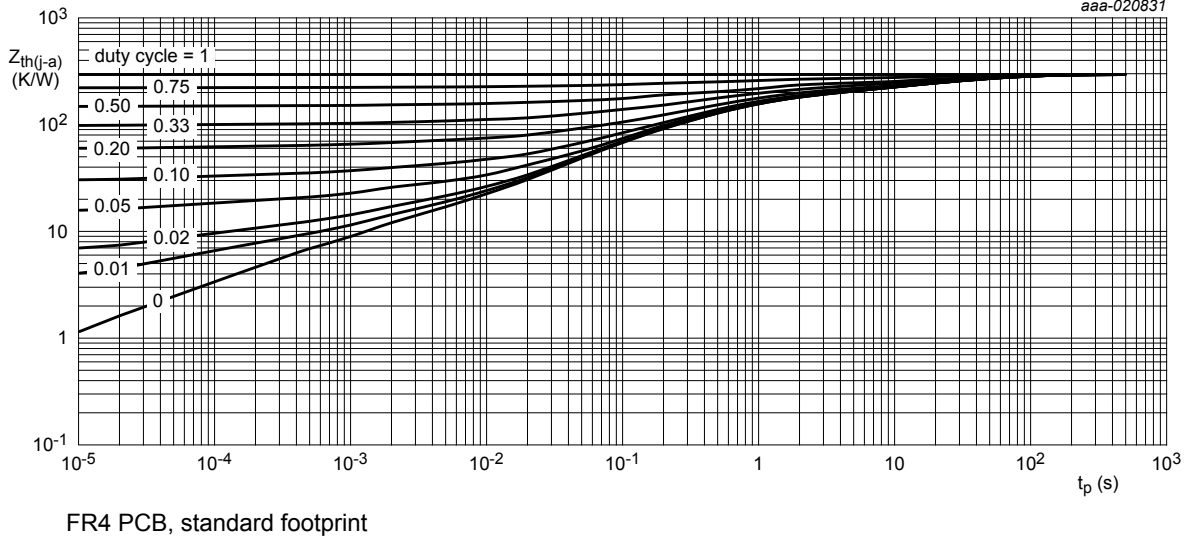


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

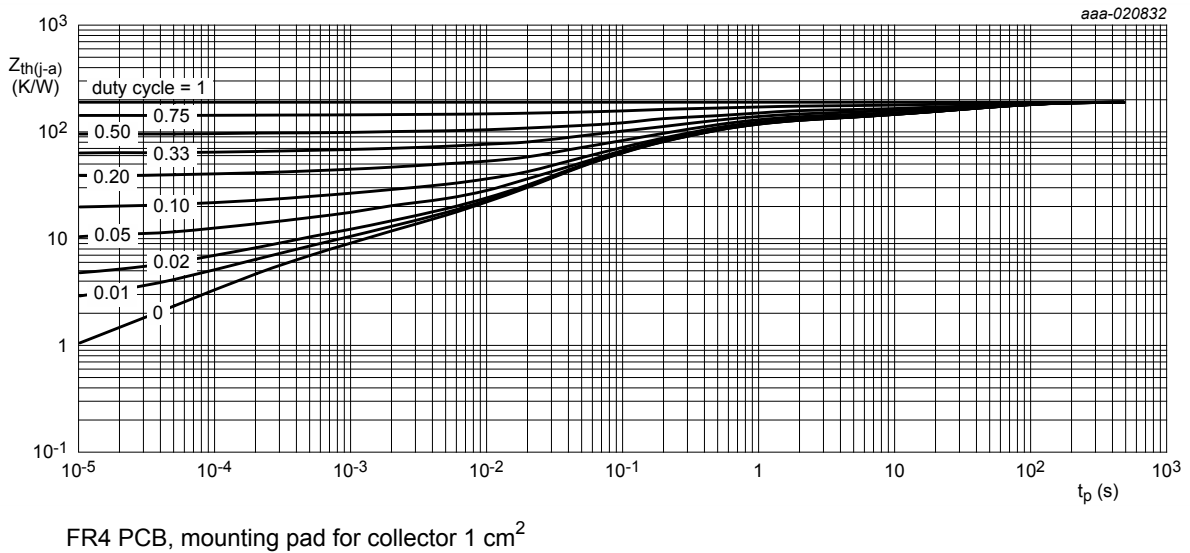


Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

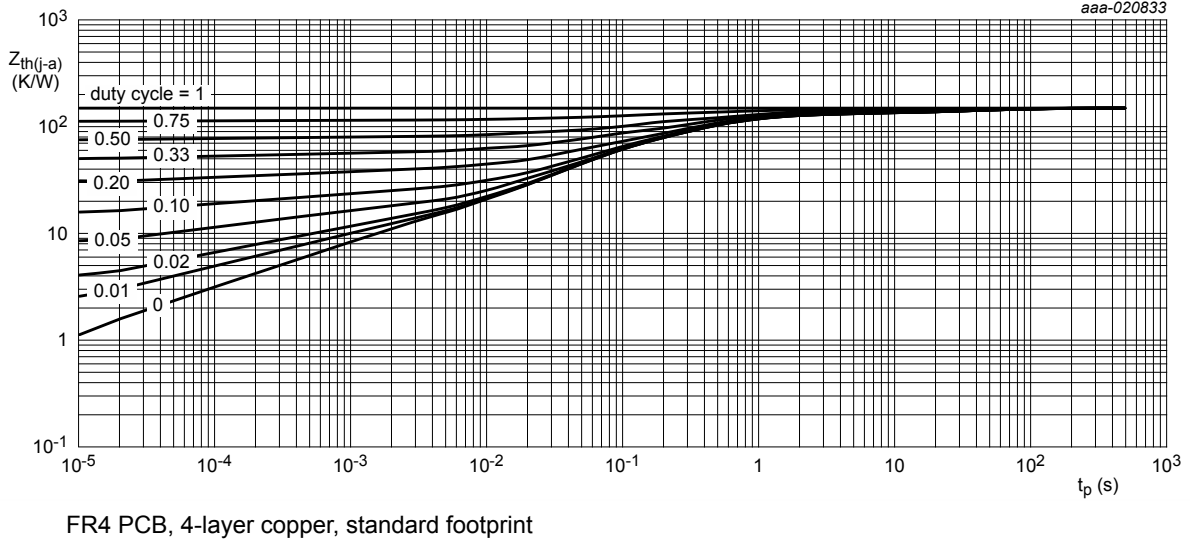


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

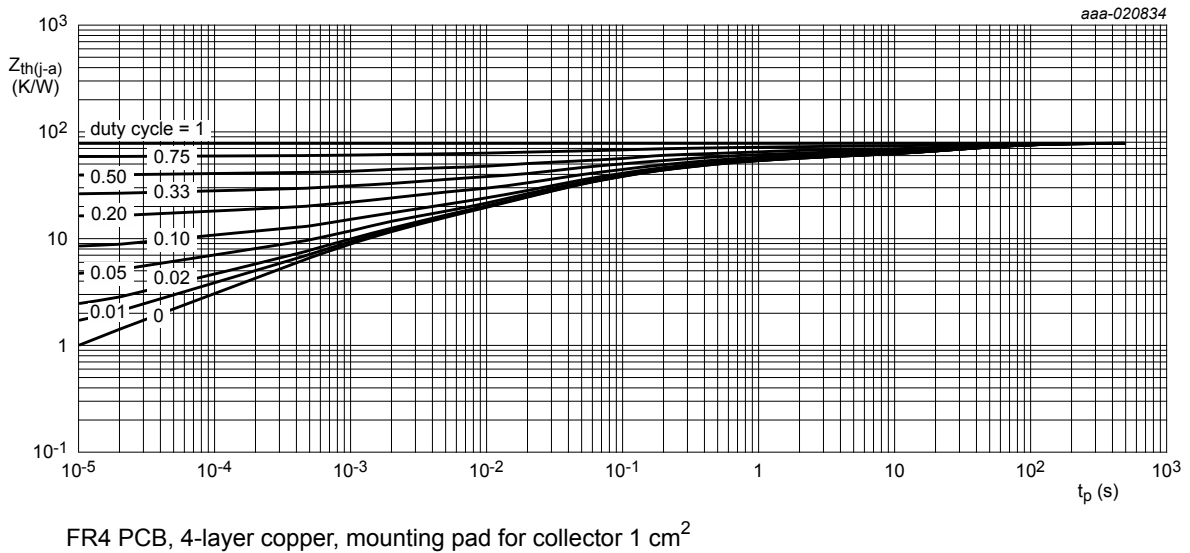


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

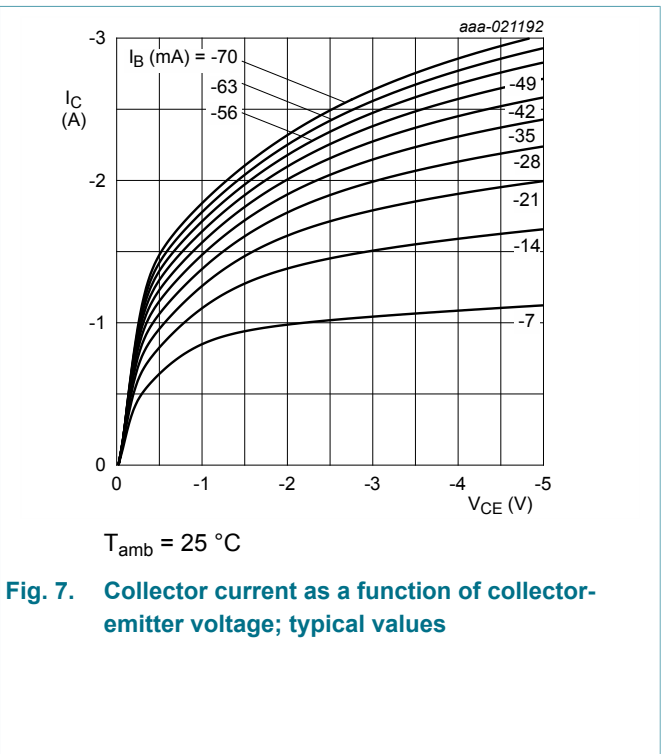
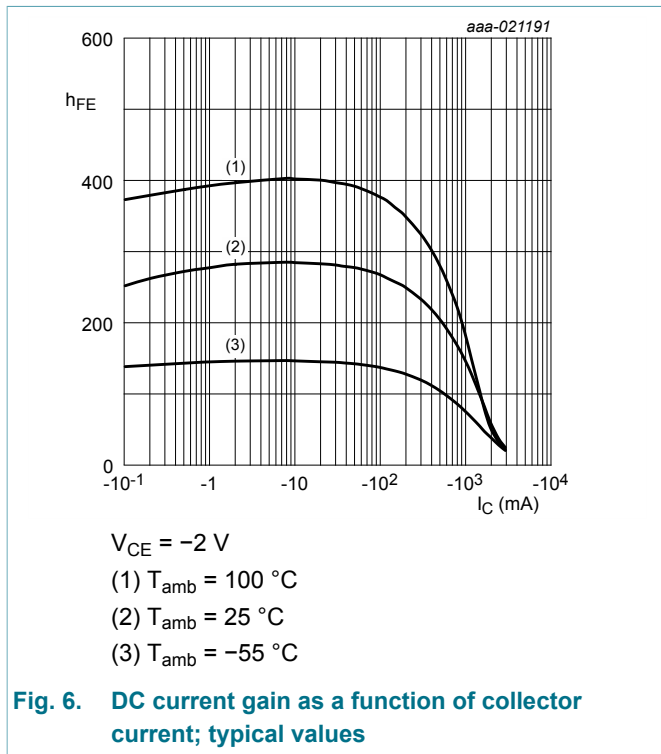
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = -48 V; I _E = 0 A; T _{amb} = 25 °C	-	-	-100	nA
		V _{CB} = -48 V; I _E = 0 A; T _j = 150 °C	-	-	-50	μA
I _{CES}	collector-emitter cut-off current	V _{CE} = -48 V; V _{BE} = 0 V; T _{amb} = 25 °C	-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -2 V; I _C = -100 mA; pulsed; t _p ## 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	170	250	-	
		V _{CE} = -2 V; I _C = -500 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	140	200	-	
		V _{CE} = -2 V; I _C = -1 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	110	150	-	
		V _{CE} = -2 V; I _C = -2 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02	50	75	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -0.5 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	-100	-140	mV
		I _C = -1 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	-200	-310	mV
		I _C = -2 A; I _B = -200 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	-350	-500	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -1 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	-	310	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = -0.5 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	-0.89	-1	V
		I _C = -1 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.93	-1.1	V
		I _C = -2 A; I _B = -200 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-1.14	-1.25	V
V _{BE}	base-emitter voltage	I _C = -0.5 A; V _{CE} = -2 V; pulsed; t _p ≤ 300 μs; δ _{factor} ≤ 0.02; T _{amb} = 25 °C	-	-0.77	-0.9	V
t _d	delay time	I _C = -1 A; I _{Bon} = -50 mA; I _{Boff} = 50 mA; T _{amb} = 25 °C	-	10	-	ns
t _r	rise time		-	80	-	ns
t _{on}	turn-on time		-	90	-	ns
t _s	storage time		-	195	-	ns

60 V, 2 A PNP/PNP low VCEsat (BISS) double transistor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time		-	75	-	ns
t_{off}	turn-off time		-	270	-	ns
f_T	transition frequency	$V_{CE} = -10\text{ V}; I_C = -500\text{ mA};$ $f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	100	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	16	-	pF



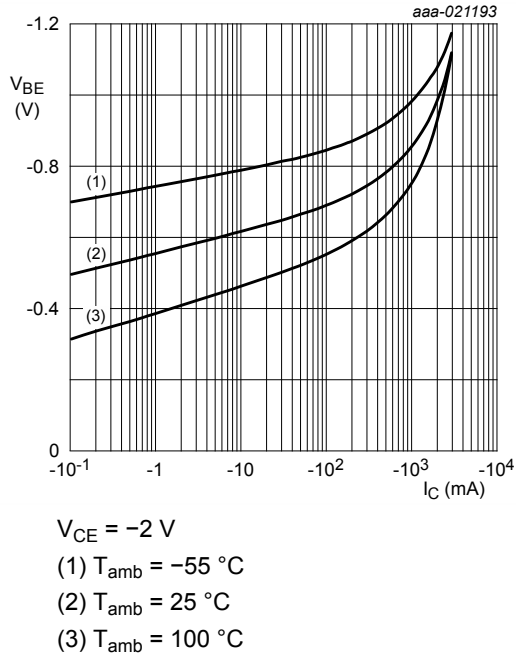


Fig. 8. Base-emitter voltage as a function of collector current; typical values

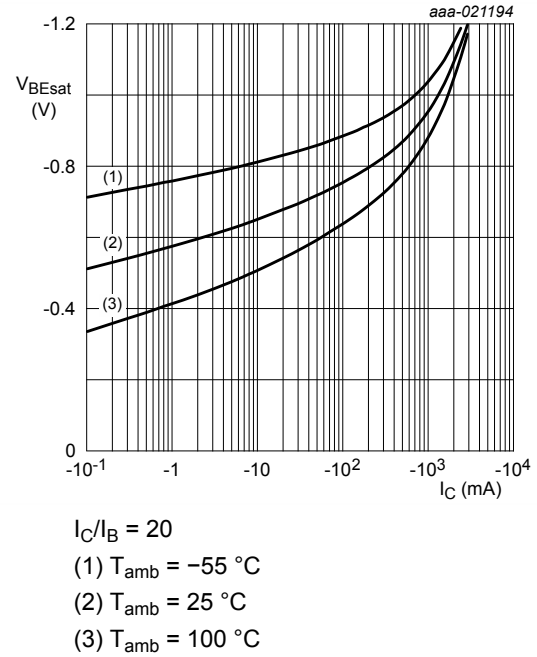


Fig. 9. Base-emitter saturation voltage as a function of collector current; typical values

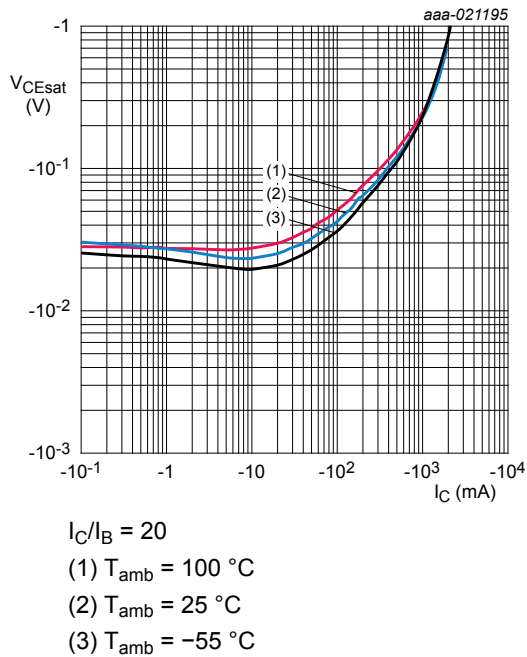


Fig. 10. Collector-emitter saturation voltage as a function of collector current; typical values

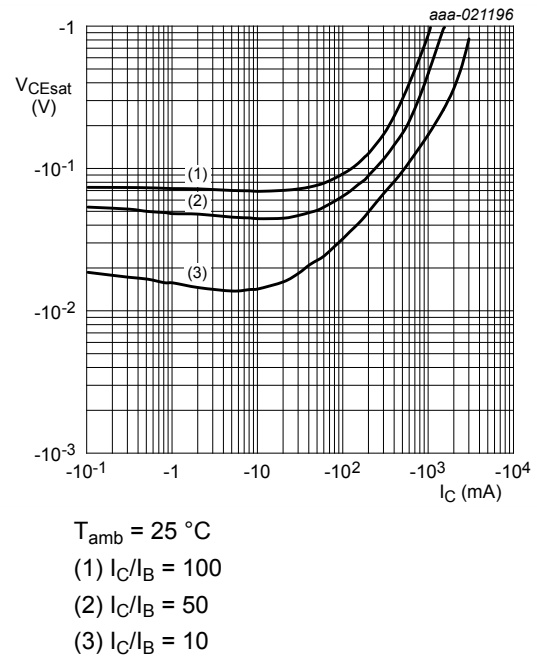
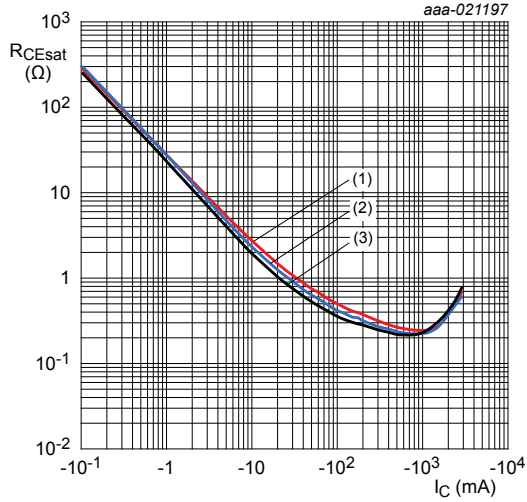
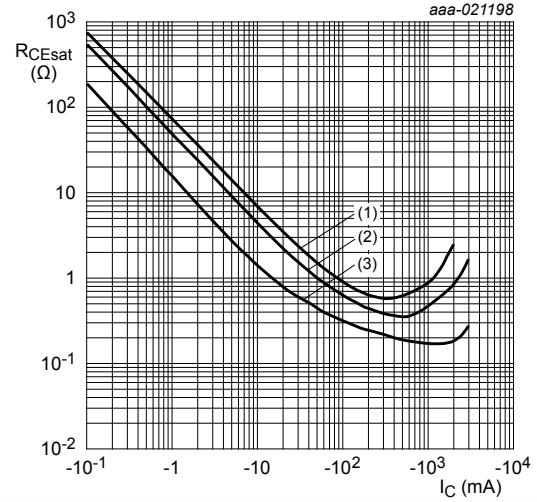


Fig. 11. Collector-emitter saturation voltage as a function of collector current; typical values



- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -55\text{ °C}$

Fig. 12. Collector-emitter saturation resistance as a function of collector current; typical values



- $T_{amb} = 25\text{ °C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig. 13. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

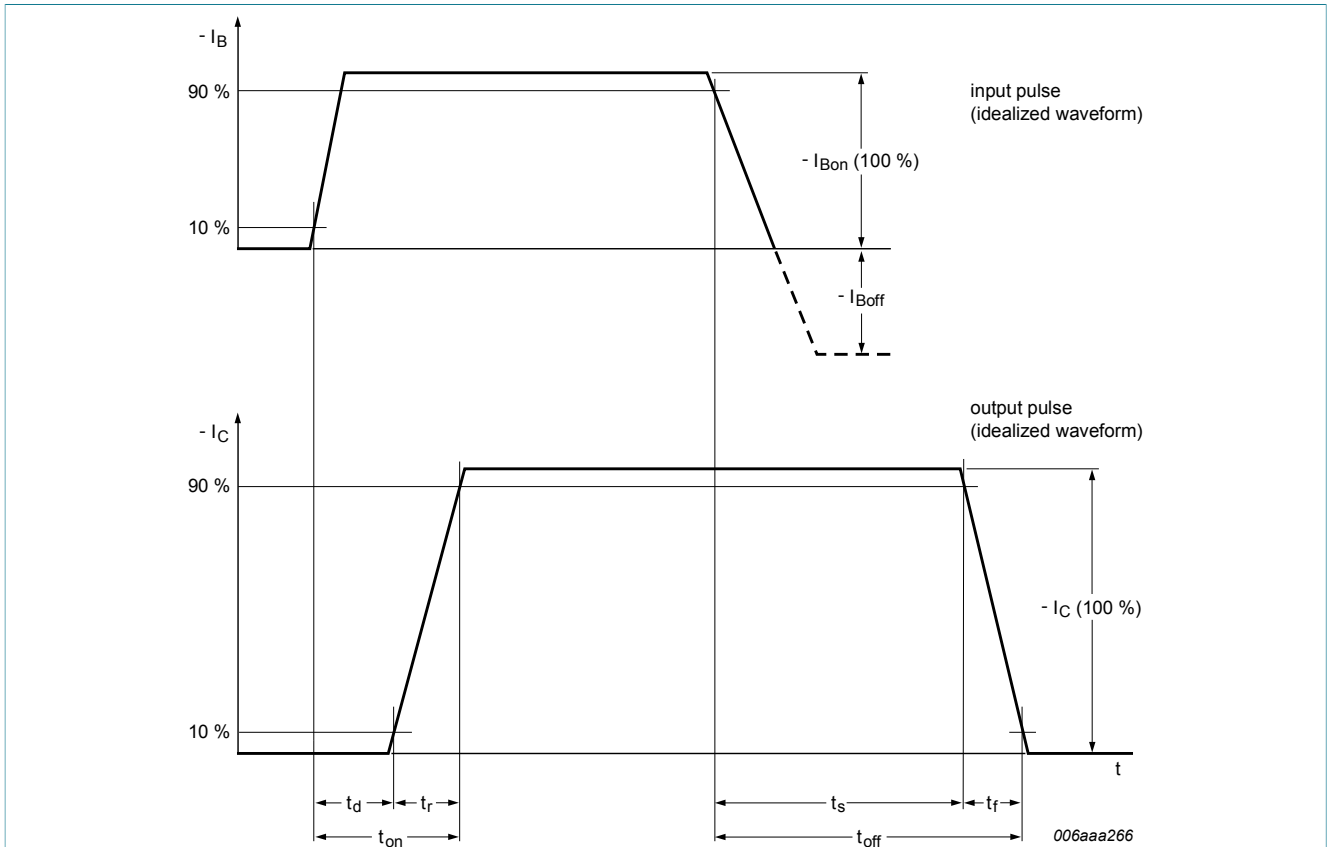


Fig. 14. BISS transistor switching time definition

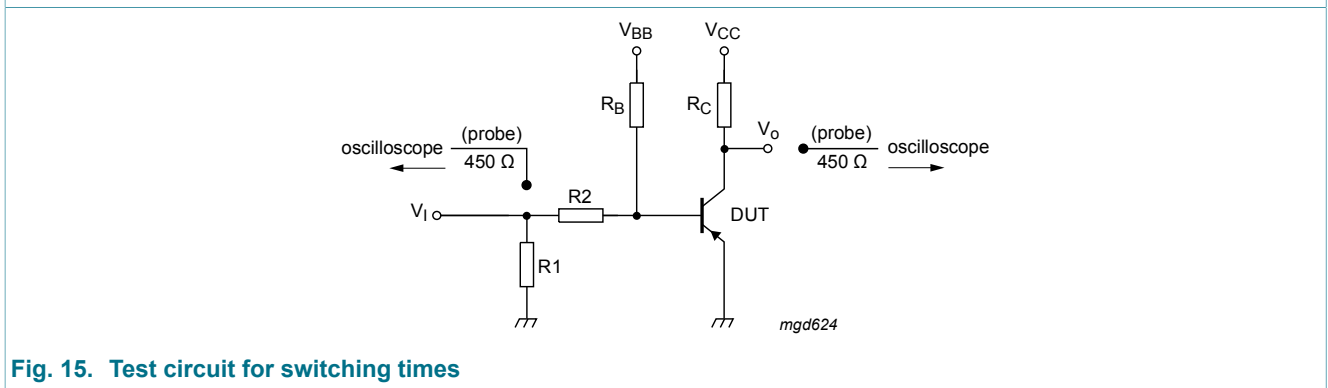


Fig. 15. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1118D

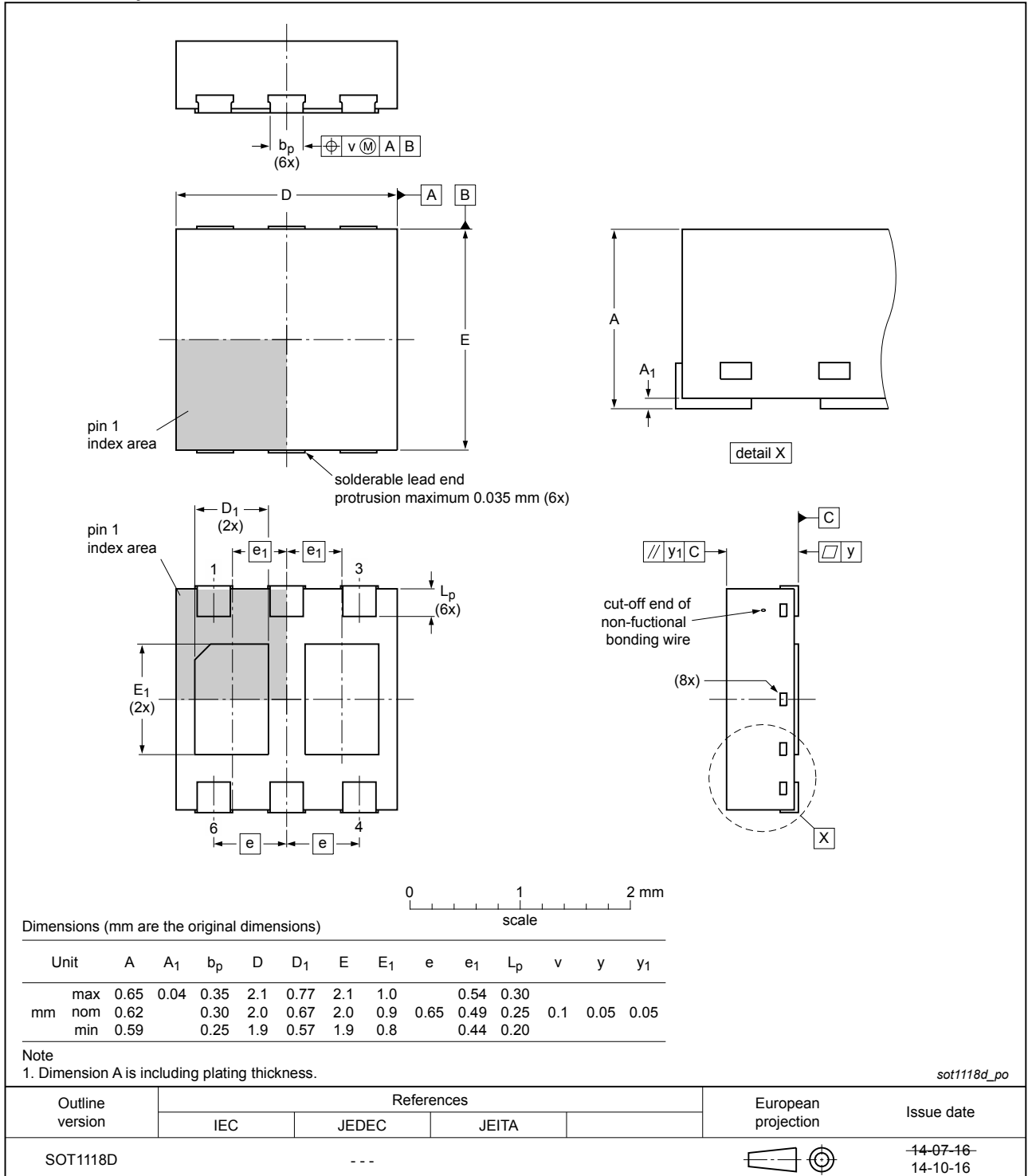


Fig. 16. Package outline DFN2020D-6 (SOT1118D)

13. Soldering

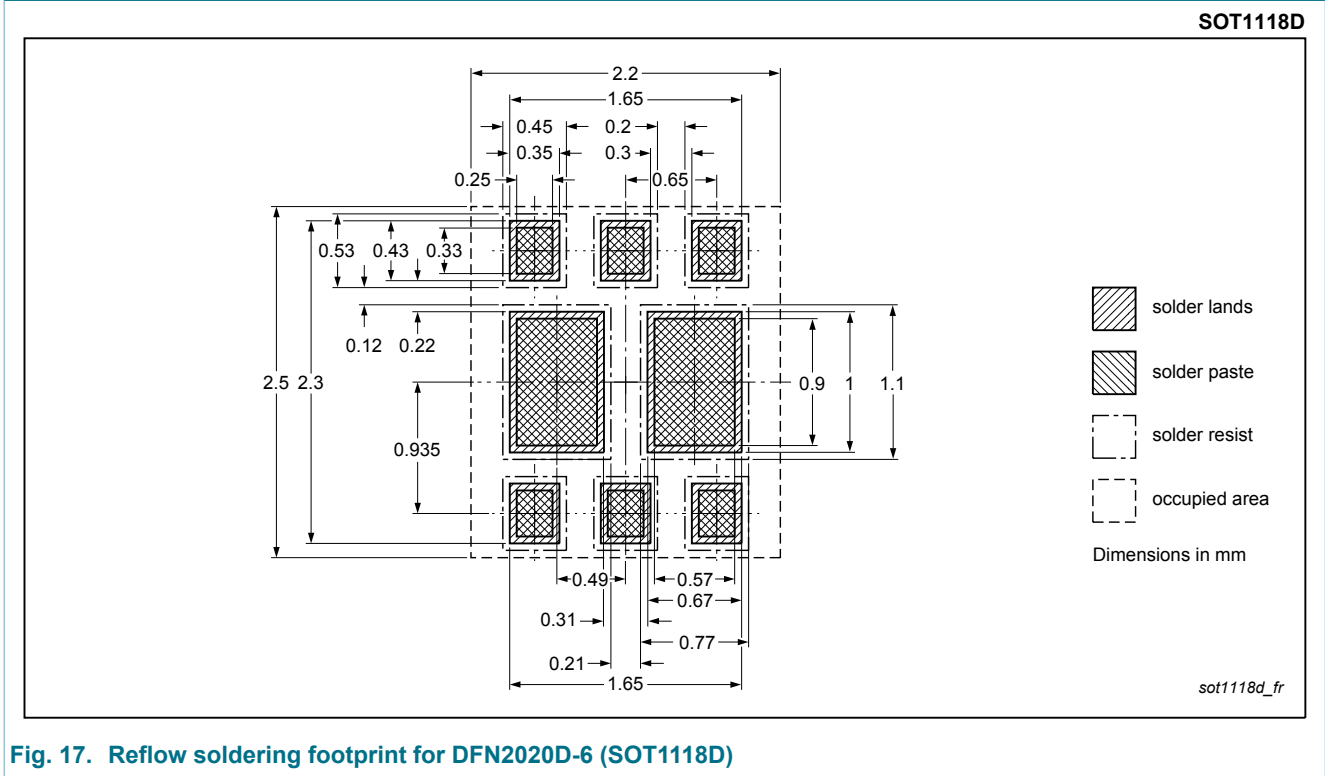


Fig. 17. Reflow soldering footprint for DFN2020D-6 (SOT1118D)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5260PAPS v.1	20151215	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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