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Parallel NOR Flash Embedded Memory

JS28F256M29EWxx, PC28F256M29EWxx, RC28F256M29EWxx
JS28F512M29EWxx, PC28F512M29EWxx, RC28F512M29EWxx
JS28F00AM29EWxx, PC28F00AM29EWxx, RC28F00AM29EWxx
PC28F00BM29EWxx, RC28F00BM29EWxx

Features

- 2Gb = stacked device (two 1Gb die)
- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–3.6V (I/O buffers)
- Asynchronous random/page read
  - Page size: 16 words or 32 bytes
  - Page access: 25ns
  - Random access: 100ns (Fortified BGA); 110ns (TSOP)
- Buffer program: 512-word program buffer
- Program time
  - 0.88µs per byte (1.14 MB/s) TYP when using full 512-word buffer size in buffer program
- Memory organization
  - Uniform blocks: 128-Kbytes or 64-Kwords each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/erase suspend and resume capability
  - Read from any block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- BLANK CHECK operation to verify an erased block
- Unlock bypass, block erase, chip erase, and write to buffer capability
  - Fast buffered/batch programming
  - Fast block/chip erase
- V_{PP}/WP# pin protection
  - Protects first or last block regardless of block protection settings
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
  - Password access
- Extended memory block
  - 128-word (256-byte) block for permanent, secure identification
  - Programmed or locked at the factory or by the customer
- Low power consumption: Standby mode
- JESD47H-compliant
  - 100,000 minimum ERASE cycles per block
  - Data retention: 20 years (TYP)
- 65nm multilevel cell (MLC) process technology
- Fortified BGA and TSOP packages
- Green packages available
  - RoHS-compliant
  - Halogen-free
- Operating temperature
  - Ambient: –40°C to +85°C

Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details	Notes
Package	JS = 56-pin TSOP, 14mm x 20mm, lead-free, halogen-free, RoHS-compliant	
	PC = 64-ball Fortified BGA, 11mm x 13mm, lead-free, halogen-free, RoHS-compliant	
	RC = 64-ball Fortified BGA, 11mm x 13mm, leaded	
Product designator	28F = NOR parallel interface	
Density	256 = 256Mb	
	512 = 512Mb	
	00A = 1Gb	
	00B = 2Gb	
Device type	M29EW = Embedded Flash memory (3V core, page, uniform block)	
Device function	H = Highest block protected by V_{PP}/WP#	1
	L = Lowest block protected by V_{PP}/WP#	
Features	A/B/D/E or an asterisk (*) = Combination of features, including packing media, special features, and specific customer request information	

Note: 1. For 2Gb device, *H* also indicates protection of the lowest block by V_{PP}/WP#.

Table 2: Standard Part Numbers by Density, Medium, and Package

Density	Medium	Package		
		JS	PC	RC
256Mb	Tray	JS28F256M29EWHA	PC28F256M29EWHA	RC28F256M29EWHA
		JS28F256M29EWLA	PC28F256M29EWLA	RC28F256M29EWLA
	Tape and Reel	JS28F256M29EWHB	PC28F256M29EWHB	RC28F256M29EWHB
		JS28F256M29EWLB	PC28F256M29EWLB	–
512Mb	Tray	JS28F512M29EWHA	PC28F512M29EWHD	RC28F512M29EWHA
		JS28F512M29EWLA	PC28F512M29EWLA	RC28F512M29EWLA
	Tape and Reel	JS28F512M29EWHB	PC28F512M29EWHB	RC28F512M29EWHB
		JS28F512M29EWLB	PC28F512M29EWLB	–
1Gb	Tray	JS28F00AM29EWHA	PC28F00AM29EWHA	RC28F00AM29EWHA
		JS28F00AM29EWLA	PC28F00AM29EWLA	RC28F00AM29EWLA
	Tape and Reel	JS28F00AM29EWHB	PC28F00AM29EWHB	RC28F00AM29EWHB
2Gb	Tray	–	PC28F00BM29EWHA	RC28F00BM29EWHA

Note: 1. For security features and part numbers, contact your local Micron sales representative.

Table 3: Part Numbers with Security Features by Density, Medium, and Package

Density	Medium	Package		
		JS	PC	RC
256Mb	Tray	–	PC28F256M29EWHD	–
		–	PC28F256M29EWLD	–
	Tape and Reel	–	–	–
512Mb	Tray	–	PC28F512M29EWHA	–
		–	PC28F512M29EWLE	–
	Tape and Reel	–	PC28F512M29EWHE	–
1Gb	Tray	–	PC28F00AM29EWHD	–
			PC28F00AM29EWLE	
	Tape and Reel	–	–	–

Note: 1. This data sheet covers only standard parts. For security parts, contact your local Micron sales representative.

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General Description

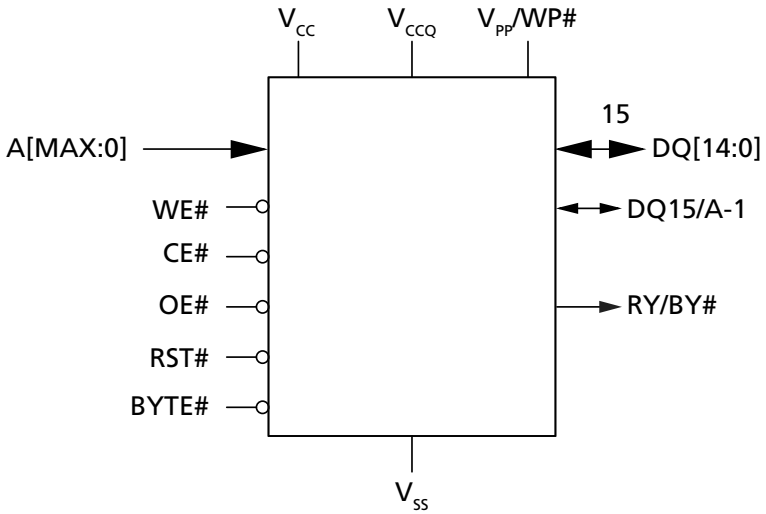
The M29EW is an asynchronous, uniform block, parallel NOR Flash memory device manufactured on 65nm multilevel cell (MLC) technology. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

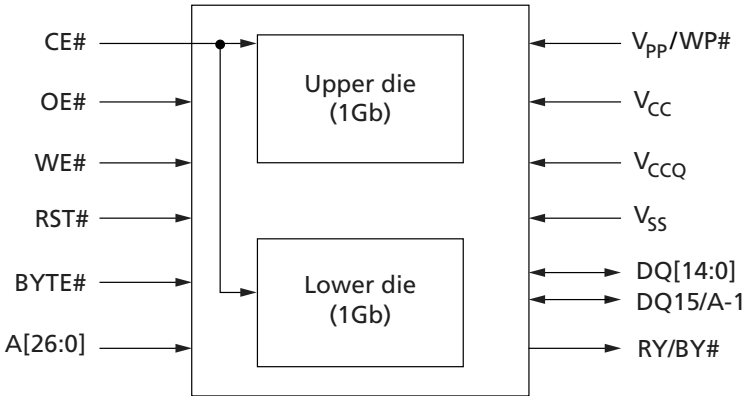
The M29EW supports asynchronous random read and page read from all blocks of the array. It also features an internal program buffer that improves throughput by programming 512 words via one command sequence. The device contains a 128-word extended memory block which overlaps addresses with array block 0. The user can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

Figure 1: Logic Diagram



Device Configurability

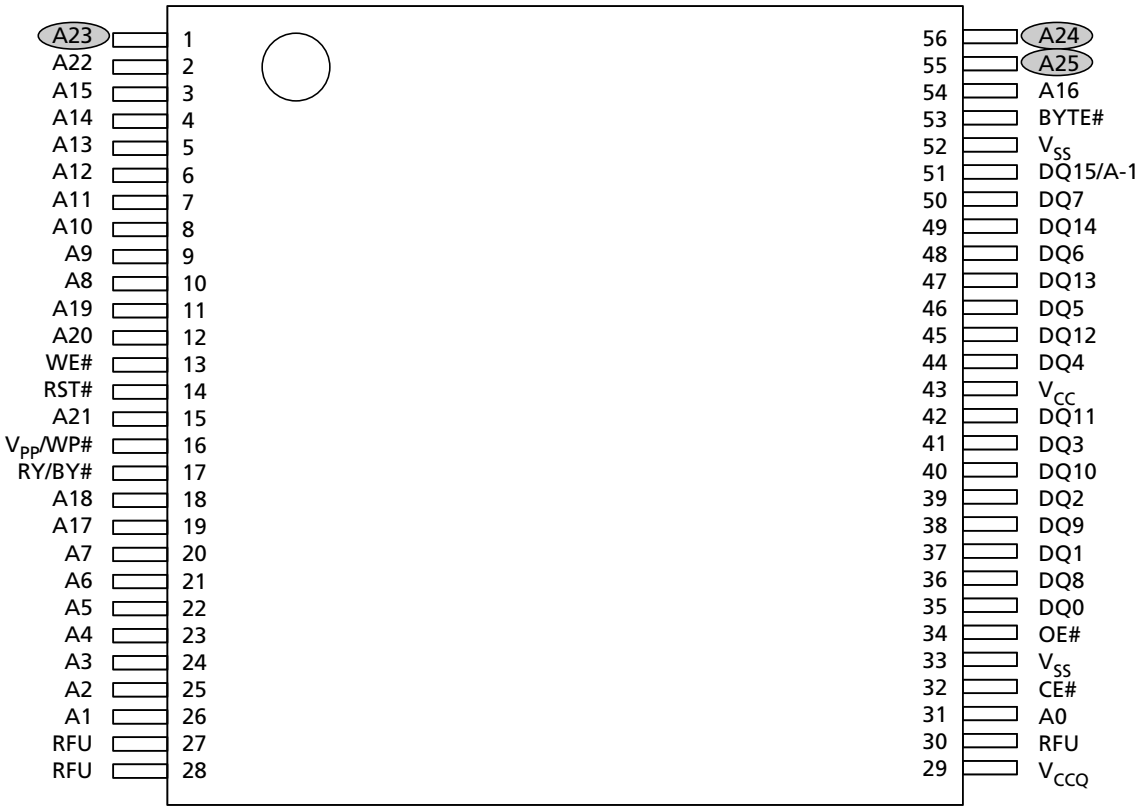
Figure 2: 2Gb Configuration



Note: 1. A[26] = V_{IH} selects the upper die; A[26] = V_{IL} selects the lower die.

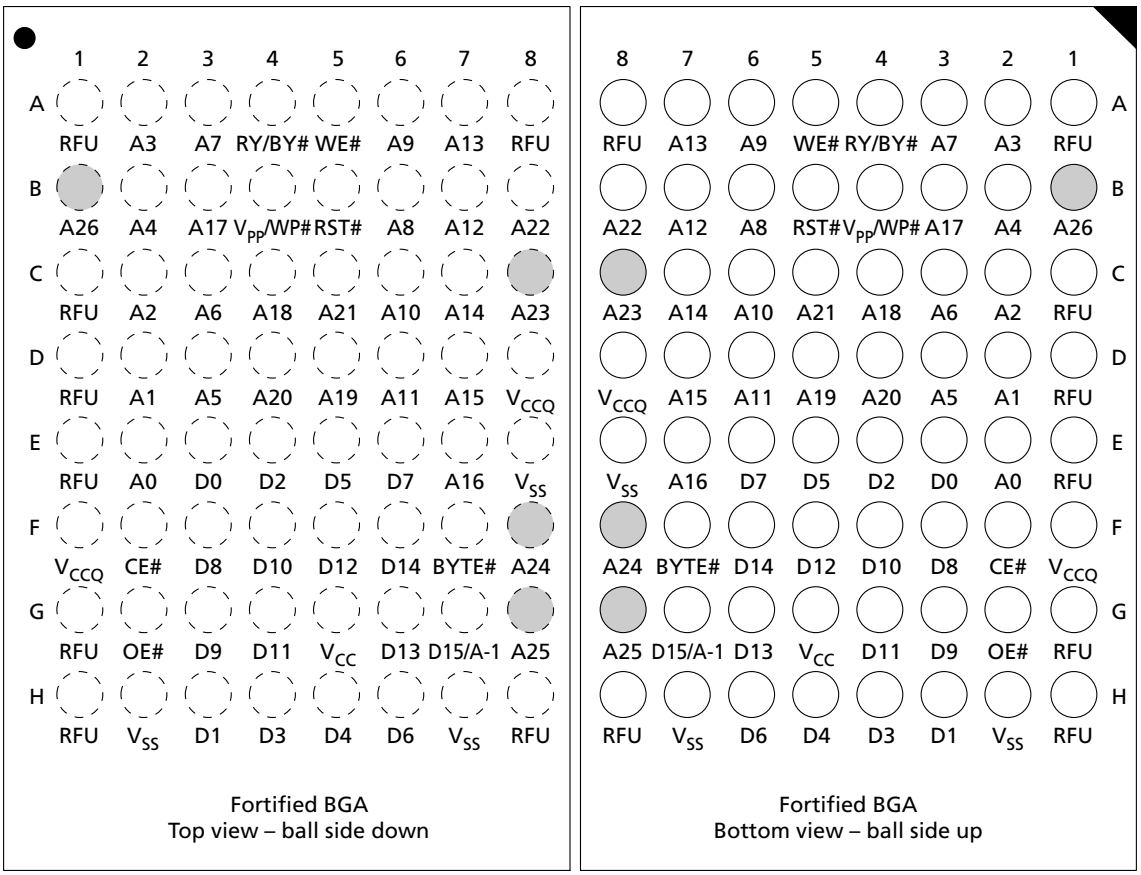
Signal Assignments

Figure 3: 56-Pin TSOP (Top View)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb and above; otherwise, it is RFU.

Figure 4: 64-Ball Fortified BGA



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb and above; otherwise, it is RFU.
5. A26 is valid for 2Gb only; otherwise it is RFU.

Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 4: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are at HIGH-Z.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides WRITE PROTECT function and V_{PPH} function. These functions protect the lowest or highest block and enable the device to enter unlock bypass mode, respectively. (Refer to Hardware Protection and Bypass Operations for details.)
BYTE#	Input	**Byte/word organization select:** Switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode.
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). See RESET AC Specifications for more details.
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During WRITE operations, these bits are not used. When reading the status register, these bits should be ignored.
DQ15/A-1	I/O	**Data I/O or address input:** When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Except where stated explicitly otherwise, DQ15 = data I/O (x16 mode); A-1 = address input (x8 mode).
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z (see RESET AC Specifications for more details). The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one (or more) of the devices is (are) busy. A 10K Ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.

Table 4: Signal Descriptions (Continued)

Name	Type	Description
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when V_{CC} <= V_{LKO}. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics).
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

Memory Organization

Memory Configuration

The main memory array is divided into 128KB or 64KW uniform blocks.

Memory Map – 256Mb–2Gb Density

Table 5: Blocks[2047:0]

Block	Block Size	Address Range (x8)		Block Size	Address Range (x16)	
		Start	End		Start	End
2047	128KB	FFE 0000h	FFF FFFFh	64KW	7FF 0000h	7FF FFFFh
⋮		⋮	⋮		⋮	⋮
1023		7FE 0000h	7FF FFFFh		3FF 0000h	3FF FFFFh
⋮		⋮	⋮		⋮	⋮
511		3FE 0000h	3FF FFFFh		1FF 0000h	1FF FFFFh
⋮		⋮	⋮		⋮	⋮
255		1FE 0000h	1FF FFFFh		0FF 0000h	0FF FFFFh
⋮		⋮	⋮		⋮	⋮
127		0FE 0000h	0FF FFFFh		07F 0000h	07F FFFFh
⋮		⋮	⋮		⋮	⋮
63		07E 0000h	07F FFFFh		03F 0000h	03F FFFFh
⋮		⋮	⋮		⋮	⋮
0		000 0000h	001 FFFFh		000 0000h	000 FFFFh

Note: 1. 256Mb device = blocks 0–255; 512Mb device = blocks 0–511; 1Gb device = blocks 0–1023; 2Gb device = blocks 0–2047, including upper and lower die.

Bus Operations

Table 6: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	8-Bit Mode			16-Bit Mode	
						A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Cell address	High-Z	Data output	Cell address	Data output
WRITE	L	H	L	H	H[3]	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	H	H	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 3ns on CE#, WE#, and RST# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# is LOW, then the highest or the lowest block remains protected, depending on line item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 16 words (32 bytes) and is addressed by address inputs A[3:0] in x16 bus mode and A[3:0] plus DQ15/A-1 in x8 bus mode. The extended memory blocks and CFI area do not support page read mode.

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation. (See AC Characteristics for timing requirement details.)

Standby

Driving CE# HIGH in read mode causes the device to enter standby, and data I/Os to be High-Z. To reduce the supply current to the standby supply current (I_{CC2}), CE# must be held within V_{CC} ±0.3V. (See DC Characteristics.)

During PROGRAM or ERASE operations the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

Registers

Status Register

Table 7: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	

Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE or BLANK CHECK operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.

6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.

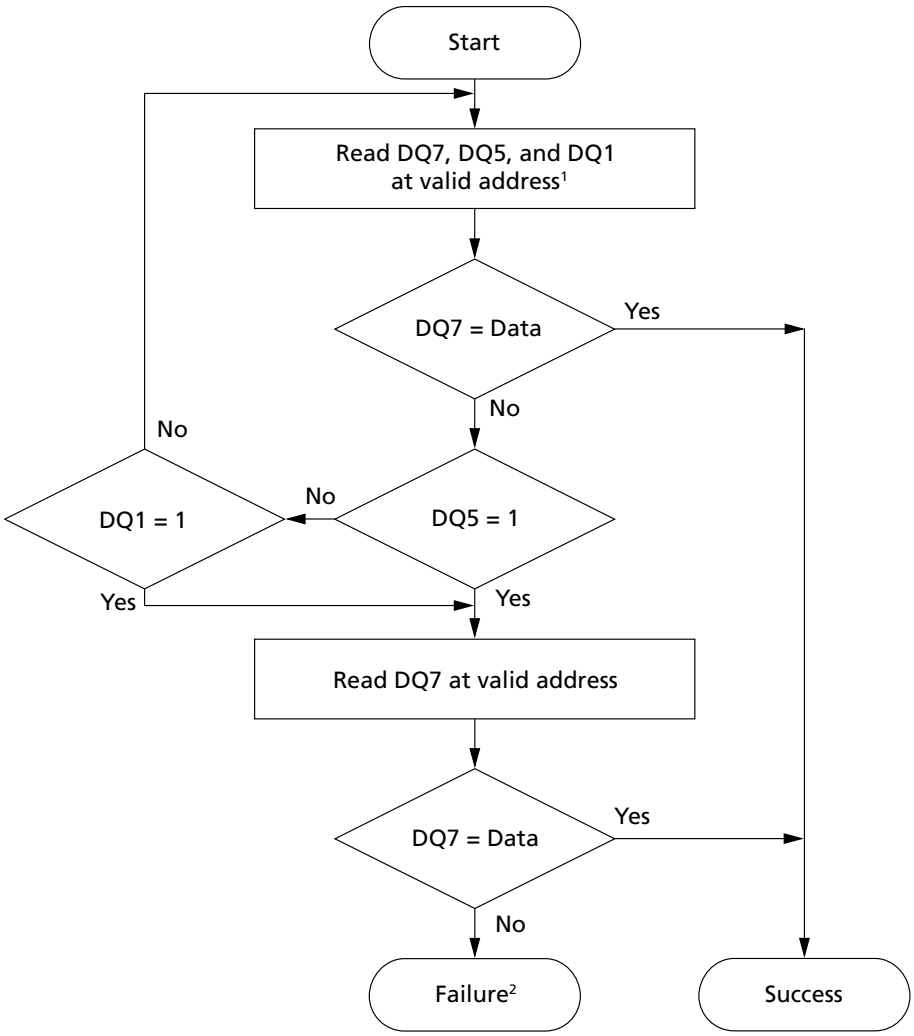
Table 8: Operations and Corresponding Bit Settings

Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0	2
BLANK CHECK	Any address	1	Toggle	0	–	–	0	0	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
PROGRAM SUSPEND	Programming block	Invalid operation						High-Z	
	Nonprogramming block	Outputs memory array data as if in read mode						High-Z	
ERASE SUSPEND	Erasing block	1	No Toggle	0	–	Toggle	–	High-Z	
	Non-erasing block	Outputs memory array data as if in read mode						High-Z	
PROGRAM during ERASE SUSPEND	Erasing block	DQ7#	Toggle	0	–	Toggle	–	0	2
	Non-erasing block	DQ7#	Toggle	0	–	No Toggle	–	0	2
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	High-Z	
PROGRAM Error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	2
ERASE Error	Any address	0	Toggle	1	1	Toggle	–	High-Z	
BLANK CHECK Error	Any address	1	Toggle	1	1	Toggle	–	High-Z	

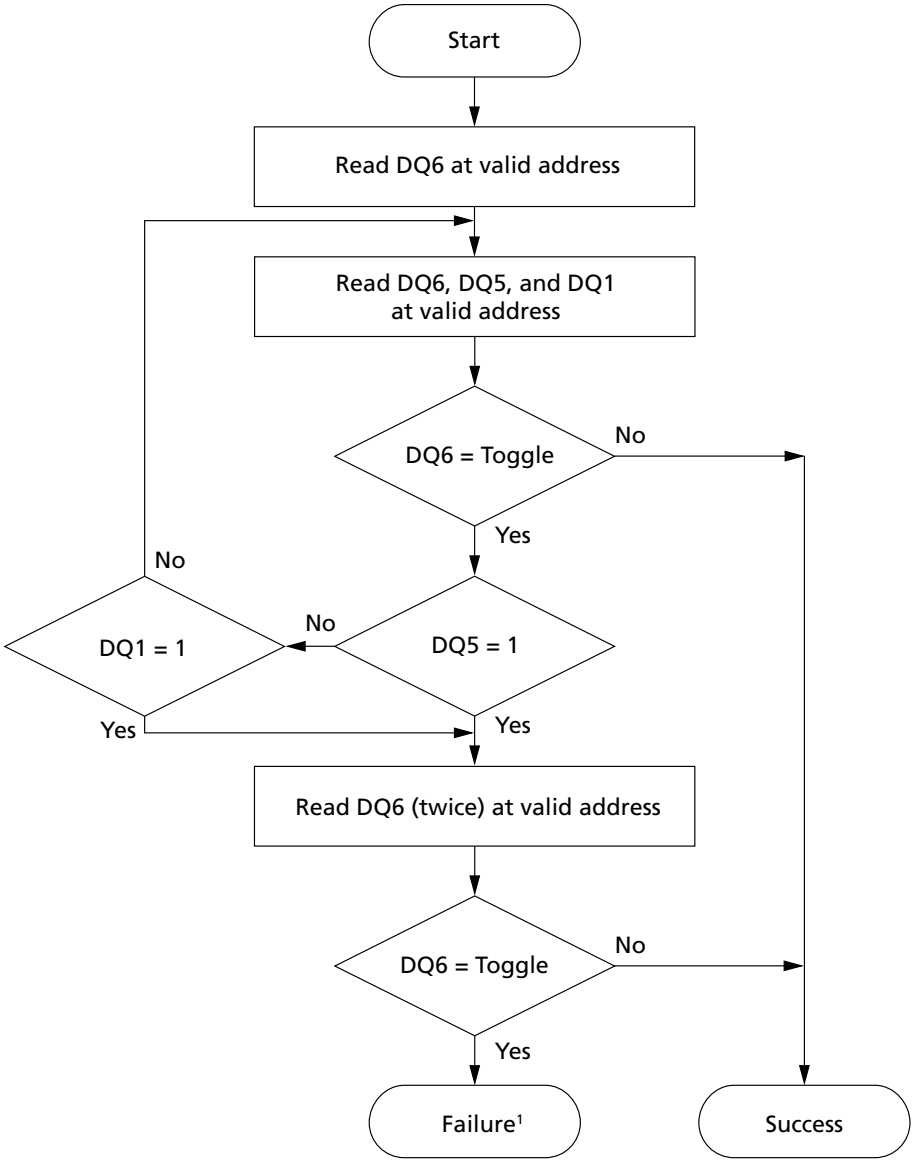
Notes: 1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.

Figure 5: Data Polling Flowchart



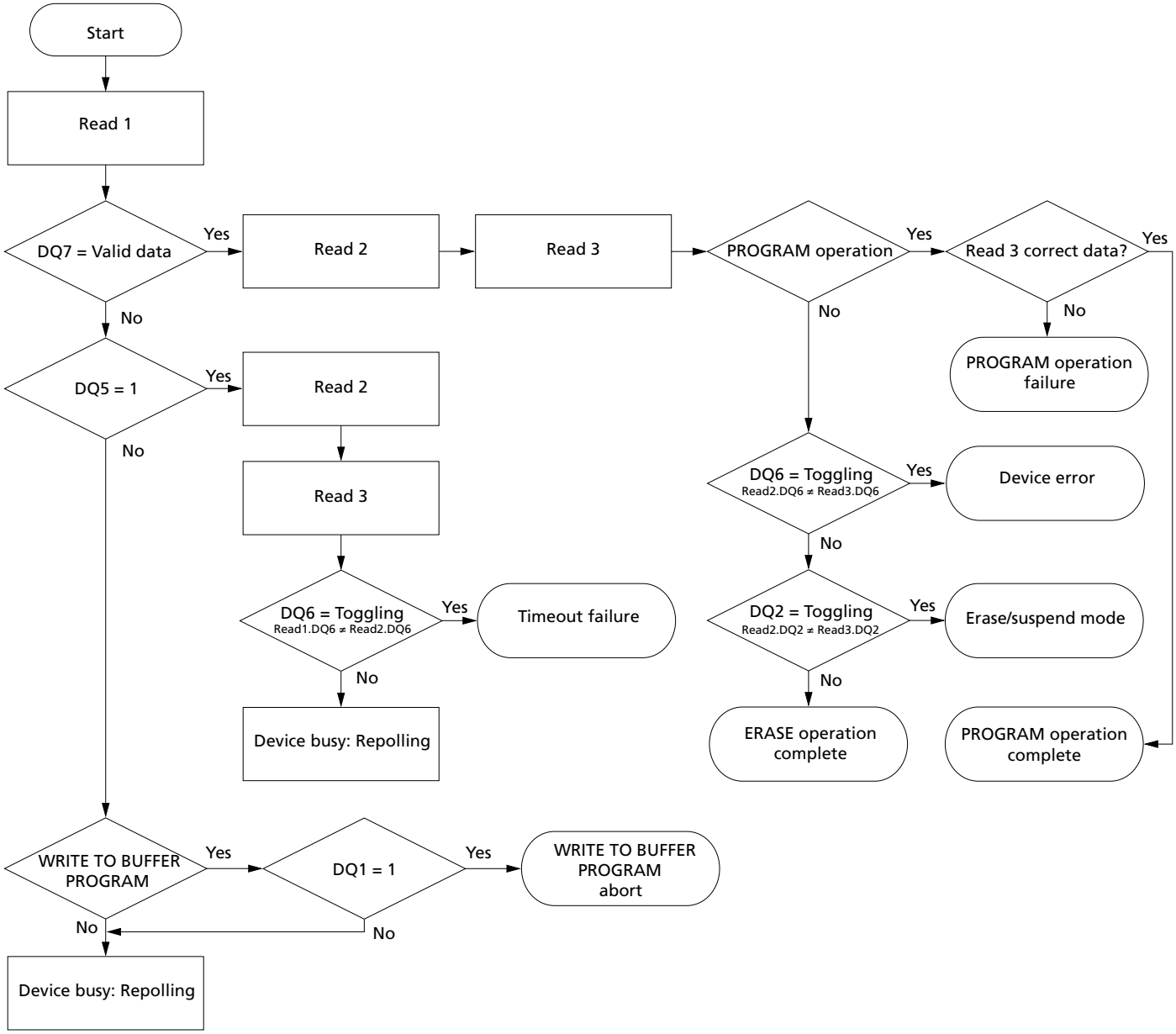
Notes:
1. Valid address is the address being programmed or an address within the block being erased or on which a BLANK CHECK operation has been executed.
2. The data polling process does not support the BLANK CHECK operation. The process represented in the Toggle Bit Flowchart figure can provide information on the BLANK CHECK operation.
3. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 6: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 7: Status Register Polling Flowchart



Lock Register

Table 9: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	

Notes:
1. The lock register is a 16-bit, one-time programmable register. DQ[15:3] are reserved and are set to a default value of 1.
2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Table 10: Block Protection Status

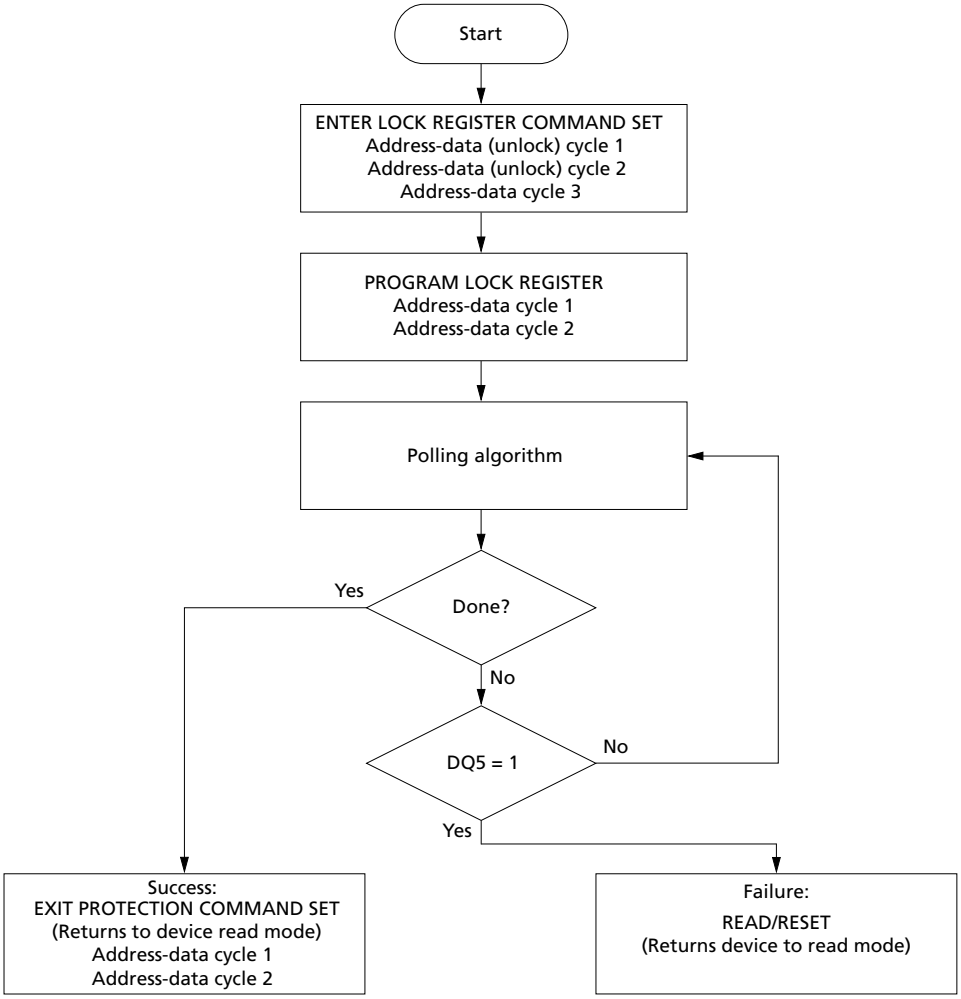
Nonvolatile Protection Bit Lock Bit[1]	Nonvolatile Protection Bit[2]	Volatile Protection Bit[3]	Block Protection Status	Block Protection Status
1	1	1	00h	Block unprotected; nonvolatile protection bit changeable.
1	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit changeable.
1	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit changeable.
1	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit changeable.
0	1	1	00h	Block unprotected; nonvolatile protection bit unchangeable.
0	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit unchangeable.
0	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit unchangeable.

Table 10: Block Protection Status (Continued)

Nonvolatile Protection Bit Lock Bit[1]	Nonvolatile Protection Bit[2]	Volatile Protection Bit[3]	Block Protection Status	Block Protection Status
0	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit unchangeable.

Notes:
1. Nonvolatile protection bit lock bit: when cleared to 1, all nonvolatile protection bits are unlocked; when set to 0, all nonvolatile protection bits are locked.
2. Block nonvolatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.
3. Block volatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.

Figure 8: Lock Register Program Flowchart



Notes: 1. Each lock register bit can be programmed only once.
2. See the Block Protection Command Definitions table for address-data cycle details.

Standard Command Definitions – Address-Data Cycles

Table 11: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	x8	X	F0											
		AAA	AA	555	55	X	F0							
	x16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	x8	AA	98											
	x16	55												
AUTO SELECT (90h)	x8	AAA	AA	555	55	AAA	90	Note 2	Note 2					2, 3, 4
	x16	555		2AA		555								
BYPASS Operations														
UNLOCK BYPASS (20h)	x8	AAA	AA	555	55	AAA	20							
	x16	555		2AA		555								
UNLOCK BYPASS RESET (90h/00h)	x8	X	90	X	00									
	x16													
PROGRAM Operations														
PROGRAM (A0h)	x8	AAA	AA	555	55	AAA	A0	PA	PD					
	x16	555		2AA		555								
UNLOCK BYPASS PROGRAM (A0h)	x8	X	A0	PA	PD									5
	x16													
WRITE TO BUFFER PROGRAM (25h)	x8	AAA	AA	555	55	BAd	25	BAd	N	PA	PD			6, 7, 8
	x16	555		2AA										
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	x8	BAd	25	BAd	N	PA	PD							5
	x16													
WRITE TO BUFFER PROGRAM CONFIRM (29h)	x8	BAd	29											
	x16													
BUFFERED PROGRAM ABORT and RESET (F0h)	x8	AAA	AA	555	55	AAA	F0							
	x16	555		2AA		555								
PROGRAM SUSPEND (B0h)	x8	X	B0											
	x16													
PROGRAM RESUME (30h)	x8	X	30											
	x16													
ERASE Operations														

Table 11: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
CHIP ERASE (80/10h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10	
	x16	555		2AA		555		555		2AA		555		
UNLOCK BYPASS CHIP ERASE (80/10h)	x8	X	80	X	10									5
	x16													
BLOCK ERASE (80/30h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30	9
	x16	555		2AA		555		555		2AA				
UNLOCK BYPASS BLOCK ERASE (80/30h)	x8	X	80	BAd	30									5
	x16													
ERASE SUSPEND (B0h)	x8	X	B0											
	x16													
ERASE RESUME (30h)	x8	X	30											
	x16													
BLANK CHECK Operations														
BLANK CHECK SETUP (EB/76h)	x8	AAA	AA	555	55	BAd	EB	BAd	76	BAd	00	BAd	00	
	x16	555		2AA										
BLANK CHECK CONFIRM and READ (29h)	x8	BAd	29	BAd	Note 2									2
	x16													

Notes:
1. A = Address; D = Data; X = "Don't Care;" BAd = Any address in the block; N = Number of bytes to be programmed; PA = Program address; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode. For the 2Gb device, the set-up command must be issued for each selected die.
2. These cells represent READ cycles (versus WRITE cycles for the others).
3. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
4. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
5. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
6. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
7. WRITE TO BUFFER PROGRAM operation: maximum cycles = 261 (x8) and 517 (x16). UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 259 (x8), 515 (x16). WRITE TO BUFFER PROGRAM operation: N + 1 = bytes to be programmed; maximum buffer size = 256 bytes (x8) and 1024 bytes (x16).
8. For x8, A[MAX:7] address pins should remain unchanged while A[6:0] and A-1 pins are used to select a byte within the N + 1 byte page. For x16, A[MAX:9] address pins should remain unchanged while A[8:0] pins are used to select a word within the N+1 word page.
9. BLOCK ERASE address cycles can extend beyond six address-data cycles, depending on the number of blocks to erase.