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Numonyx™ StrataFlash® Embedded Memory (P33)

Datasheet

Product Features

- High performance:
  - 85 ns initial access
  - 52MHz with zero wait states, 17ns clock-to-data output synchronous-burst read mode
  - 25 ns asynchronous-page read mode
  - 4-, 8-, 16-, and continuous-word burst mode
  - Buffered Enhanced Factory Programming (BEFP) at 5 µs/byte (Typ)
  - 3.0 V buffered programming at 7 µs/byte (Typ)
- Architecture:
  - Multi-Level Cell Technology: Highest Density at Lowest Cost
  - Asymmetrically-blocked architecture
  - Four 32-KByte parameter blocks: top or bottom configuration
  - 128-KByte main blocks
- Voltage and Power:
  - V_{CC} (core) voltage: 2.3 V – 3.6 V
  - V_{CCQ} (I/O) voltage: 2.3 V – 3.6 V
  - Standby current: 35µA (Typ) for 64-Mbit
  - 4-Word synchronous read current: 16 mA (Typ) at 52MHz
- Quality and Reliability
  - Operating temperature: –40 °C to +85 °C
  - Minimum 100,000 erase cycles per block
  - ETOX™ VIII process technology
- Security:
  - One-Time Programmable Registers:
    - 64 unique factory device identifier bits
    - 2112 user-programmable OTP bits
  - Selectable OTP space in Main Array:
    - Four pre-defined 128-KByte blocks (top or bottom configuration).
    - Up to Full Array OTP Lockout
  - Absolute write protection: $V_{PP} = V_{SS}$
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down capability
- Software:
  - 20 µs (Typ) program suspend
  - 20 µs (Typ) erase suspend
  - Numonyx™ Flash Data Integrator optimized
  - Basic Command Set and Extended Command Set compatible
  - Common Flash Interface capable
- Density and Packaging
  - 56-Lead TSOP package (64, 128, 256, 512-Mbit)
  - 64-Ball Numonyx™ Easy BGA package (64, 128, 256, 512-Mbit)
  - Numonyx™ QUAD+ SCSP (64, 128, 256, 512-Mbit)
  - 16-bit wide data bus

314749-05
November 2007

Contents

Revision History

Date	Revision	Description
April 2006	001	Initial release
August 2006	002	Product release
May 2007	003	Update and provide general document clarifications Revise ICCR values for Page-Mode Read Added note for V_{ccq} change on TSOP burst operation Added TSOP Burst AC Read specification Updated new revision of CFI Updated Flowcharts Updated description of Burst Operation Document changes regarding burst operation with the TSOP package.
October 2007	004	Updated for 65nm lithography. Define W602 Erase to Suspend.
November 2007	05	Applied Numonyx template and datasheet organization.

1.0 Introduction

This document provides information about the Numonyx™ StrataFlash® Embedded Memory (P33) device and describes its features, operation, and specifications.

P33 is the latest generation of Numonyx™ StrataFlash® memory devices. Offered in 64-Mbit up through 512-Mbit densities, the P33 flash memory device brings reliable, two-bit-per-cell storage technology to the embedded flash market segment. Benefits include more density in less space, high-speed interface, lowest cost-per-bit NOR device, and support for code and data storage. Features include high-performance synchronous-burst read mode, fast asynchronous access times, low power, flexible security options, and three industry standard package choices.

P33 product family is manufactured using Intel* 130 nm ETOX™ VIII process technology. The P33 product family is also planned on the Numonyx™ 65nm process lithography. 65nm AC timing changes are noted in this datasheet, and should be taken into account for all new designs

1.1 Nomenclature

3.0 V :	V_{CC} (core) and V_{CCQ} (I/O) voltage range of 2.3 V – 3.6 V
9.0 V :	V_{PP} voltage range of 8.5 V – 9.5 V
Block :	A group of bits, bytes, or words within the flash memory array that erase simultaneously. The Numonyx™ StrataFlash® Embedded Memory (P33) has two block sizes: 32 KByte and 128 KByte.
Main block :	An array block that is usually used to store code and/or data. Main blocks are larger than parameter blocks.
Parameter block :	An array block that may be used to store frequently changing data or small system parameters that traditionally would be stored in EEPROM.
Top parameter device :	A device with its parameter blocks located at the highest physical address of its memory map.
Bottom parameter device :	A device with its parameter blocks located at the lowest physical address of its memory map.

1.2 Acronyms

BEFP :	Buffer Enhanced Factory Programming
CUI :	Command User Interface
MLC :	Multi-Level Cell
OTP :	One-Time Programmable
PLR :	Protection Lock Register
PR :	Protection Register
RCR :	Read Configuration Register
RFU :	Reserved for Future Use
SR :	Status Register
WSM :	Write State Machine

1.3 Conventions

VCC :	Signal or voltage connection
V_{CC} :	Signal or voltage level
0h :	Hexadecimal number suffix
0b :	Binary number suffix
SR[4] :	Denotes an individual register bit.
A[15:0] :	Denotes a group of similarly named signals, such as address or data bus.
A5 :	Denotes one element of a signal group membership, such as an individual address bit.
Bit :	Single Binary unit
Byte :	Eight bits
Word :	Two bytes, or sixteen bits
Kbit :	1024 bits
KByte :	1024 bytes
KWord :	1024 words
Mbit :	1,048,576 bits
MByte :	1,048,576 bytes
MWord :	1,048,576 words
K	1,000
M	1,000,000

2.0 Functional Overview

This section provides an overview of the features and capabilities of the Numonyx™ StrataFlash® Embedded Memory (P33) device.

The Kearny Family Flash memory provides density upgrades from 64-Mbit through 512-Mbit. This family of devices provides high performance at low voltage on a 16-bit data bus. Individually erasable memory blocks are sized for optimum code and data storage.

Upon initial power up or return from reset, the device defaults to asynchronous page-mode read. Configuring the RCR enables synchronous burst-mode reads. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides an easy CPU-to-flash memory synchronization.

In addition to the enhanced architecture and interface, the device incorporates technology that enables fast factory program and erase operations. Designed for low-voltage systems, the Kearny Family Flash memory supports read operations with V_{CC} at 3.0V, and erase and program operations with V_{PP} at 3.0V or 9.0V. BEFP provides the fastest flash array programming performance with V_{PP} at 9.0V, which increases factory throughput. With V_{PP} at 3.0V, VCC and VPP can be tied together for a simple, ultra low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when $V_{PP} \leq V_{PPLK}$.

The CUI is the interface between the system processor and all internal operations of the device. An internal WSM automatically executes the algorithms and timings necessary for block erase and program. A Status Register indicates erase or program completion and any errors that may have occurred.

An industry-standard command sequence invokes program and erase automation. Each erase operation erases one block. The Erase Suspend feature allows system software to pause an erase cycle to read or program data in another block. Program Suspend allows system software to pause programming to read other locations. Data is programmed in word increments (16 bits).

The Kearny Family Flash memory protection register allows unique flash device identification that can be used to increase system security. The individual Block Lock feature provides zero-latency block locking and unlocking. In addition, the Kearny Family Flash memory may also pre-define main array space as OTP.

2.1 Virtual Chip Enable Description

The 512 Mbit Kearny Family Flash memory employs a Virtual Chip Enable which combines two 256-Mbit die with a common chip enable, F1-CE# for QUAD+ packages or CE# for Easy BGA packages (refer to Figure 10 and Figure 11 for additional details). Address A24 (QUAD+ package) or A25 (Easy BGA and TSOP package) is then used to select between the die pair with F1-CE# / CE# asserted, depending upon the package option used. When chip enable is asserted and QUAD+ A24 (Easy BGA A25) is low (V_{IL}), The lower parameter die is selected; when chip enable is asserted and QUAD+ A24 (Easy BGA A25) is high (V_{IH}), the upper parameter die is selected. Refer to Table 1, "Flash Die Virtual Chip Enable Truth Table for 512 Mbit QUAD+ Package" and Table 2, "Flash Die Virtual Chip Enable Truth Table for 512 Mbit TSOP / Easy BGA Package" for additional details.

Table 1: Flash Die Virtual Chip Enable Truth Table for 512 Mbit QUAD+ Package

Die Selected	F1-CE#	A24
Lower Param Die	L	L
Upper Param Die	L	H

Table 2: Flash Die Virtual Chip Enable Truth Table for 512 Mbit TSOP / Easy BGA Package

Die Selected	CE#	A25
Lower Param Die	L	L
Upper Param Die	L	H

3.0 Package Information

3.1 56-Lead TSOP

Figure 1: TSOP Mechanical Specifications

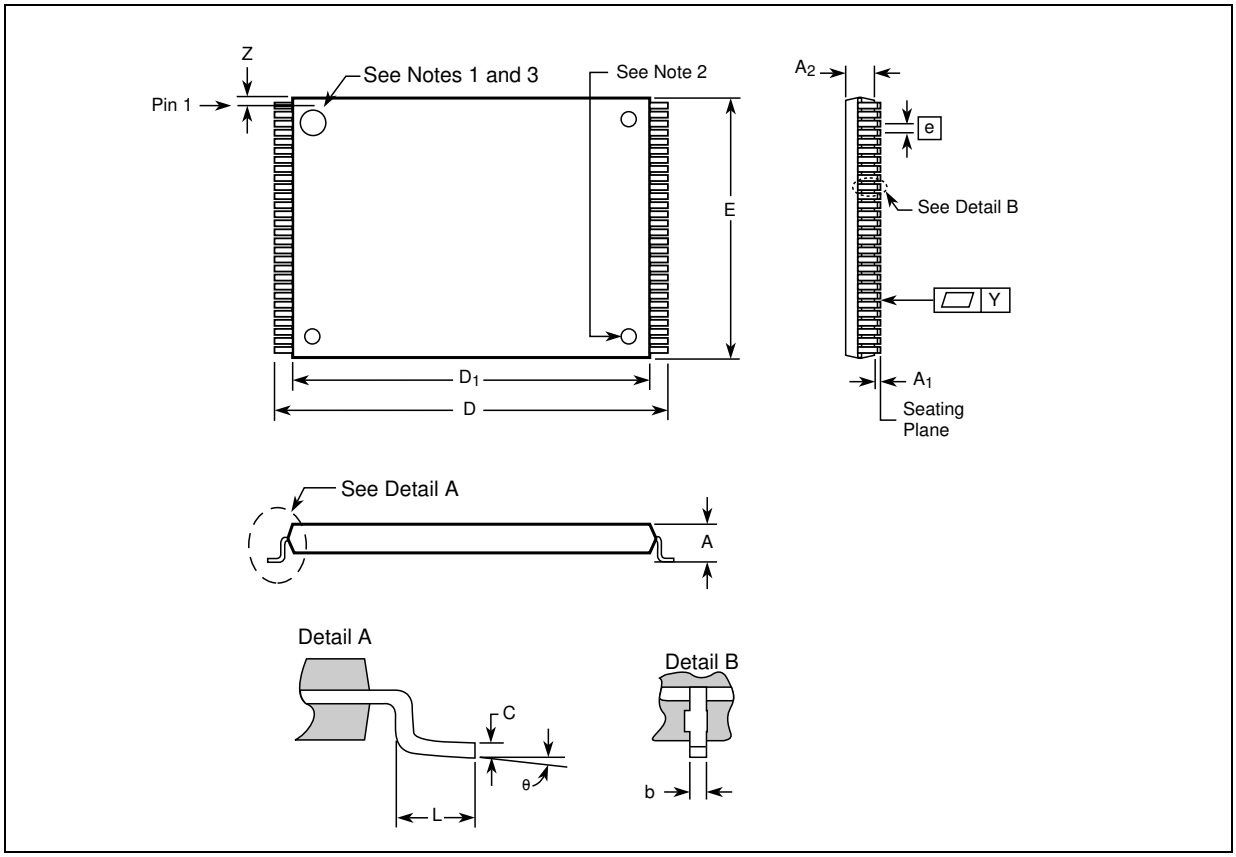


Table 3: TSOP Package Dimensions (Sheet 1 of 2)

Product Information	Symbol	Millimeters			Inches			Notes
		Min	Nom	Max	Min	Nom	Max	
Package Height	A	-	-	1.200	-	-	0.047	
Standoff	A_1	0.050	-	-	0.002	-	-	
Package Body Thickness	A_2	0.965	0.995	1.025	0.038	0.039	0.040	
Lead Width	b	0.100	0.150	0.200	0.004	0.006	0.008	
Lead Thickness	c	0.100	0.150	0.200	0.004	0.006	0.008	
Package Body Length	D_1	18.200	18.400	18.600	0.717	0.724	0.732	
Package Body Width	E	13.800	14.000	14.200	0.543	0.551	0.559	
Lead Pitch	e	-	0.500	-	-	0.0197	-	
Terminal Dimension	D	19.800	20.00	20.200	0.780	0.787	0.795	
Lead Tip Length	L	0.500	0.600	0.700	0.020	0.024	0.028	

Table 3: TSOP Package Dimensions (Sheet 2 of 2)

Product Information	Symbol	Millimeters			Inches			Notes
		Min	Nom	Max	Min	Nom	Max	
Lead Count	N	-	56	-	-	56	-	
Lead Tip Angle	ý	0°	3°	5°	0°	3°	5°	
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.004	
Lead to Package Offset	Z	0.150	0.250	0.350	0.006	0.010	0.014	

Notes:
1. One dimple on package denotes Pin 1.
2. If two dimples, then the larger dimple denotes Pin 1.
3. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.

3.2 64-Ball Easy BGA Package

Figure 2: 64-Mbit and 128-Mbit Easy BGA Mechanical Specifications

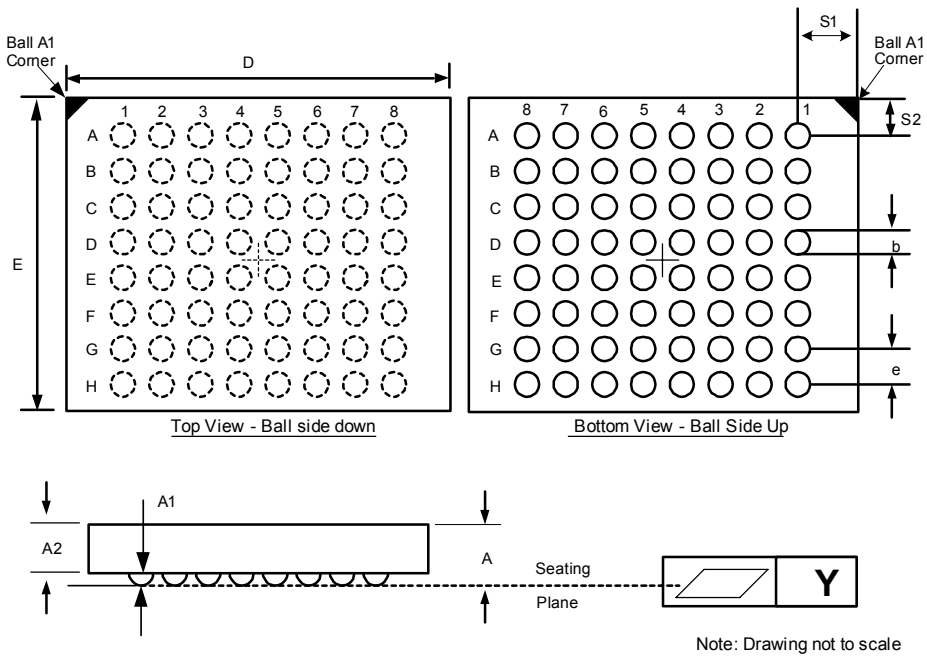


Table 4: 64-Mbit and 128-Mbit Easy BGA Package Dimensions (Sheet 1 of 2)

Product Information	Symbol	Millimeters			Inches			Notes
		Min	Nom	Max	Min	Nom	Max	
Package Height	A	-	-	1.200	-	-	0.0472	
Ball Height	A1	0.250	-	-	0.0098	-	-	
Package Body Thickness	A2	-	0.780	-	-	0.0307	-	

Table 4: 64-Mbit and 128-Mbit Easy BGA Package Dimensions (Sheet 2 of 2)

Product Information	Symbol	Millimeters			Inches			Notes
		Min	Nom	Max	Min	Nom	Max	
Ball (Lead) Width	b	0.330	0.430	0.530	0.0130	0.0169	0.0209	
Package Body Width	D	9.900	10.000	10.100	0.3898	0.3937	0.3976	1
Package Body Length	E	7.900	8.000	8.100	0.3110	0.3149	0.3189	1
Pitch	[e]	-	1.000	-	-	0.0394	-	
Ball (Lead) Count	N	-	64	-	-	64	-	
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039	
Corner to Ball A1 Distance Along D	S1	1.400	1.500	1.600	0.0551	0.0591	0.0630	1
Corner to Ball A1 Distance Along E	S2	0.400	0.500	0.600	0.0157	0.0197	0.0236	1

Notes:
1. Daisy Chain Evaluation Unit information is at Nu;monyx™ Flash Memory Packaging Technology http://developer.Numonyx.com/design/flash/packtech.

Figure 3: 256-Mbit and 512-Mbit Easy BGA Mechanical Specifications

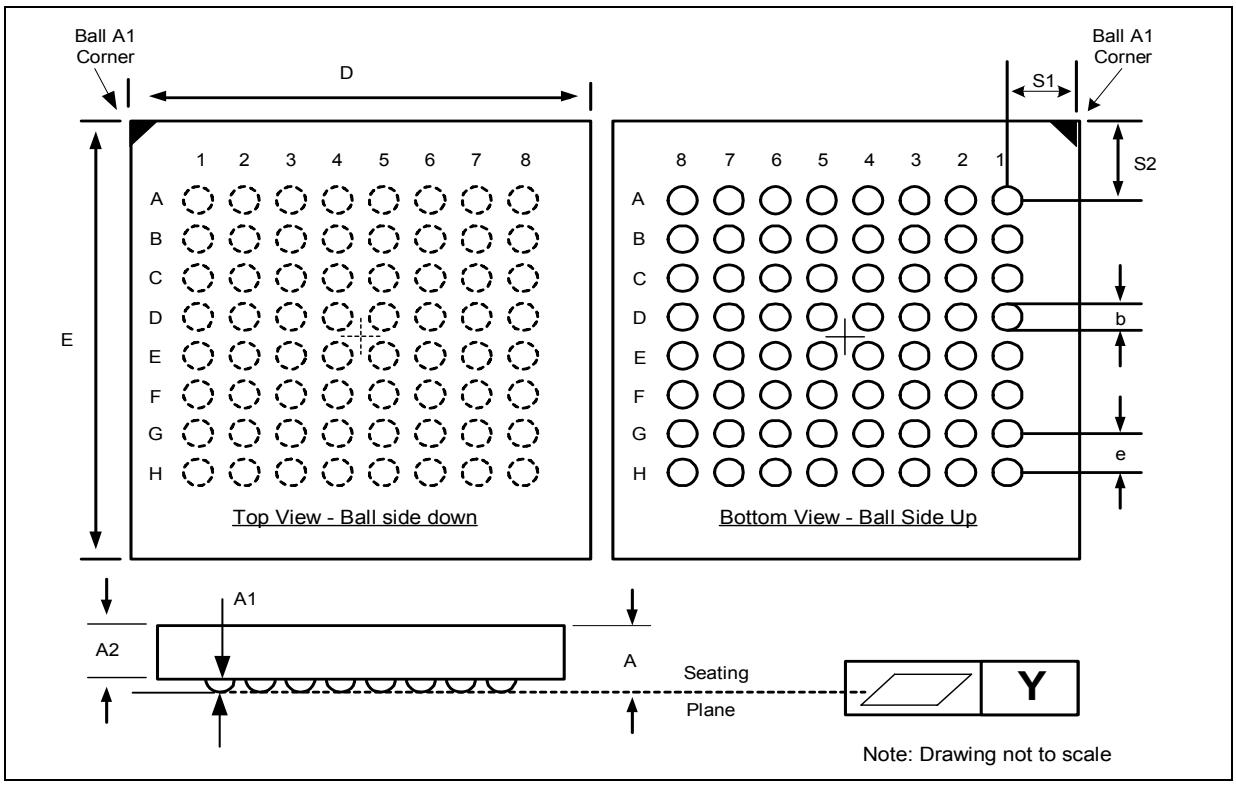


Table 5: 256-Mbit and 512-Mbit Easy BGA Package Dimensions

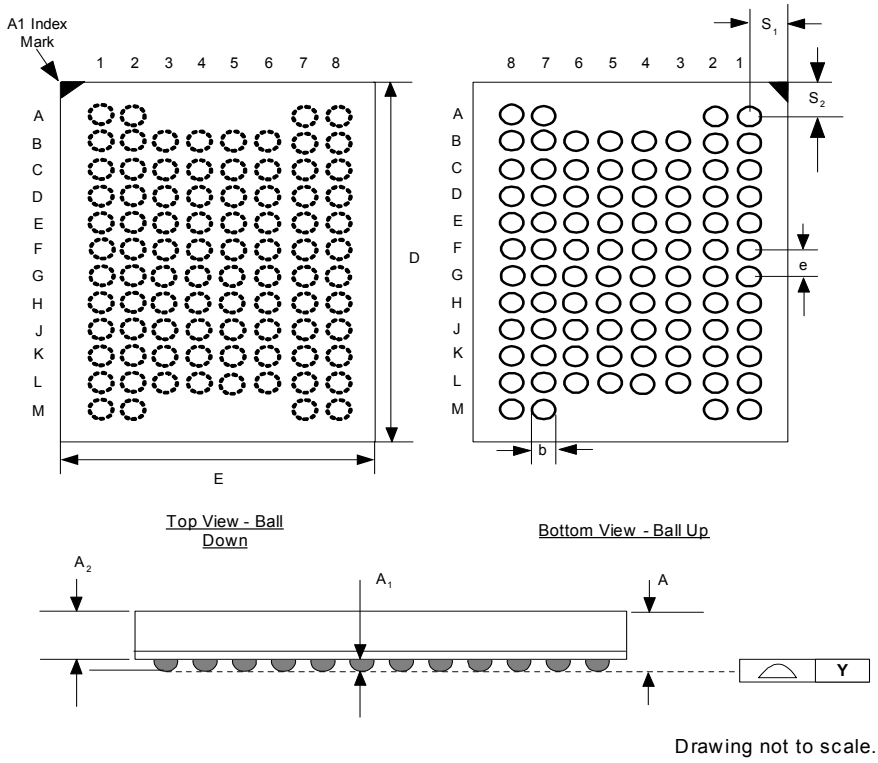
Product Information	Symbol	Millimeters			Inches			Notes
		Min	Nom	Max	Min	Nom	Max	
Package Height (256-Mbit)	A	-	-	1.200	-	-	0.0472	
Package Height (512-Mbit)	A	-	-	1.300	-	-	0.0512	
Ball Height	A1	0.250	-	-	0.0098	-	-	
Package Body Thickness (256-Mbit)	A2	-	0.780	-	-	0.0307	-	
Package Body Thickness (512-Mbit)	A2	-	0.910	-	-	0.0358	-	
Ball (Lead) Width	b	0.330	0.430	0.530	0.0130	0.0169	0.0209	
Package Body Width	D	9.900	10.000	10.100	0.3898	0.3937	0.3976	1
Package Body Length	E	12.900	13.000	13.100	0.5079	0.5118	0.5157	1
Pitch	[e]	-	1.000	-	-	0.0394	-	
Ball (Lead) Count	N	-	64	-	-	64	-	
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039	
Corner to Ball A1 Distance Along D	S1	1.400	1.500	1.600	0.0551	0.0591	0.0630	1
Corner to Ball A1 Distance Along E	S2	2.900	3.000	3.100	0.1142	0.1181	0.1220	1

Notes:

1. Daisy Chain Evaluation Unit information is at Numonyx™ Flash Memory Packaging Technology http://developer.numonyx.com/design/flash/packtech.

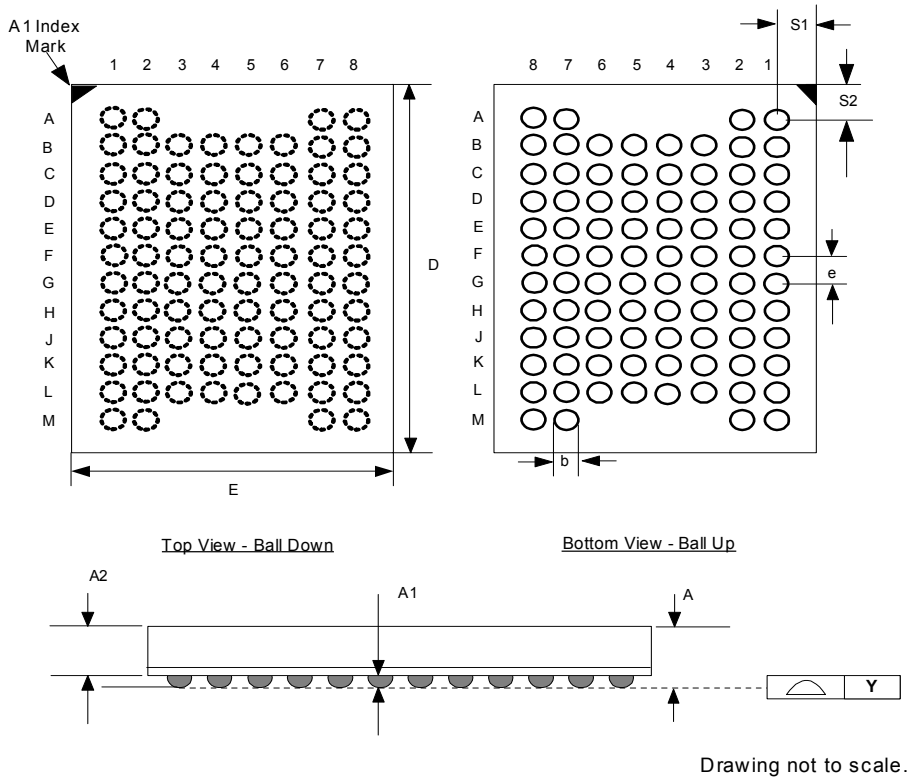
3.3 QUAD+ SCSP Packages

Figure 4: 64/128-Mbit, 88-ball (80 active) QUAD+ SCSP Specifications (8x10x1.2 mm)



		Millimeters			Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
Package Height	A	-	-	1.200	-	-	0.0472
Ball Height	A1	0.200	-	-	0.0079	-	-
Package Body Thickness	A2	-	0.860	-	-	0.0339	-
Ball (Lead) Width	b	0.325	0.375	0.425	0.0128	0.0148	0.0167
Package Body Width	D	9.900	10.000	10.100	0.3898	0.3937	0.3976
Package Body Length	E	7.900	8.000	8.100	0.3110	0.3150	0.3189
Pitch	e	-	0.800	-	-	0.0315	-
Ball (Lead) Count	N	-	88	-	-	88	-
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300	0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700	0.0197	0.0236	0.0276

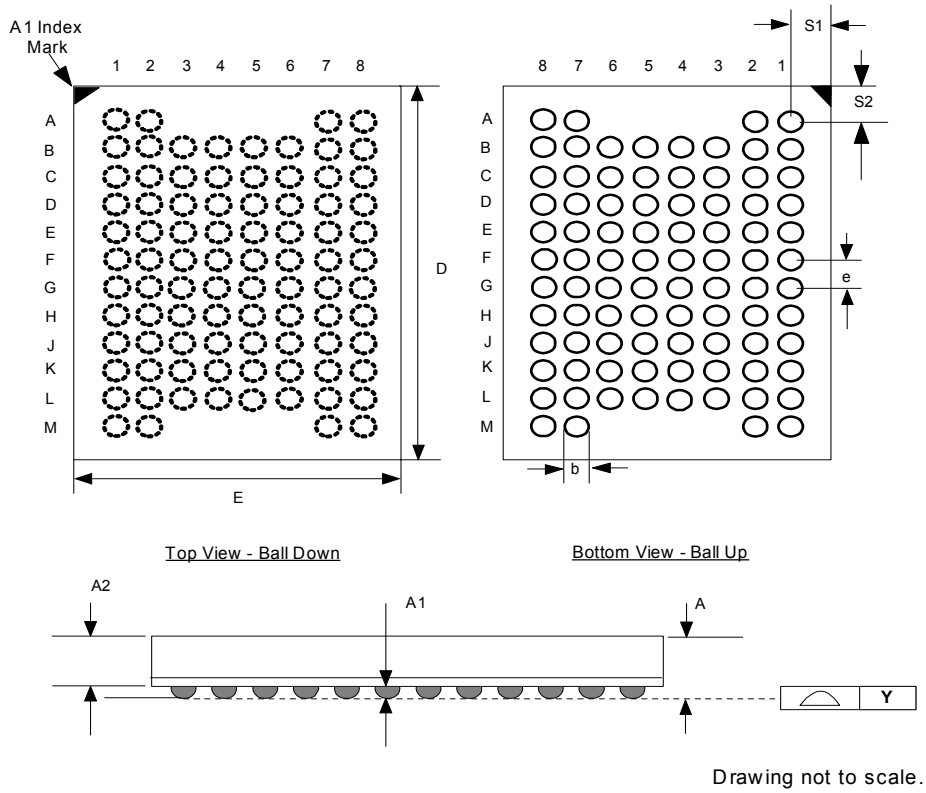
Figure 5: 256-Mbit, 88-ball (80 active) QUAD+ SCSP Specifications (8x11x1.0 mm)



Note: Dimensions A1, A2, and b are preliminary

		Millimeters			Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
Package Height	A	-	-	1.000	-	-	0.0394
Ball Height	A1	0.117	-	-	0.0046	-	-
Package Body Thickness	A2	-	0.740	-	-	0.0291	-
Ball (Lead) Width	b	0.300	0.350	0.400	0.0118	0.0138	0.0157
Package Body Length	D	10.900	11.00	11.100	0.4291	0.4331	0.4370
Package Body Width	E	7.900	8.00	8.100	0.3110	0.3150	0.3189
Pitch	e	-	0.80	-	-	0.0315	-
Ball (Lead) Count	N	-	88	-	-	88	-
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300	0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	1.000	1.100	1.200	0.0394	0.0433	0.0472

Figure 6: 512-Mbit, 88-ball (80 active) QUAD+ SCSP Specifications (8x11x1.2 mm)



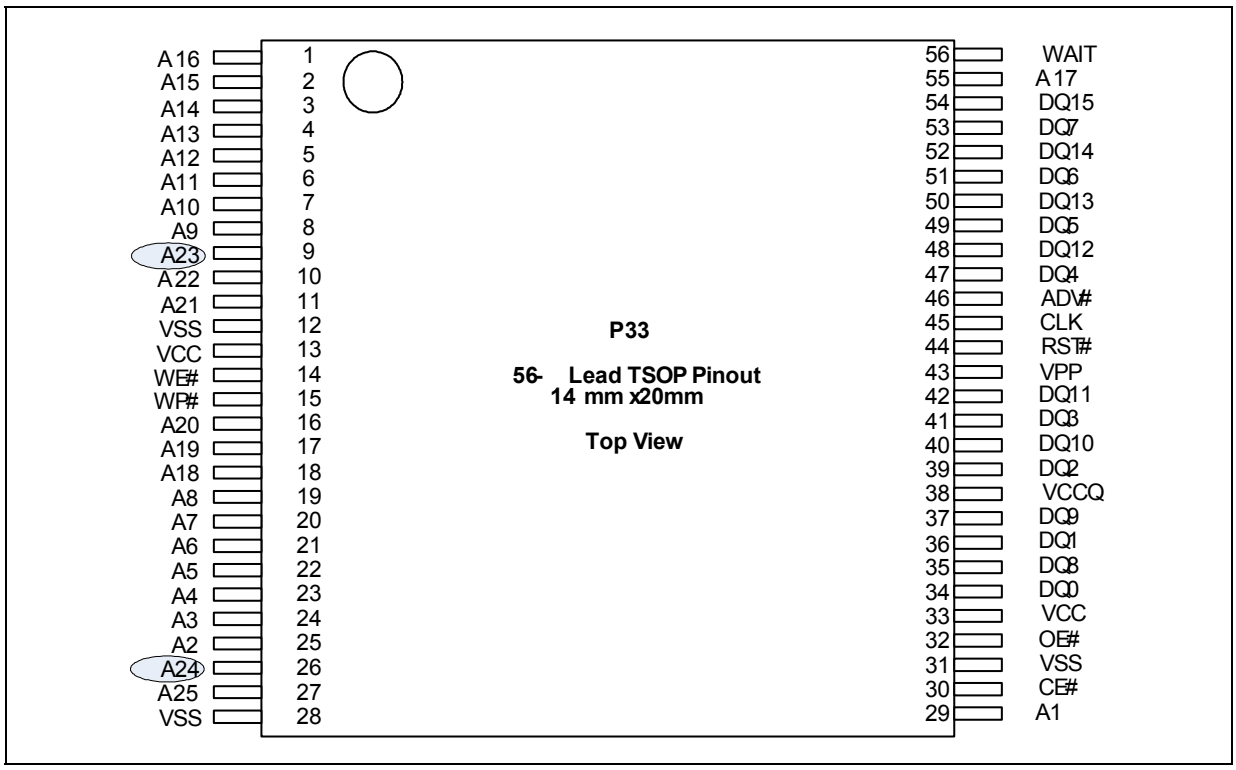
Drawing not to scale.

		Millimeters			Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
Package Height	A	-	-	1.200	-	-	0.0472
Ball Height	A1	0.200	-	-	0.0079	-	-
Package Body Thickness	A2	-	0.860	-	-	0.0339	-
Ball (Lead) Width	b	0.325	0.375	0.425	0.0128	0.0148	0.0167
Package Body Length	D	10.900	11.000	11.100	0.4291	0.4331	0.4370
Package Body Width	E	7.900	8.000	8.100	0.3110	0.3150	0.3189
Pitch	e	-	0.800	-	-	0.0315	-
Ball (Lead) Count	N	-	88	-	-	88	-
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300	0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	1.000	1.100	1.200	0.0394	0.0433	0.0472

4.0 Ballout and Signal Descriptions

4.1 Signal Ballout

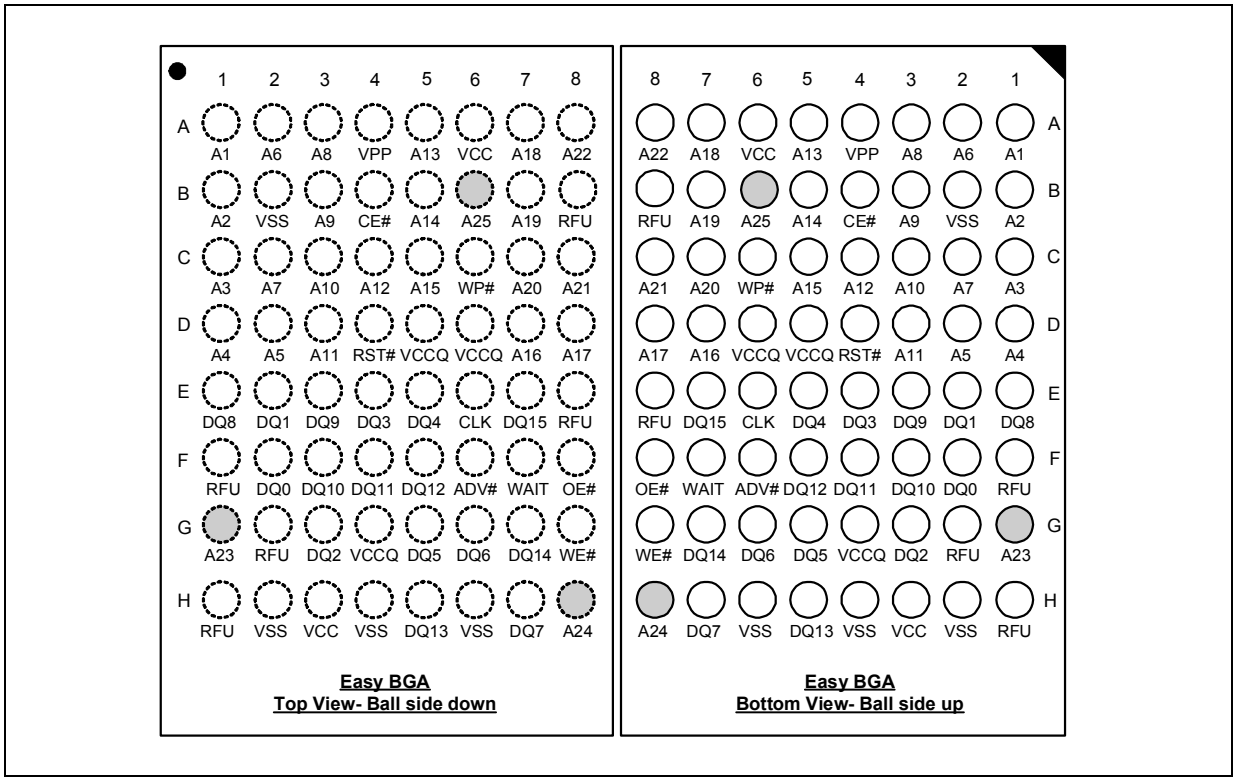
Figure 7: 56-Lead TSOP Pinout (64/128/256/512-Mbit)



Notes:

1. A1 is the least significant address bit.
2. A23 is valid for 128-Mbit densities and above; otherwise, it is a no connect (NC).
3. A24 is valid for 256-Mbit densities and above; otherwise, it is a no connect (NC).
4. A25 is valid for 512-Mbit densities; otherwise, it is a no connect (NC).
5. Please refer to the latest specification update for synchronous read operation on the TSOP package. The synchronous read input signals (i.e. ADV# and CLK) should be tied off to support asynchronous reads otherwise. See Section 4.2, "Signal Descriptions" on page 19. for additional information.

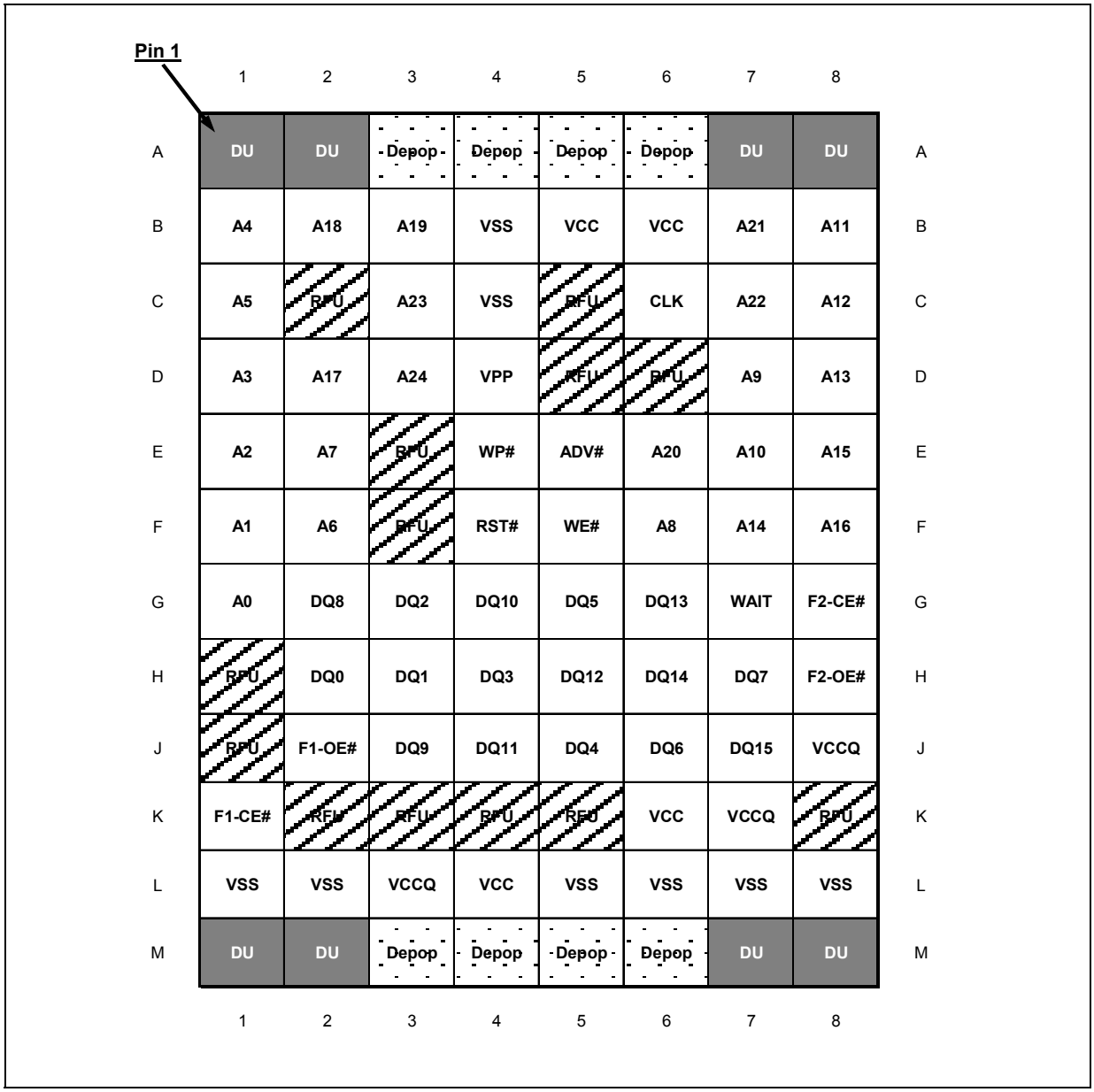
Figure 8: 64-Ball Easy BGA Ballout (64/128/256/512-Mbit)



Notes:

1. A1 is the least significant address bit.
2. A23 is valid for 128-Mbit densities and above; otherwise, it is a no connect.
3. A24 is valid for 256-Mbit densities and above; otherwise, it is a no connect.
4. A25 is valid for 512-Mbit densities; otherwise, it is a no connect.

Figure 9: 88-Ball (80-Active Ball) QUAD+ SCSP Ballout



Notes:
1. A22 is valid for 128-Mbit densities and above; otherwise, it is a no connect.
2. A23 is valid for 256-Mbit densities and above; otherwise, it is a no connect.
3. A24 is valid for 512-Mbit densities and above; otherwise, it is a no connect.
4. F2-CE# and F2-OE# are no connects.

4.2 Signal Descriptions

This section has signal descriptions for the various Numonyx™ StrataFlash® Embedded Memory (P33) device packages.

Table 6: TSOP and Easy BGA Signal Descriptions

Symbol	Type	Name and Function
A[MAX:1]	Input	**ADDRESS INPUTS:** Device address inputs. 64-Mbit: A[22:1]; 128-Mbit: A[23:1]; 256-Mbit: A[24:1]; 512-Mbit: A[25:1]. Note: The virtual selection of the 256-Mbit "Top parameter" die in the dual-die 512-Mbit configuration is accomplished by setting A25 high (V_{IH}).
DQ[15:0]	Input/ Output	**DATA INPUT/OUTPUTS:** Inputs data and commands during write cycles; outputs data during memory, Status Register, Protection Register, and Read Configuration Register reads. Data balls float when the CE# or OE# are deasserted. Data is internally latched during writes.
ADV#	Input	**ADDRESS VALID:** Active low input. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. In asynchronous mode, the address is latched when ADV# going high or continuously flows through if ADV# is held low. WARNING: Designs not using ADV# must tie it to VSS to allow addresses to flow through.
CE#	Input	**CHIP ENABLE:** Active low input. CE# low selects the associated flash memory die. When asserted, flash internal control logic, input buffers, decoders, and sense amplifiers are active. When deasserted, the associated flash die is deselected, power is reduced to standby levels, data and WAIT outputs are placed in high-Z state. WARNING: All chip enables must be high when device is not in use.
CLK	Input	**CLOCK:** Synchronizes the device with the system's bus frequency in synchronous-read mode. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. WARNING: Designs not using CLK for synchronous read mode must tie it to VCCQ or VSS.
OE#	Input	**OUTPUT ENABLE:** Active low input. OE# low enables the device's output data buffers during read cycles. OE# high places the data outputs and WAIT in High-Z.
RST#	Input	**RESET:** Active low input. RST# resets internal automation and inhibits write operations. This provides data protection during power transitions. RST# high enables normal operation. Exit from reset places the device in asynchronous read array mode.
WAIT	Output	**WAIT:** Indicates data valid in synchronous array or non-array burst reads. RCR[10], (WT) determines its polarity when asserted. WAIT's active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is high-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, WAIT indicates invalid data when asserted and valid data when deasserted. • In asynchronous page mode, and all write modes, WAIT is deasserted.
WE#	Input	**WRITE ENABLE:** Active low input. WE# controls writes to the device. Address and data are latched on the rising edge of WE#.
WP#	Input	**WRITE PROTECT:** Active low input. WP# low enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the Unlock command. WP# high overrides the lock-down function enabling blocks to be erased or programmed using software commands.
VPP	Power/ Input	**Erase and Program Power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system program and erase operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as V_{PPL} min. V_{PP} must remain above V_{PPL} min to perform in-system flash modification. VPP may be 0 V during read operations. V_{PPH} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. VPP can be connected to 9 V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9 V may reduce block cycling capability.
VCC	Power	**Device Core Power Supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \le V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
VCCQ	Power	**Output Power Supply:** Output-driver source voltage.
VSS	Power	**Ground:** Connect to system ground. Do not float any VSS connection.
RFU	—	**Reserved for Future Use:** Reserved by Numonyx for future device functionality and enhancement. These should be treated in the same way as a Don't Use (DU) signal.
DU	—	**Don't Use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No Connect:** No internal connection; can be driven or floated.

Table 7: QUAD+ SCSP Signal Descriptions

Symbol	Type	Name and Function
A[MAX:0]	Input	**ADDRESS INPUTS:** Device address inputs. 64-Mbit: A[21:0]; 128-Mbit: A[22:0]; 256-Mbit: A[23:0]; 512-Mbit: A[24:0]. Note: The virtual selection of the 256-Mbit "Top parameter" die in the dual-die 512-Mbit configuration is accomplished by setting A24 high (V_{IH}).
DQ[15:0]	Input/ Output	**DATA INPUT/OUTPUTS:** Inputs data and commands during write cycles; outputs data during memory, Status Register, Protection Register, and Read Configuration Register reads. Data balls float when the CE# or OE# are deasserted. Data is internally latched during writes.
ADV#	Input	**ADDRESS VALID:** Active low input. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. In asynchronous mode, the address is latched when ADV# going high or continuously flows through if ADV# is held low. WARNING: Designs not using ADV# must tie it to VSS to allow addresses to flow through.
F1-CE#	Input	**FLASH CHIP ENABLE:** Active low input. CE# low selects the associated flash memory die. When asserted, flash internal control logic, input buffers, decoders, and sense amplifiers are active. When deasserted, the associated flash die is deselected, power is reduced to standby levels, data and WAIT outputs are placed in high-Z state. Note: F2-CE# is a NC for this part WARNING: All chip enables must be high when device is not in use.
CLK	Input	**CLOCK:** Synchronizes the device with the system's bus frequency in synchronous-read mode. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. WARNING: Designs not using CLK for synchronous read mode must tie it to VCCQ or VSS.
F1-OE#	Input	**OUTPUT ENABLE:** Active low input. OE# low enables the device's output data buffers during read cycles. OE# high places the data outputs and WAIT in High-Z. Note: F2-OE# is a NC for this part.
RST#	Input	**RESET:** Active low input. RST# resets internal automation and inhibits write operations. This provides data protection during power transitions. RST# high enables normal operation. Exit from reset places the device in asynchronous read array mode.
WAIT	Output	**WAIT:** Indicates data valid in synchronous array or non-array burst reads. Read Configuration Register bit 10 (RCR 10, WT) determines its polarity when asserted. WAIT's active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is high-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, WAIT indicates invalid data when asserted and valid data when deasserted. • In asynchronous page mode, and all write modes, WAIT is deasserted.
WE#	Input	**WRITE ENABLE:** Active low input. WE# controls writes to the device. Address and data are latched on the rising edge of WE#.
WP#	Input	**WRITE PROTECT:** Active low input. WP# low enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the Unlock command. WP# high overrides the lock-down function enabling blocks to be erased or programmed using software commands.
VPP	Power/ Input	**Erase and Program Power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system program and erase operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as V_{PPL} min. V_{PP} must remain above V_{PPL} min to perform in-system flash modification. VPP may be 0 V during read operations. V_{PPH} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. VPP can be connected to 9 V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9 V may reduce block cycling capability.
VCC	Power	**Device Core Power Supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \le V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
VCCQ	Power	**Output Power Supply:** Output-driver source voltage.
VSS	Power	**Ground:** Connect to system ground. Do not float any VSS connection.
RFU	—	**Reserved for Future Use:** Reserved by Numonyx for future device functionality and enhancement. These should be treated in the same way as a Don't Use (DU) signal.
DU	—	**Don't Use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No Connect:** No internal connection; can be driven or floated.

4.3 Dual Die SCSP Configurations

Figure 10: 512-Mbit Easy BGA / TSOP Top or Bottom Parameter Block Diagram

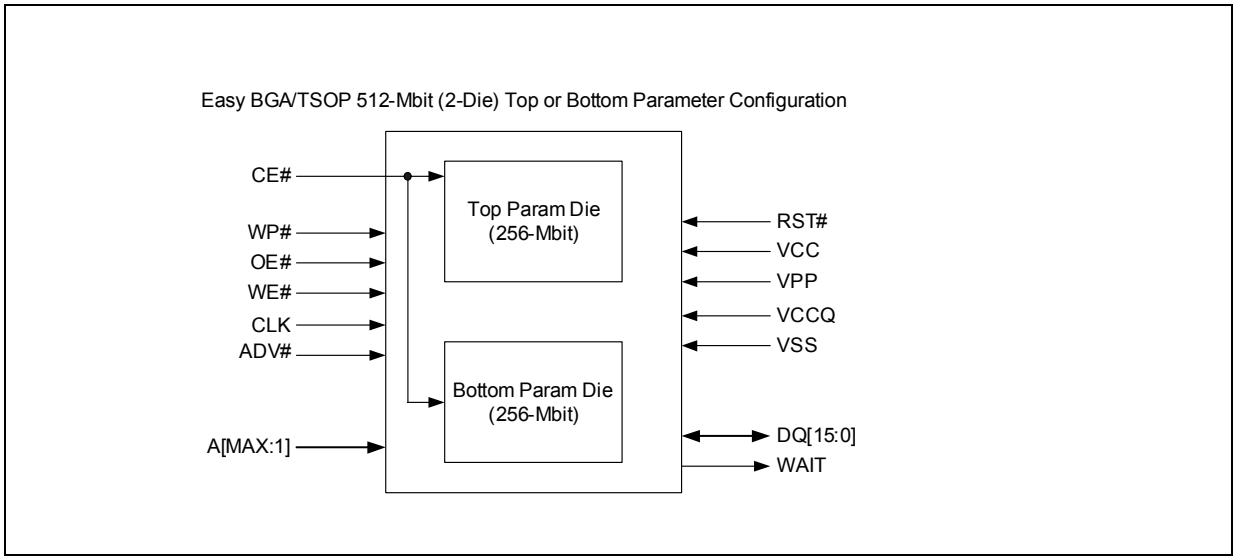
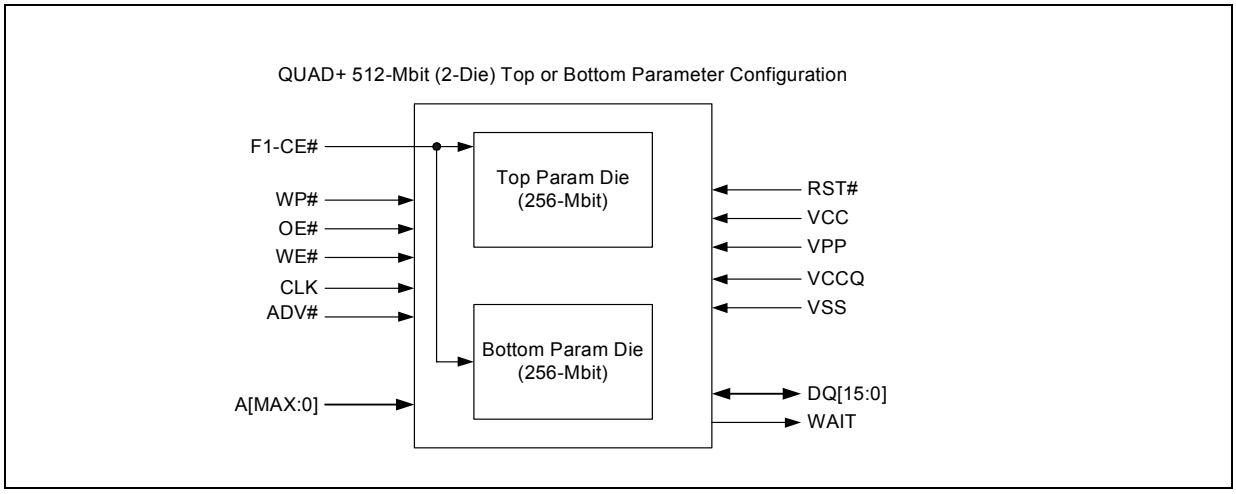


Figure 11: 512-Mbit QUAD+ SCSP Top or Bottom Parameter Block Diagram



Note: $A_{max}=V_{ih}$ selectes the Top Parameter Die; $A_{max}=V_{il}$ selects the Bottom Parameter Die.

4.4 Memory Maps

Table 8 through Table 10 show the Numonyx™ StrataFlash® Embedded Memory (P33) maps. The memory array is divided into multiple 8-Mbit Programming Regions (see Section 11.3, "Programming Operations" on page 57).

Table 8: Discrete Top Parameter Memory Maps (all packages)

	Size (KB)	Blk	64-Mbit
One Programming Region	32	66	3FC000 - 3FFFFF
	⋮	⋮	⋮
	32	63	3F0000 - 3F3FFF
	128	62	3E0000 - 3EFFFF
	⋮	⋮	⋮
	128	56	380000 - 38FFFF
Seven Programming Regions	128	55	370000 - 37FFFF
	128	54	360000 - 36FFFF
	⋮	⋮	⋮
	128	1	010000 - 01FFFF
	128	0	000000 - 00FFFF

	Size (KB)	Blk	128-Mbit
One Programming Region	32	130	7FC000 - 7FFFFF
	⋮	⋮	⋮
	32	127	7F0000 - 7F3FFF
	128	126	7E0000 - 7EFFFF
	⋮	⋮	⋮
	128	120	780000 - 78FFFF
Fifteen Programming Regions	128	119	770000 - 77FFFF
	128	118	760000 - 76FFFF
	⋮	⋮	⋮
	128	1	010000 - 01FFFF
	128	0	000000 - 00FFFF

	Size (KB)	Blk	256-Mbit
One Programming Region	32	258	FFC000 - FFFFFF
	⋮	⋮	⋮
	32	255	FF0000 - FF3FFF
	128	254	FE0000 - FEFFFF
	⋮	⋮	⋮
	128	248	F80000 - F8FFFF
Thirty-One Programming Regions	128	247	F70000 - F7FFFF
	128	246	F60000 - F6FFFF
	⋮	⋮	⋮
	128	1	010000 - 01FFFF
	128	0	000000 - 00FFFF

Table 9: Discrete Bottom Parameter Memory Maps (all packages)

	Size (KB)	Blk	64-Mbit
Seven Programming Regions	128	66	3F0000 - 3FFFFF
	128	65	3E0000 - 3EFFFF
	⋮	⋮	⋮
	128	12	090000 - 09FFFF
	128	11	080000 - 08FFFF

	Size (KB)	Blk	128-Mbit
Fifteen Programming Regions	128	130	7F0000 - 7FFFFF
	128	129	7E0000 - 7EFFFF
	⋮	⋮	⋮
	128	12	090000 - 09FFFF
	128	11	080000 - 08FFFF

Table 9: Discrete Bottom Parameter Memory Maps (all packages)

	Size (KB)	Blk	64-Mbit
One Programming Region	128	10	070000 - 07FFFF
	⋮	⋮	⋮
	128	4	010000 - 01FFFF
	32	3	00C000 - 00FFFF
	⋮	⋮	⋮
	32	0	000000 - 003FFF

	Size (KB)	Blk	128-Mbit
One Programming Region	128	10	070000 - 07FFFF
	⋮	⋮	⋮
	128	4	010000 - 01FFFF
	32	3	00C000 - 00FFFF
	⋮	⋮	⋮
	32	0	000000 - 003FFF

	Size (KB)	Blk	256-Mbit
Thirty-One Programming Regions	128	258	FF0000 - FFFFFF
	128	257	FE0000 - FEFFFF
	⋮	⋮	⋮
	128	12	090000 - 09FFFF
	128	11	080000 - 08FFFF
One Programming Region	128	10	070000 - 07FFFF
	⋮	⋮	⋮
	128	4	010000 - 01FFFF
	32	3	00C000 - 00FFFF
	⋮	⋮	⋮
	32	0	000000 - 003FFF

Block size is referenced in K-Bytes where a byte=8 bits. Block Address range is referenced in K-Words where a Word is the size of the flash output bus (16 bits).

Note: The Dual-Die memory map are the same for both parameter options.

Table 10: 512-Mbit Top and Bottom Parameter Memory Map (Easy BGA, TSOP, and QUAD+ SCSP) (Sheet 1 of 2)

512-Mbit Flash (2x256-Mbit w/ 1CE)			
Die Stack Config	**Size (KB)**	**Blk**	**Address Range**
256-Mbit Top Parameter Die	32	517	1FFC000 - 1FFFFFF
	⋮	⋮	⋮
	32	514	1FF0000 - 1FF3FFF
	128	513	1FE0000 - 1FEFFFF
	⋮	⋮	⋮
	128	259	1000000 - 100FFFF
	128	258	FF0000 - FFFFFF
	⋮	⋮	⋮

Table 10: 512-Mbit Top and Bottom Parameter Memory Map (Easy BGA, TSOP, and QUAD+ SCSP) (Sheet 2 of 2)

512-Mbit Flash (2x256-Mbit w/ 1CE)			
Die Stack Config	**Size (KB)**	**Blk**	**Address Range**
256-Mbit	128	4	010000 - 01FFFF
Bottom Parameter Die	32	3	00C000 - 00FFFF
	⋮	⋮	⋮
	32	0	000000 - 003FFF

Note: Refer to the appropriate 256-Mbit Memory Map (Table 8 or Table 9) for Programming Region information. Block size is referenced in K-Bytes where a byte=8 bits. Block Address range is referenced in K-Words where a Word is the size of the flash output bus (16 bits).