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Micron Parallel NOR Flash Embedded Memory (P33-65nm)

JS28F512P33BFD, JS28F512P33TFA, JS28F512P33EFA
PC28F512P33BFD, PC28F512P33TFA, PC28F512P33EFA
JS28F00AP33BFA, JS28F00AP33TFA, JS28F00AP33EFA
PC28F00AP33BFA, PC28F00AP33TFA, PC28F00AP33EFA,
PC28F00BP33EFA

Features

- High performance
- Easy BGA package features
  - 95ns initial access for 512Mb, 1Gb Easy BGA
  - 100ns initial access for 2Gb Easy BGA
  - 25ns 16-word asychronous page read mode
  - 52 MHz (Easy BGA) with zero WAIT states and 17ns clock-to-data output synchronous burst read mode
  - 4-, 8-, 16-, and continuous word options for burst mode
- TSOP package features
  - 105ns initial access for 512Mb, 1Gb TSOP
- Both Easy BGA and TSOP package features
  - Buffered enhanced factory programming (BEFP) at 2 MB/s (TYP) using a 512-word buffer
  - 3.0V buffered programming at 1.46 MB/s (TYP) using a 512-word buffer
- Architecture
  - MLC: highest density at lowest cost
  - Symmetrically blocked architecture (512Mb, 1Gb, 2Gb)
  - Asymmetrically blocked architecture (512Mb, 1Gb); four 32KB parameter blocks: top or bottom configuration
  - 128KB main blocks
  - Blank check to verify an erased block
- Voltage and power
  - V_{CC} (core) voltage: 2.3–3.6V
  - V_{CCQ} (I/O) voltage: 2.3–3.6V
  - Standy current: 70µA (TYP) for 512Mb; 75µA (TYP) for 1Gb
  - 52 MHz continuous synchronous read current: 21mA (TYP), 24mA (MAX)
- Security
  - One-time programmable register: 64 OTP bits, programmed with unique information from Micron; 2112 OTP bits available for customer programming
  - Absolute write protection: $V_{PP} = V_{SS}$
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down
  - Password access
- Software
  - 25µs (TYP) program suspend
  - 25µs (TYP) erase suspend
  - Flash Data Integrator optimized
  - Basic command set and extended function Interface (EFI) command set compatible
  - Common flash interface
- Density and Packaging
  - 56-lead TSOP package (512Mb, 1Gb)
  - 64-ball Easy BGA package (512Mb, 1Gb, 2Gb)
  - 16-bit wide data bus
- Quality and reliabilty
  - JESD47 compliant
  - Operating temperature: –40°C to +85°C
  - Minimum 100,000 ERASE cycles per block
  - 65nm process technology

Discrete and MCP Part Numbering Information

Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Note: Not all part numbers listed here are available for ordering.

Table 1: Discrete Part Number Information

Part Number Category	Category Details
Package	JS = 56-lead TSOP, lead free
	PC = 64-ball Easy BGA, lead-free
Product Line	28F = Micron Flash memory
Density	512 = 512Mb 00A = 1Gb 00B = 2Gb
Product Family	P33 (V_{CC} = 2.3–3.6V; V_{CCQ} = 2.3–3.6V)
Parameter Location	B/T = Bottom/Top parameter E = Symmetrical Blocks
Lithography	F = 65nm
Features	*

Note: 1. The last digit is assigned randomly to cover packaging media, features, or other specific configuration information. Sample part number: JS28F512P33EF*

Table 2: Standard Part Numbers

Density	Configuration	Medium	JS	PC
512Mb	Bottom boot	Tray	JS28F512P33BFD	PC28F512P33BFD
		Tape & Reel	–	–
	Top boot	Tray	JS28F512P33TFA	PC28F512P33TFA
		Tape & Reel	–	–
	Uniform	Tray	JS28F512P33EFA	PC28F512P33EFA
		Tape & Reel	–	–
1Gb	Bottom boot	Tray	JS28F00AP33BFA	PC28F00AP33BFA
		Tape & Reel	–	–
	Top boot	Tray	JS28F00AP33TFA	PC28F00AP33TFA
		Tape & Reel	–	–
	Uniform	Tray	JS28F00AP33EFA	PC28F00AP33EFA
		Tape & Reel	–	–
2Gb	Uniform	Tray	–	PC28F00BP33EFA
		Tape & Reel	–	–

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General Description

The Micron Parallel NOR Flash memory is the latest generation of Flash memory devices. Benefits include more density in less space, high-speed interface device, and support for code and data storage. Features include high-performance synchronous-burst read mode, fast asynchronous access times, low power, flexible security options, and three industry-standard package choices. The product family is manufactured using Micron 65nm process technology.

The NOR Flash device provides high performance at low voltage on a 16-bit data bus. Individually erasable memory blocks are sized for optimum code and data storage.

Upon initial power up or return from reset, the device defaults to asynchronous page-mode read. Configuring the read configuration register enables synchronous burst-mode reads. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

In addition to the enhanced architecture and interface, the device incorporates technology that enables fast factory PROGRAM and ERASE operations. Designed for low-voltage systems, the devIce supports READ operations with V_{CC} at the low voltages, and ERASE and PROGRAM operations with V_{PP} at the low voltages or V_{PPH}. Buffered enhanced factory programming (BEFP) provides the fastest Flash array programming performance with V_{PP} at V_{PPH}, which increases factory throughput. With V_{PP} at low voltages, V_{CC} and V_{PP} can be tied together for a simple, ultra low-power design. In addition to voltage flexibility, a dedicated V_{PP} connection provides complete data protection when $V_{PP} \le V_{PPLK}$.

A command user interface is the interface between the system processor and all internal operations of the device. The device automatically executes the algorithms and timings necessary for block erase and program. A status register indicates ERASE or PROGRAM completion and any errors that may have occurred.

An industry-standard command sequence invokes program and erase automation. Each ERASE operation erases one block. The erase suspend feature enables system software to pause an ERASE cycle to read or program data in another block. Program suspend enables system software to pause programming to read other locations. Data is programmed in word increments (16 bits).

The protection register enables unique device identification that can be used to increase system security. The individual block lock feature provides zero-latency block locking and unlocking. The device includes enhanced protection via password access; this new feature supports write and/or read access protection of user-defined blocks. In addition, the device also provides the full-device OTP security feature.

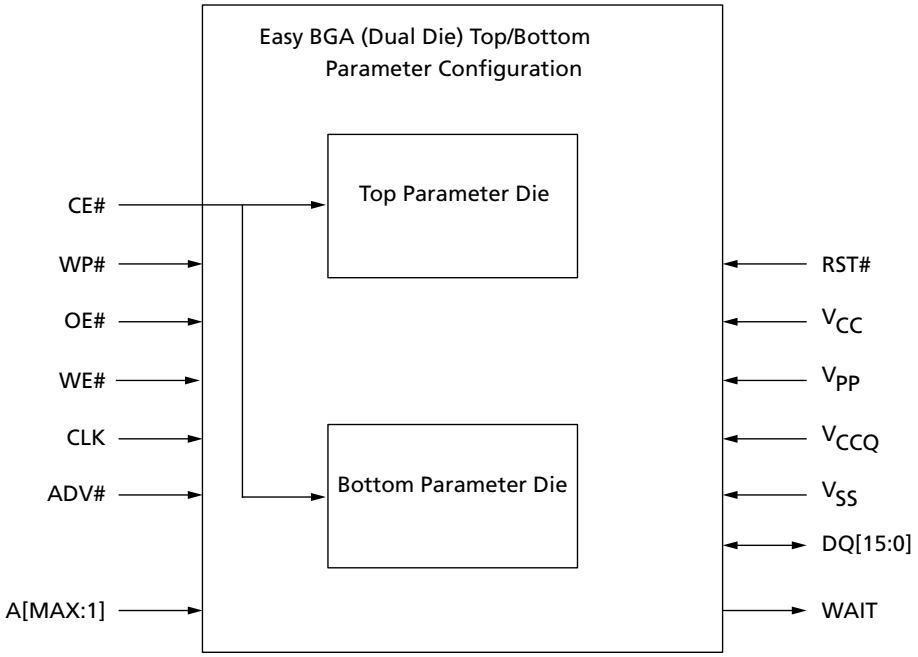
Virtual Chip Enable Description

The 2Gb device employs a virtual chip enable feature, which combines two 1Gb die with a common chip enable, CE# for Easy BGA packages. The maximum address bit is then used to select between the die pair with CE# asserted. When CE# is asserted and the maximum address bit is LOW, the lower parameter die is selected; when CE# is asserted and the maximum address bit is HIGH, the upper parameter die is selected.

Table 3: Virtual Chip Enable Truth Table for Easy BGA Packages

Die Selected	CE#	A[MAX]
Lower parameter die	L	L
Upper parameter die	L	H

Figure 1: Easy BGA Block Diagram



Memory Map

Figure 2: Memory Map – 512Mb and 1Gb

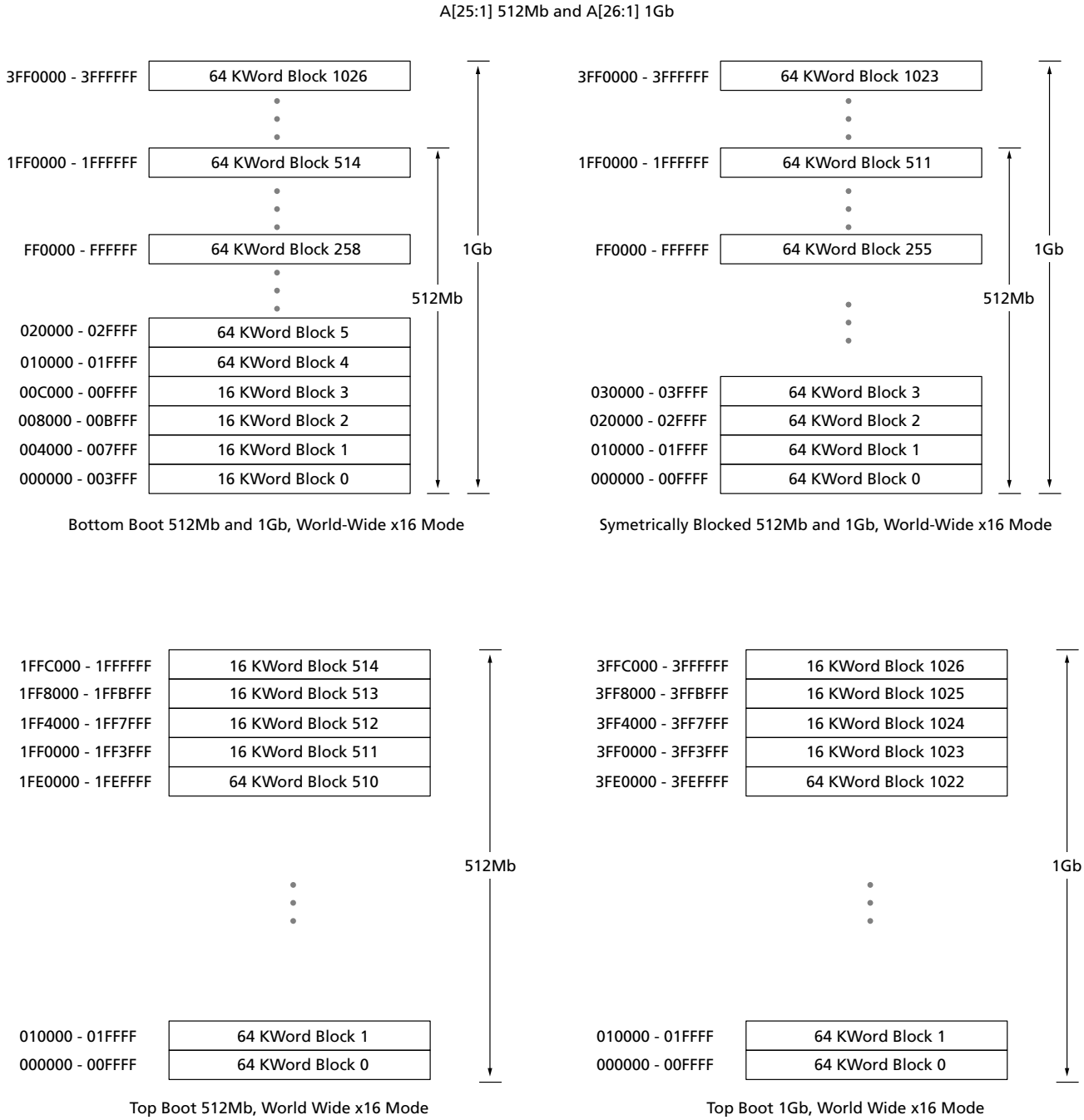
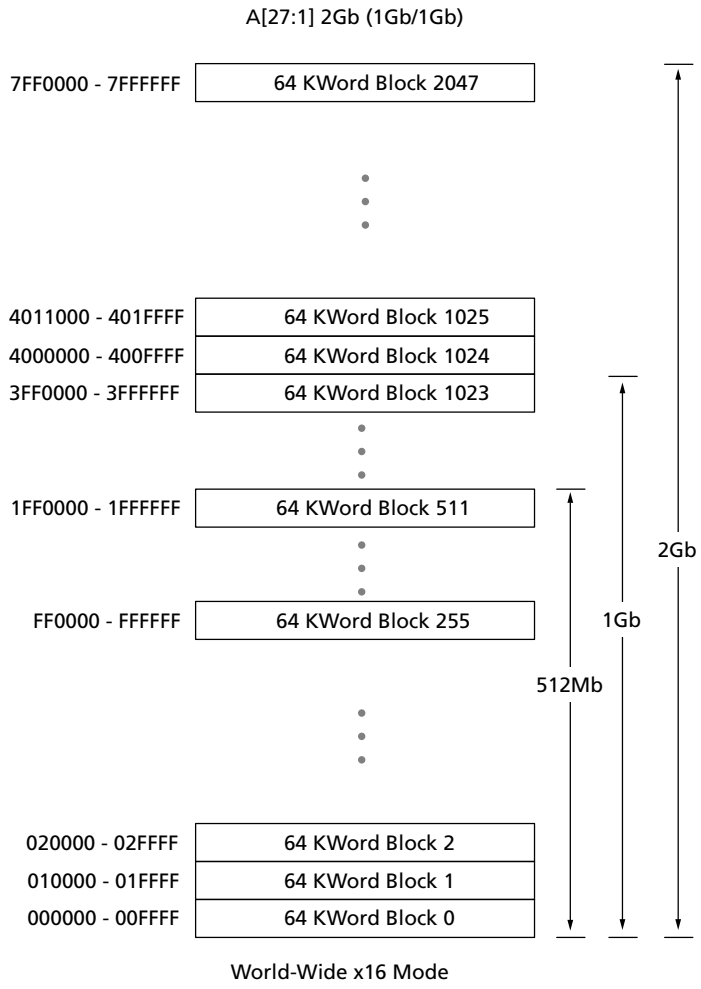
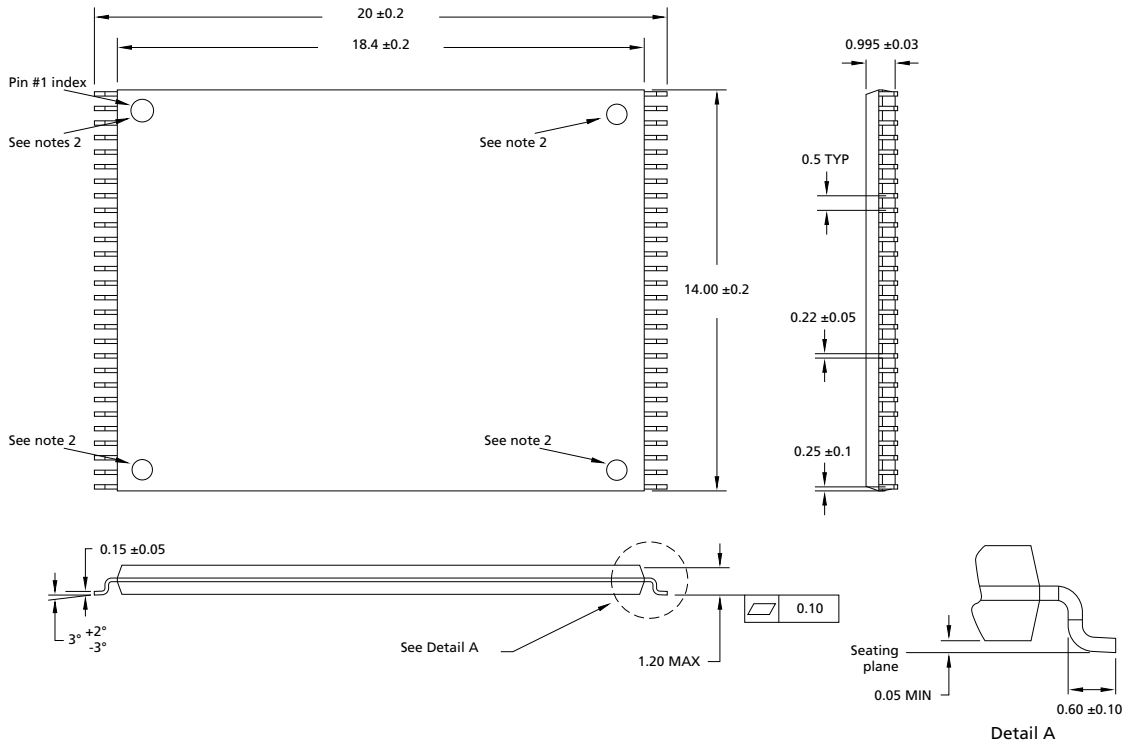


Figure 3: Memory Map – 2Gb



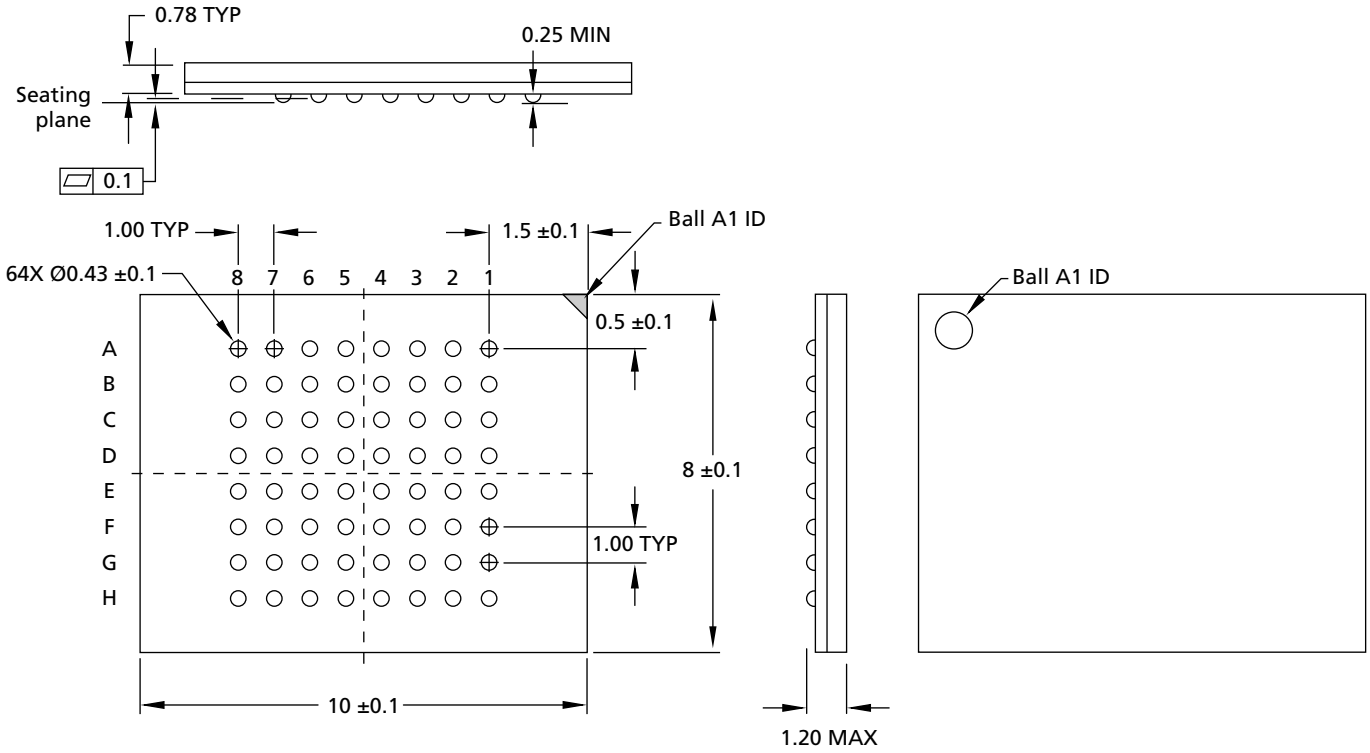
Package Dimensions

Figure 4: 56-Pin TSOP – 14mm x 20mm



Notes:
1. All dimensions are in millimeters. Drawing not to scale.
2. One dimple on package denotes pin 1; if two dimples, then the larger dimple denotes pin 1. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.
3. For the lead width value of 0.22 ±0.05, there is also a legacy value of 0.15 ±0.05.

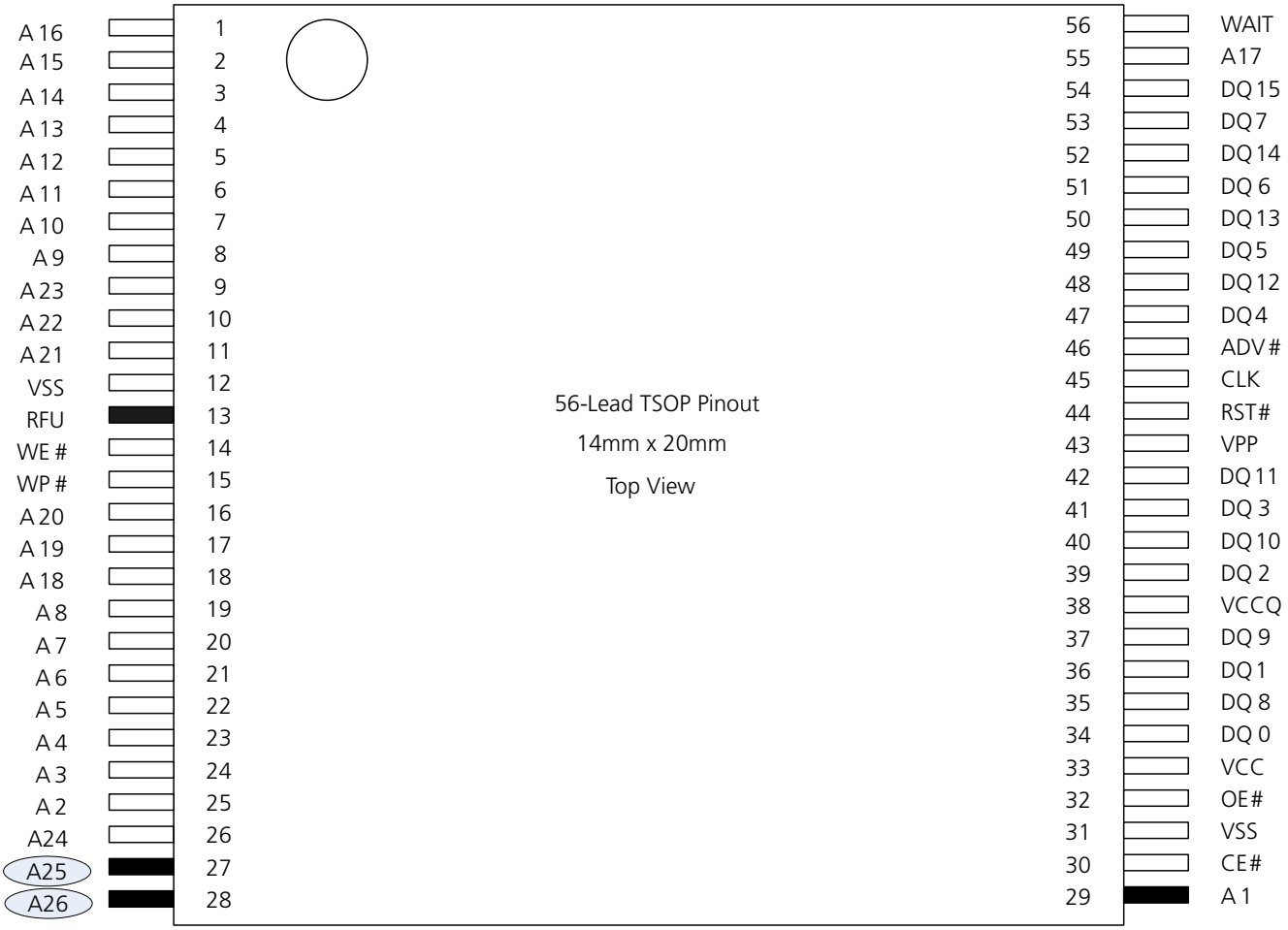
Figure 5: 64-Ball Easy BGA – 8mm x 10mm x 1.2mm



Notes:
1. All dimensions are in millimeters. Drawing not to scale.
2. The 512Mb device does not contain the A1 ID ball located on the back side of the device.

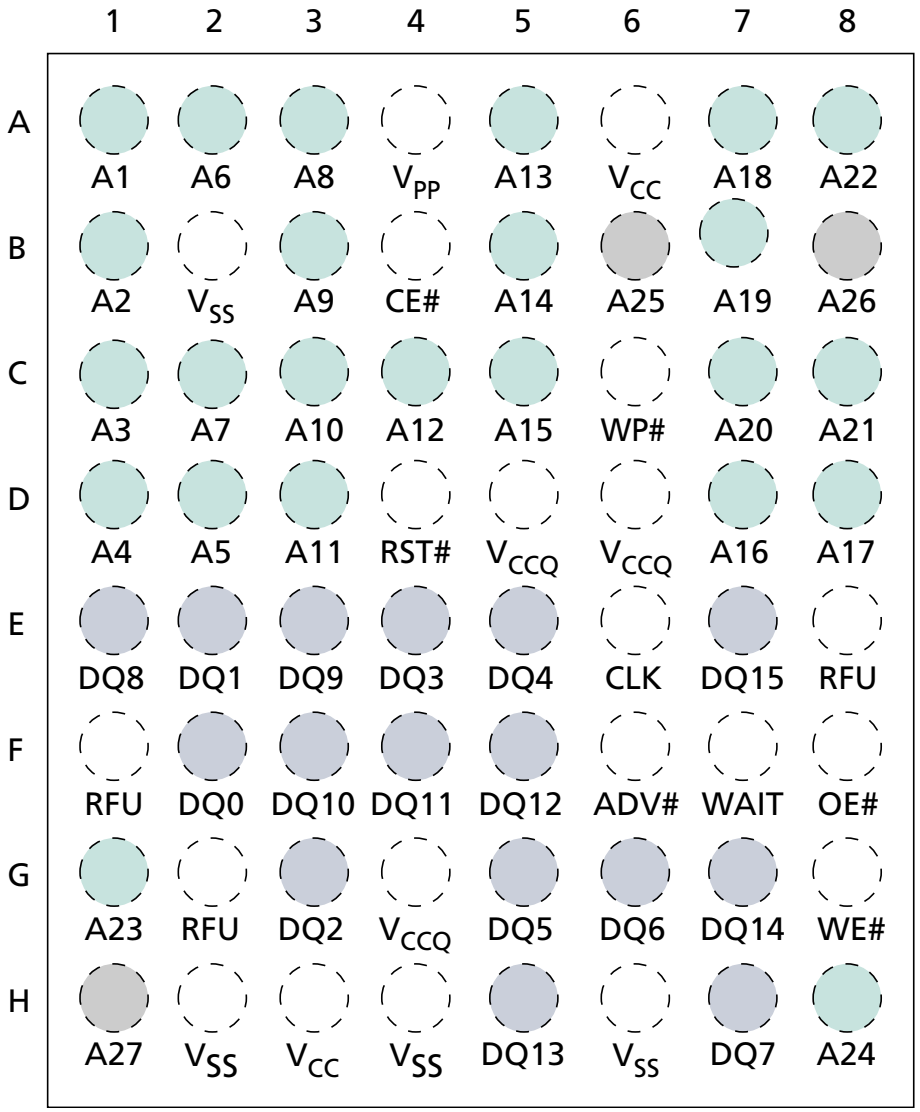
Pinouts and Ballouts

Figure 6: 56-Lead TSOP Pinout – 512Mb and 1Gb



Notes:
1. A1 is the least significant address bit.
2. ADV# must be tied to V_{SS} or driven to LOW throughout the asynchronous read mode.
3. A25 is valid for 512Mb densities and above; otherwise, it is a no connect (NC).
4. A26 is valid for 1Gb densities and above; otherwise, it is a no connect (NC).
5. One dimple on package denotes Pin 1 which will always be in the upper left corner of the package, in reference to the product mark.

Figure 7: 64-Ball Easy BGA (Top View – Balls Down) – 512Mb, 1Gb, and 2Gb



Notes:
1. A1 is the least significant address bit.
2. A25 is valid for 512Mb densities and above; otherwise, it is a no connect (NC).
3. A26 is valid for 1Gb densities and above; otherwise, it is a no connect (NC).
4. A27 is valid for 2Gb densities and above; otherwise, it is a no connect (NC).
5. One dimple on package denotes Pin 1 which will always be in the upper left corner of the package, in reference to the product mark.

Signal Descriptions

Table 4: TSOP and Easy BGA Signal Descriptions

Symbol	Type	Name and Function
A[MAX:1]	Input	**Address inputs:** Device address inputs. **Note:** Unused active address pins should not be left floating; tie them to V_{CCQ} or V_{SS} according to specific design requirements.
ADV#	Input	**Address valid:** Active LOW input. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. In asynchronous mode, the address is latched when ADV# goes HIGH or continuously flows through if ADV# is held LOW. **Note:** Designs not using ADV# must tie it to V_{SS} to allow addresses to flow through.
CE#	Input	**Chip enable:** Active LOW input. CE# LOW selects the associated die. When asserted, internal control logic, input buffers, decoders, and sense amplifiers are active. When de-asserted, the associated die is deselected, power is reduced to standby levels, data and wait outputs are placed in High-Z. **Note:** CE# must be driven HIGH when device is not in use.
CLK	Input	**Clock:** Synchronizes the device with the system bus frequency in synchronous-read mode. During synchronous READs, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. **Note:** Designs not using CLK for synchronous read mode must tie it to V_{CCQ} or V_{SS}.
OE#	Input	**Output enable:** Active LOW input. OE# LOW enables the device's output data buffers during READ cycles. OE# HIGH places the data outputs and WAIT in High-Z.
RST#	Input	**Reset:** Active LOW input. RST# resets internal automation and inhibits WRITE operations. This provides data protection during power transitions. RST# HIGH enables normal operation. Exit from reset places the device in asynchronous read array mode.
WP#	Input	**Write protect:** Active LOW input. WP# LOW enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the Unlock command. WP# HIGH overrides the lock-down function enabling blocks to be erased or programmed using software commands. **Note:** Designs not using WP# for protection could tie it to V_{CCQ} or V_{SS} without additional capacitor.
WE#	Input	**Write enable:** Active LOW input. WE# controls writes to the device. Address and data are latched on the rising edge of WE# or CE#, whichever occurs first.
V_{PP}	Power/Input	**Erase and program power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system PROGRAM and ERASE operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as $V_{PPL,min}$. V_{PP} must remain above $V_{PPL,min}$ to perform in-system modification. V_{PP} may be 0V during READ operations. V_{PP} can be connected to 9V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9V may reduce block cycling capability.
DQ[15:0]	Input/Output	**Data input/output:** Inputs data and commands during WRITE cycles; outputs data during memory, status register, protection register, and read configuration register reads. Data balls float when the CE# or OE# are de-asserted. Data is internally latched during writes.

Table 4: TSOP and Easy BGA Signal Descriptions (Continued)

Symbol	Type	Name and Function
WAIT	Output	**Wait:** Indicates data valid in synchronous array or non-array burst reads. Read configuration register bit 10 (RCR.10, WT) determines its polarity when asserted. This signal's active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is High-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, this signal indicates invalid data when asserted and valid data when de-asserted. • In asynchronous page mode, and all write modes, this signal is de-asserted.
V_{CC}	Power	**Device core power supply:** Core (logic) source voltage. Writes to the array are inhibited when $V_{CC} \le V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	Power	**Output power supply:** Output-driver source voltage.
V_{SS}	Power	**Ground:** Connect to system ground. Do not float any V_{SS} connection.
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a DU signal.
DU	—	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No connect:** No internal connection; can be driven or floated.

Bus Operations

CE# LOW and RST# HIGH enable READ operations. The device internally decodes upper address inputs to determine the accessed block. ADV# LOW opens the internal address latches. OE# LOW activates the outputs and gates selected data onto the I/O bus.

Bus cycles to/from the device conform to standard microprocessor bus operations. Bus operations and the logic levels that must be applied to the device control signal inputs are shown here.

Table 5: Bus Operations

Bus Operation		RST#	CLK	ADV#	CE#	OE#	WE#	WAIT	DQ[15:0]	Notes
READ	Asynchronous	H	X	L	L	L	H	De-asserted	Output	-
	Synchronous	H	Running	L	L	L	H	Driven	Output	-
WRITE		H	X	L	L	H	L	High-Z	Input	1
OUTPUT DISABLE		H	X	X	L	H	H	High-Z	High-Z	2
STANDBY		H	X	X	H	X	X	High-Z	High-Z	2
RESET		L	X	X	X	X	X	High-Z	High-Z	2, 3

Notes:
1. Refer to the Device Command Bus Cycles for valid DQ[15:0] during a WRITE operation.
2. X = "Don't Care" (H or L).
3. RST# must be at V_{SS} ± 0.2V to meet the maximum specified power-down current.

Read

To perform a READ operation, RST# and WE# must be de-asserted while CE# and OE# are asserted. CE# is the device-select control. When asserted, it enables the device. OE# is the data-output control. When asserted, the addressed flash memory data is driven onto the I/O bus.

Write

To perform a WRITE operation, both CE# and WE# are asserted while RST# and OE# are de-asserted. During a WRITE operation, address and data are latched on the rising edge of WE# or CE#, whichever occurs first. The Command Bus Cycles table shows the bus cycle sequence for each of the supported device commands, while the Command Codes and Definitions table describes each command.

Note: WRITE operations with invalid V_{CC} and/or V_{PP} voltages can produce spurious results and should not be attempted.

Output Disable

When OE# is de-asserted, device outputs DQ[15:0] are disabled and placed in High-Z state, WAIT is also placed in High-Z.

Standby

When CE# is de-asserted the device is deselected and placed in standby, substantially reducing power consumption. In standby, the data outputs are placed in High-Z, independent of the level placed on OE#. Standby current (I_{CCS}) is the average current meas-

ured over any 5ms time interval, 5µs after CE# is de-asserted. During standby, average current is measured over the same time interval 5µs after CE# is de-asserted.

When the device is deselected (while CE# is de-asserted) during a PROGRAM or ERASE operation, it continues to consume active power until the PROGRAM or ERASE operation is completed.

Reset

As with any automated device, it is important to assert RST# when the system is reset. When the system comes out of reset, the system processor attempts to read from the device if it is the system boot device. If a CPU reset occurs with no device reset, improper CPU initialization may occur because the device may be providing status information rather than array data. Micron devices enable proper CPU initialization following a system reset through the use of the RST# input. RST# should be controlled by the same low-true reset signal that resets the system CPU.

After initial power-up or reset, the device defaults to asynchronous read array mode, and the status register is set to 0x80. Asserting RST# de-energizes all internal circuits, and places the output drivers in High-Z. When RST# is asserted, the device shuts down the operation in progress, a process which takes a minimum amount of time to complete. When RST# has been de-asserted, the device is reset to asynchronous read array state.

When device returns from a reset (RST# de-asserted), a minimum wait is required before the initial read access outputs valid data. Also, a minimum delay is required after a reset before a write cycle can be initiated. After this wake-up interval passes, normal operation is restored.

Note: If RST# is asserted during a PROGRAM or ERASE operation, the operation is terminated and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, because the data may have been only partially written or erased.

Device Command Codes

The system CPU provides control of all in-system READ, WRITE, and ERASE operations of the device via the system bus. The device manages all block-erase and word-program algorithms.

Device commands are written to the CUI to control all device operations. The CUI does not occupy an addressable memory location; it is the mechanism through which the device is controlled.

Note: For a dual device, all setup commands should be re-issued to the device when a different die is selected.

Table 6: Command Codes and Definitions

Mode	Device Mode	Code	Description
Read	Read array	0xFF	Places the device in read array mode. Array data is output on DQ[15:0].
	Read status register	0x70	Places the device in read status register mode. The device enters this mode after a PROGRAM or ERASE command is issued. Status register data is output on DQ[7:0].
	Read device ID or read configuration register	0x90	Places device in read device identifier mode. Subsequent reads output manufacturer/device codes, configuration register data, block lock status, or protection register data on DQ[15:0].
	Read CFI	0x98	Places the device in read CFI mode. Subsequent reads output CFI information on DQ[7:0].
	Clear status register	0x50	The device sets status register error bits. The clear status register command is used to clear the SR error bits.
Write	Word program setup	0x40	First cycle of a 2-cycle programming command; prepares the CUI for a WRITE operation. On the next write cycle, the address and data are latched and the device executes the programming algorithm at the addressed location. During PROGRAM operations, the device responds only to READ STATUS REGISTER and PROGRAM SUSPEND commands. CE# or OE# must be toggled to update the status register in asynchronous read. CE# or ADV# must be toggled to update the status register data for synchronous non-array reads. The READ ARRAY command must be issued to read array data after programming has finished.
	Buffered program	0xE8	This command loads a variable number of words up to the buffer size of 512 words onto the program buffer.
	Buffered program confirm	0xD0	The CONFIRM command is issued after the data streaming for writing into the buffer is completed. The device then performs the buffered program algorithm, writing the data from the buffer to the memory array.
	BEFP setup	0x80	First cycle of a two-cycle command; initiates buffered enhanced factory program mode (BEFP). The CUI then waits for the BEFP CONFIRM command, 0xD0, that initiates the BEFP algorithm. All other commands are ignored when BEFP mode begins.
	BEFP confirm	0xD0	If the previous command was BEFP SETUP (0x80), the CUI latches the address and data, and prepares the device for BEFP mode.

Table 6: Command Codes and Definitions (Continued)

Mode	Device Mode	Code	Description
Erase	Block erase setup	0x20	First cycle of a two-cycle command; prepares the CUI for a BLOCK ERASE operation. The device performs the erase algorithm on the block addressed by the ERASE CONFIRM command. If the next command *is not* the ERASE CONFIRM (0xD0) command, the CUI sets status register bits SR4 and SR5, and places the device in read status register mode.
	Block erase confirm	0xD0	If the first command was BLOCK ERASE SETUP (0x20), the CUI latches the address and data, and the device erases the addressed block. During BLOCK ERASE operations, the device responds only to READ STATUS REGISTER and ERASE SUSPEND commands. CE# or OE# must be toggled to update the status register in asynchronous read. CE# or ADV# must be toggled to update the status register data for synchronous non-array reads.
Suspend	Program or erase suspend	0xB0	This command issued to any device address initiates a suspend of the currently-executing program or BLOCK ERASE operation. The status register indicates successful suspend operation by setting either SR2 (program suspended) or SR6 (erase suspended), along with SR7 (ready). The device remains in the suspend mode regardless of control signal states (except for RST# asserted).
	Suspend resume	0xD0	This command issued to any device address resumes the suspended PROGRAM or BLOCK ERASE operation.
Protection	Block lock setup	0x60	First cycle of a two-cycle command; prepares the CUI for block lock configuration changes. If the next command is not BLOCK LOCK (0x01), BLOCK UNLOCK (0xD0), or BLOCK LOCK DOWN (0x2F), the CUI sets status register bits SR5 and SR4, indicating a command sequence error.
	Block lock	0x01	If the previous command was BLOCK LOCK SETUP (0x60), the addressed block is locked.
	Block unlock	0xD0	If the previous command was BLOCK LOCK SETUP (0x60), the addressed block is unlocked. If the addressed block is in a lock down state, the operation has no effect.
	Block lock down	0x2F	If the previous command was BLOCK LOCK SETUP (0x60), the addressed block is locked down.
	OTP register or lock register program setup	0xC0	First cycle of a two-cycle command; prepares the device for a OTP REGISTER or LOCK REGISTER PROGRAM operation. The second cycle latches the register address and data, and starts the programming algorithm to program data the OTP array.
Configuration	Read configuration register setup	0x60	First cycle of a two-cycle command; prepares the CUI for device read configuration. If the SET READ CONFIGURATION REGISTER command (0x03) is not the next command, the CUI sets status register bits SR4 and SR5, indicating a command sequence error.
	Read configuration register	0x03	If the previous command was READ CONFIGURATION REGISTER SETUP (0x60), the CUI latches the address and writes A[16:1] to the read configuration register for Easy BGA and TSOP, A[15:0] for QUAD+. Following a CONFIGURE READ CONFIGURATION REGISTER command, subsequent READ operations access array data.

Table 6: Command Codes and Definitions (Continued)

Mode	Device Mode	Code	Description
Blank Check	Block blank check	0xBC	First cycle of a two-cycle command; initiates the BLANK CHECK operation on a main block.
	Block blank check confirm	0xD0	Second cycle of blank check command sequence; it latches the block address and executes blank check on the main array block.
EFI	Extended function interface	0xEB	First cycle of a multiple-cycle command; initiate operation using extended function interface. The second cycle is a Sub-Op-Code, the data written on third cycle is one less than the word count; the allowable value on this cycle are 0–511. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved.

Device Command Bus Cycles

Device operations are initiated by writing specific device commands to the command user interface (CUI). Several commands are used to modify array data including WORD PROGRAM and BLOCK ERASE commands. Writing either command to the CUI initiates a sequence of internally timed functions that culminate in the completion of the requested task. However, the operation can be aborted by either asserting RST# or by issuing an appropriate suspend command.

Table 7: Command Bus Cycles

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Op	Addr[1]	Data[2]	Op	Addr[1]	Data[2]
Read	READ ARRAY	1	WRITE	DnA	0xFF	–	–	–
	READ DEVICE IDENTIFIER	≥2	WRITE	DnA	0x90	READ	DBA + IA	ID
	READ CFI	≥2	WRITE	DnA	0x98	READ	DBA + CFI-A	CFI-D
	READ STATUS REGISTER	2	WRITE	DnA	0x70	READ	DnA	SRD
	CLEAR STATUS REGISTER	1	WRITE	DnA	0x50	–	–	–
Program	WORD PROGRAM	2	WRITE	WA	0x40	WRITE	WA	WD
	BUFFERED PROGRAM[3]	>2	WRITE	WA	0xE8	WRITE	WA	N - 1
	BUFFERED ENHANCED FACTORY PROGRAM (BEFP)[4]	>2	WRITE	WA	0x80	WRITE	WA	0xD0
Erase	BLOCK ERASE	2	WRITE	BA	0x20	WRITE	BA	0xD0
Suspend	PROGRAM/ERASE SUSPEND	1	WRITE	DnA	0xB0	–	–	–
	PROGRAM/ERASE RESUME	1	WRITE	DnA	0xD0	–	–	–
Protection	BLOCK LOCK	2	WRITE	BA	0x60	WRITE	BA	0x01
	BLOCK UNLOCK	2	WRITE	BA	0x60	WRITE	BA	0xD0
	BLOCK LOCK DOWN	2	WRITE	BA	0x60	WRITE	BA	0x2F
	PROGRAM OTP REGISTER	2	WRITE	PRA	0xC0	WRITE	OTP-RA	OTP-D
	PROGRAM LOCK REGISTER	2	WRITE	LRA	0xC0	WRITE	LRA	LRD
Configuration	CONFIGURE READ CONFIGURATION REGISTER	2	WRITE	RCD	0x60	WRITE	RCD	0x03
Blank Check	BLOCK BLANK CHECK	2	WRITE	BA	0xBC	WRITE	BA	D0
EFI	EXTENDED FUNCTION INTERFACE [5]	>2	WRITE	WA	0xEB	Write	WA	Sub-Op code

Notes:
1. First command cycle address should be the same as the operation's target address. DBA = Device base address (needed for dual die 512Mb device); DnA = Address within the device; IA = Identification code address offset; CFI-A = Read CFI address offset; WA = Word address of memory location to be written; BA = Address within the block; OTP-RA = Protection register address; LRA = Lock register address; RCD = Read configuration register data on A[16:1] for Easy BGA and TSOP, A[15:0] for QUAD+ package.
2. ID = Identifier data; CFI-D = CFI data on DQ[15:0]; SRD = Status register data; WD = Word data; N = Word count of data to be loaded into the write buffer; OTP-D = Protection register data; LRD = Lock register data.

3. The second cycle of the BUFFERED PROGRAM command is the word count of the data to be loaded into the write buffer. This is followed by up to 512 words of data. Then the CONFIRM command (0xD0) is issued, triggering the array programming operation.
4. The CONFIRM command (0xD0) is followed by the buffer data.
5. The second cycle is a Sub-Op-Code, the data written on third cycle is N-1; 1≤ N ≤ 512. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved, after the data words are loaded, the final cycle is the confirm cycle 0xD0).

Read Operations

The device supports two read modes: asynchronous page mode and synchronous burst mode. Asynchronous page mode is the default read mode after device power-up or a reset. Under asynchronous page mode, the device can also perform single word read. The read configuration register must be configured to enable synchronous burst reads of the array.

The device can be in any of four read states: read array, read identifier, read status, or read CFI. Upon power-up, or after a reset, the device defaults to read array. To change the read state, the appropriate READ command must be written to the device.

Asynchronous Single Word Read

To perform an asynchronous single word read, an address is driven onto the address bus, and CE# is asserted.

Note: To perform an asynchronous single word read for a TSOP package, ADV# must be LOW throughout the READ cycle. For an Easy BGA package, ADV# can be driven HIGH to latch the address or be held LOW throughout the READ cycle.

WE# and RST# must already have been de-asserted. WAIT is set to a de-asserted state during single word mode, as determined by bit 10 of the read configuration register. CLK is not used for asynchronous single word reads, and is ignored. If asynchronous reads are to be performed only, CLK should be tied to a valid V_{IH} or V_{SS} level, WAIT can be floated, and ADV# must be tied to ground. After OE# is asserted, the data is driven onto DQ[15:0] after an initial access time ^{t}AVQV or ^{t}GLQV delay.

Asynchronous Page Mode Read (Easy BGA Only)

Note: Asynchronous Page Mode Read is supported only in the main array.

Following a device power-up or reset, asynchronous page mode is the default read mode and the device is set to read array. However, to perform array reads after any other device operation (WRITE operation), the READ ARRAY command must be issued in order to read from the array.

Asynchronous page mode reads can only be performed when read configuration register bit RCR15 is set.

To perform an asynchronous page-mode read, an address is driven onto the address bus, and CE# and ADV# are asserted. WE# and RST# must already have been de-asserted. WAIT is de-asserted during asynchronous page mode. ADV# can be driven HIGH to latch the address, or it must be held LOW throughout the READ cycle. CLK is not used for asynchronous page mode reads, and is ignored. If only asynchronous reads are to be performed, CLK should be tied to a valid V_{IH} or V_{SS} level, WAIT signal can be floated, and ADV# must be tied to ground. Array data is driven onto DQ[15:0] after an initial access time ^{t}AVQV delay.

In asynchronous page mode, 16 data words are “sensed” simultaneously from the array and loaded into an internal page buffer. The buffer word corresponding to the initial address on the address bus is driven onto DQ[15:0] after the initial access delay. The lowest four address bits determine which word of the 16-word page is output from the data buffer at any given time.

Synchronous Burst Mode Read (Easy BGA Only)

Read configuration register bits RCR[15:0] must be set before synchronous burst operation can be performed. Synchronous burst mode can be performed for both array and non-array reads such as read ID, read status, or read query.

To perform a synchronous burst read, an initial address is driven onto the address bus, and CE# and ADV# are asserted. WE# and RST# must already have been de-asserted. ADV# is asserted, and then de-asserted to latch the address. Alternately, ADV# can remain asserted throughout the burst access, in which case the address is latched on the next valid CLK edge while ADV# is asserted.

During synchronous array and non-array read modes, the first word is output from the data buffer on the next valid CLK edge after the initial access latency delay. Subsequent data is output on valid CLK edges following a minimum delay. However, for a synchronous non-array read, the same word of data will be output on successive clock edges until the burst length requirements are satisfied. Refer to the timing diagrams for more detailed information.

Read CFI

The READ CFI command instructs the device to output CFI data when read. See Common Flash Interface for details on issuing the READ CFI command, and for details on addresses and offsets within the CFI database.

Read Device ID

The READ DEVICE IDENTIFIER command instructs the device to output manufacturer code, device identifier code, block lock status, protection register data, or configuration register data.

Table 8: Device ID Information

Item	Address	Data
Manufacturer code	0x00	0x89
Device ID code	0x01	ID (see the Device ID Codes table)
Block lock configuration Block is unlocked Block is locked Block is not locked down Block is locked down	Block base address + 0x02	**Lock bit** DQ_0 = 0b0 DQ_0 = 0b1 DQ_1 = 0b0 DQ_1 = 0b1
Read configuration register	0x05	RCR contents
General purpose register	Device base address + 0x07	General purpose register data
Lock register 0	0x80	PR-LK0 data
64-bit factory-programmed OTP register	0x81–0x84	Factory OTP register data
64-bit user-programmable OTP register	0x85–0x88	User OTP register data
Lock register 1	0x89	PR-LK1 OTP register lock data
128-bit user-programmable protection registers	0x8A–0x109	OTP register data