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Micron Parallel NOR Flash Embedded Memory (P30-65nm)

JS28F256P30B/TFx, RC28F256P30B/TFx, PC28F256P30B/TFx, RD48F4400P0VBQEx, RC48F4400P0VB0Ex, PC48F4400P0VB0Ex, PF48F4000P0ZB/TQEx

Features

- High performance
  - 100ns initial access for Easy BGA
  - 110ns initial access for TSOP
  - 25ns 16-word asychronous page read mode
  - 52 MHz (Easy BGA) with zero WAIT states and 17ns clock-to-data output synchronous burst read mode
  - 4-, 8-, 16-, and continuous word options for burst mode
  - Buffered enhanced factory programming (BEFP) at 2 MB/s (TYP) using a 512-word buffer
  - 1.8V buffered programming at 1.14 MB/s (TYP) using a 512-word buffer
- Architecture
  - MLC: highest density at lowest cost
  - Asymmetrically blocked architecture
  - Four 32KB parameter blocks: top or bottom configuration
  - 128KB main blocks
  - Blank check to verify an erased block
- Voltage and power
  - V_{CC} (core) voltage: 1.7V to 2.0V
  - V_{CCQ} (I/O) voltage: 1.7V to 3.6V
  - Standy current: 65µA (TYP) for 256Mb
  - 52 MHz continuous synchronous read current: 21mA (TYP), 24mA (MAX)
- Security
  - One-time programmable register: 64 OTP bits, programmed with unique information from Micron; 2112 OTP bits available for customer programming
  - Absolute write protection: $V_{PP} = V_{SS}$
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down
  - Password access
- Software
  - 25µs (TYP) program suspend
  - 25µs (TYP) erase suspend
  - Flash Data Integrator optimized
  - Basic command set and extended function Interface (EFI) command set compatible
  - Common flash interface
- Density and Packaging
  - 56-lead TSOP package (256Mb only)
  - 64-ball Easy BGA package (256Mb, 512Mb)
  - QUAD+ and SCSP packages (256Mb, 512Mb)
  - 16-bit wide data bus
- Quality and reliabilty
  - JESD47 compliant
  - Operating temperature: –40°C to +85°C
  - Minimum 100,000 ERASE cycles per block
  - 65nm process technology

Discrete and MCP Part Numbering Information

Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Note: Not all part numbers listed here are available for ordering.

Table 1: Discrete Part Number Information

Part Number Category	Category Details
Package	JS = 56-lead TSOP, lead free
	PC = 64-ball Easy BGA, lead-free
	RC = 64-ball Easy BGA, leaded
Product Line	28F = Micron Flash memory
Density	256 = 256Mb
Product Family	P30 (VCC = 1.7 to 2.0V; VCCQ = 1.7 to 3.6V)
Parameter Location	B/T = Bottom/Top parameter
Lithography	F = 65nm
Features	*

Note: 1. The last digit is assigned randomly to cover packaging media, features, or other specific configuration information. Sample part number: JS28F256P30BF*

Table 2: MCP Part Number Information

Part Number Category	Category Details
Package	RD = Micron MCP, leaded
	PF = Micron MCP, lead-free
	RC = 64-ball Easy BGA, leaded
	PC = 64-ball Easy BGA, lead-free
Product Line	48F = Micron Flash memory only
Density	0 = No die
	4 = 256Mb
Product Family	P = Micron Flash memory (P30)
	0 = No die
IO Voltage and Chip Configuration	Z = Individual Chip Enables
	V = Virtual Chip Enables
	VCC = 1.7 to 2.0V; VCCQ = 1.7 to 3.6V
Parameter Location	B/T = Bottom/Top parameter
Ballout	Q = QUAD+
	0 = Discrete
Lithography	E = 65nm
Features	*

Note: 1. The last digit is assigned randomly to cover packaging media, features, or other specific configuration information. Sample part number: RC48F4400P0VB0E*

Table 3: Discrete and MCP Part Combinations

Package	Density	Packing Media	Boot Configuration [1]	Part Number
JS	256Mb	Tray	B	JS28F256P30BFE
		Tape and Reel		JS28F256P30BFF
		Tray	T	JS28F256P30TFE
PC	256Mb	Tray	B	PC28F256P30BFE
		Tape and Reel		PC28F256P30BFF
		Tray	T	PC28F256P30TFE
	512Mb (256Mb/256Mb)	Tray	B/T	PC48F4400P0VB0EE
		Tape and Reel		PC48F4400P0VB0EF
PF	256Mb	Tray	B	PF48F4000P0ZBQEF
		Tray	T	PF48F4000P0ZTQEJ
	512Mb (256Mb/256Mb)	Tray	B/T	PF48F4400P0VBQEF
		Tape and Reel		PF48F4400P0VBQEK

Table 3: Discrete and MCP Part Combinations (Continued)

Package	Density	Packing Media	Boot Configuration [1]	Part Number
RC	256Mb	Tray	B	RC28F256P30BFE
		Tray	T	RC28F256P30TFE
		Tape and Reel		RC28F256P30TFF
	512Mb (256Mb/256Mb)	Tray	B/T	RC48F4400P0VB0EJ
RD	512Mb (256Mb/256Mb)	Tray	B/T	RD48F4400P0VBQEJ

Note: 1. Bottom Boot/Top Boot = B/T

Table 4: OTP Feature Part Combinations

Package	Density	Packing Media	Boot Configuration [1]	Part Number
JS	–	–	–	–
PC	256Mb	Tape and Reel	B	PC28F256P30BFR
PF	–	–	–	–
RC	–	–	–	–
RD	–	–	–	–

Notes: 1. This data sheet covers only standard parts. For OTP parts, contact your local Micron representative.
2. Bottom Boot/Top Boot = B/T

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General Description

The Micron Parallel NOR Flash memory is the latest generation of Flash memory devices. Benefits include more density in less space, high-speed interface device, and support for code and data storage. Features include high-performance synchronous-burst read mode, fast asynchronous access times, low power, flexible security options, and three industry-standard package choices. The product family is manufactured using Micron 65nm process technology.

The NOR Flash device provides high performance at low voltage on a 16-bit data bus. Individually erasable memory blocks are sized for optimum code and data storage.

Upon initial power up or return from reset, the device defaults to asynchronous page-mode read. Configuring the read configuration register enables synchronous burst-mode reads. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

In addition to the enhanced architecture and interface, the device incorporates technology that enables fast factory PROGRAM and ERASE operations. Designed for low-voltage systems, the devIce supports READ operations with V_{CC} at the low voltages, and ERASE and PROGRAM operations with V_{PP} at the low voltages or V_{PPH}. Buffered enhanced factory programming (BEFP) provides the fastest Flash array programming performance with V_{PP} at V_{PPH}, which increases factory throughput. With V_{PP} at low voltages, V_{CC} and V_{PP} can be tied together for a simple, ultra low-power design. In addition to voltage flexibility, a dedicated V_{PP} connection provides complete data protection when $V_{PP} \leq V_{PPLK}$.

A command user interface is the interface between the system processor and all internal operations of the device. The device automatically executes the algorithms and timings necessary for block erase and program. A status register indicates ERASE or PROGRAM completion and any errors that may have occurred.

An industry-standard command sequence invokes program and erase automation. Each ERASE operation erases one block. The erase suspend feature enables system software to pause an ERASE cycle to read or program data in another block. Program suspend enables system software to pause programming to read other locations. Data is programmed in word increments (16 bits).

The protection register enables unique device identification that can be used to increase system security. The individual block lock feature provides zero-latency block locking and unlocking. The device includes enhanced protection via password access; this new feature supports write and/or read access protection of user-defined blocks. In addition, the device also provides the full-device OTP security feature.

Virtual Chip Enable Description

The 512Mb device employs a virtual chip enable feature, which combines two 256Mb die with a common chip enable, F1-CE# for QUAD+ packages, or CE# for Easy BGA packages. The maximum address bit is then used to select between the die pair with F1-CE#/CE# asserted, depending upon the package option used. When F1-CE#/CE# is asserted and the maximum address bit is LOW, the lower parameter die is selected; when F1-CE#/CE# is asserted and the maximum address bit is HIGH, the upper parameter die is selected.

Table 5: Virtual Chip Enable Truth Table for 512Mb (QUAD+ Package)

Die Selected	F1-CE#	A24
Lower Param Die	L	L
Upper Param Die	L	H

Table 6: Virtual Chip Enable Truth Table for 512Mb (Easy BGA Packages)

Die Selected	CE#	A25
Lower Param Die	L	L
Upper Param Die	L	H

Figure 1: 512Mb Easy BGA Block Diagram

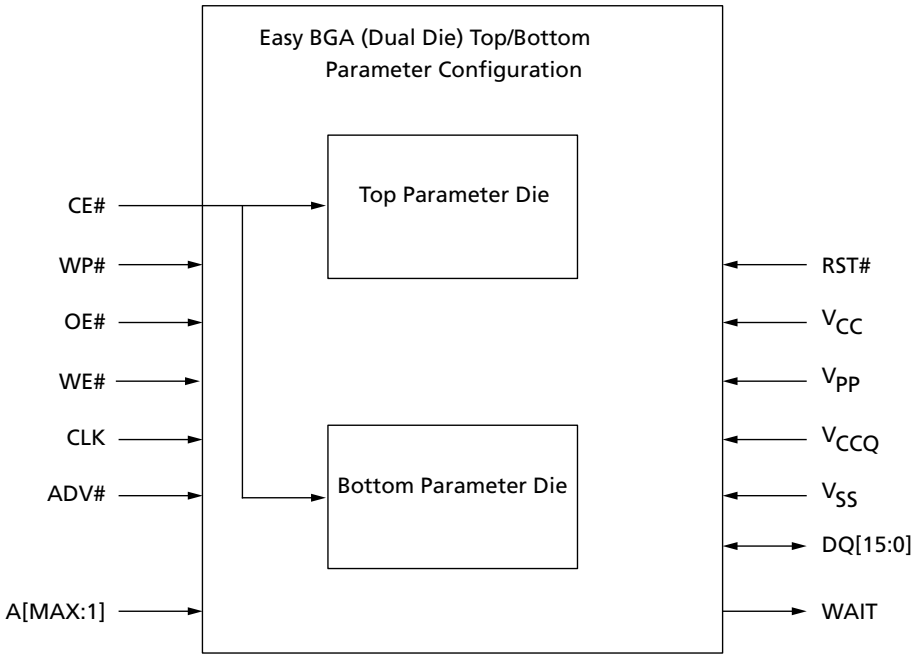
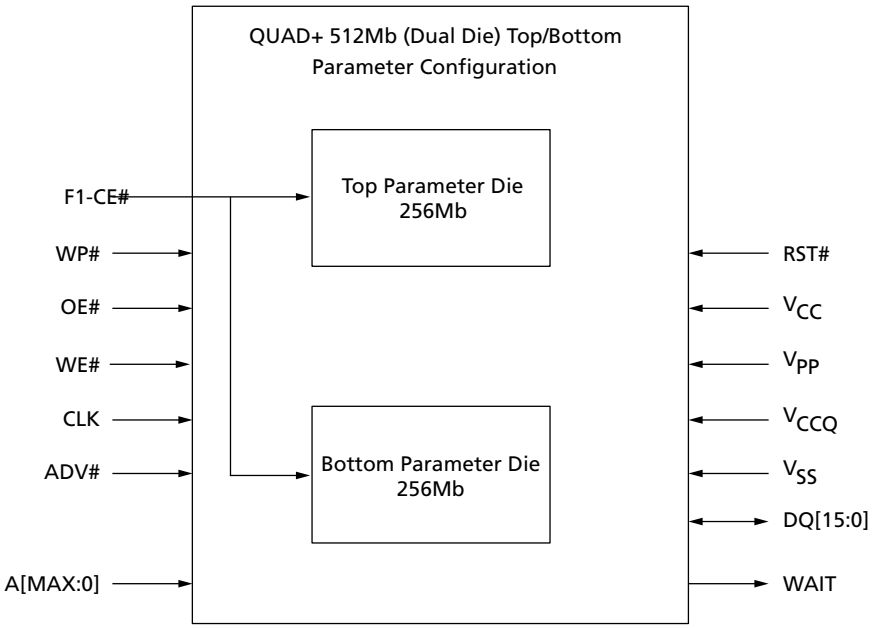
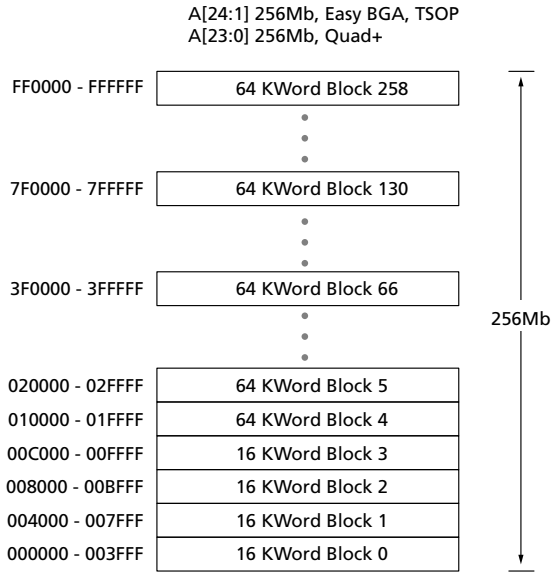


Figure 2: 512Mb QUAD+ Block Diagram

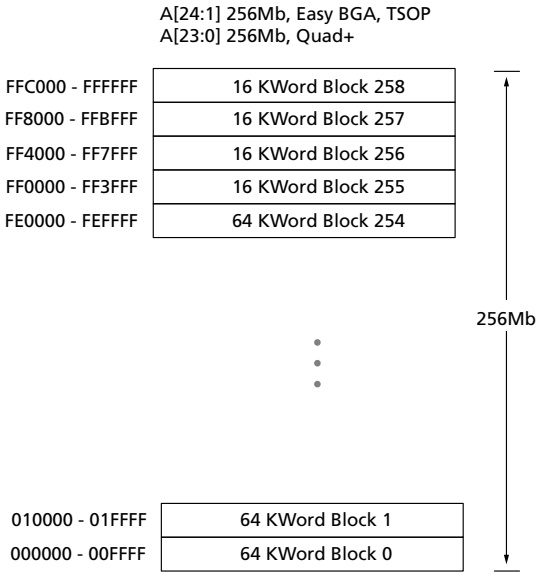


Memory Map

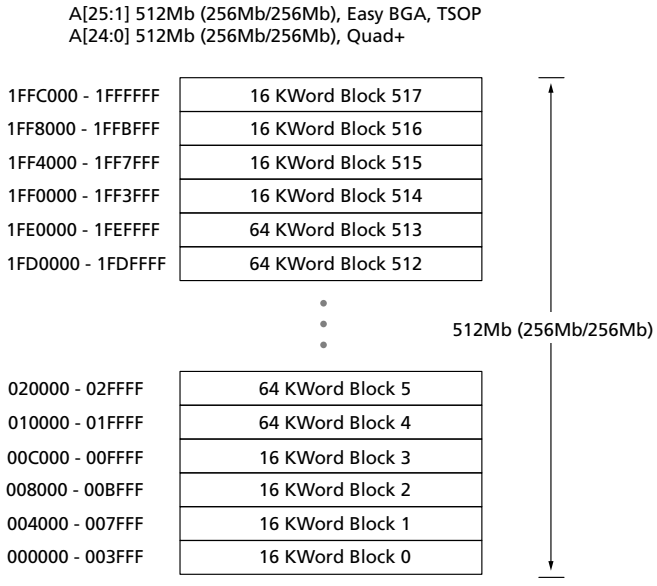
Figure 3: Memory Map – 256Mb and 512Mb



Bottom Boot 256Mb, World-Wide x16 Mode



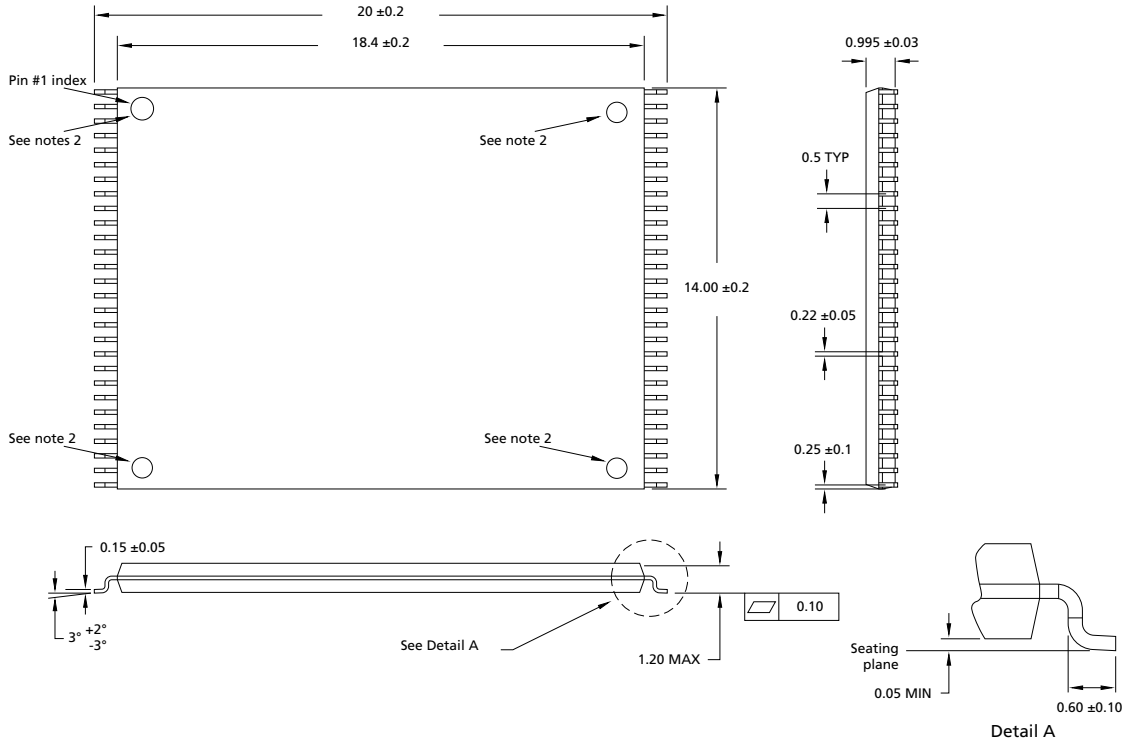
Top Boot 256Mb, World-Wide x16 Mode



512Mb (256Mb/256Mb), World Wide x16 Mode

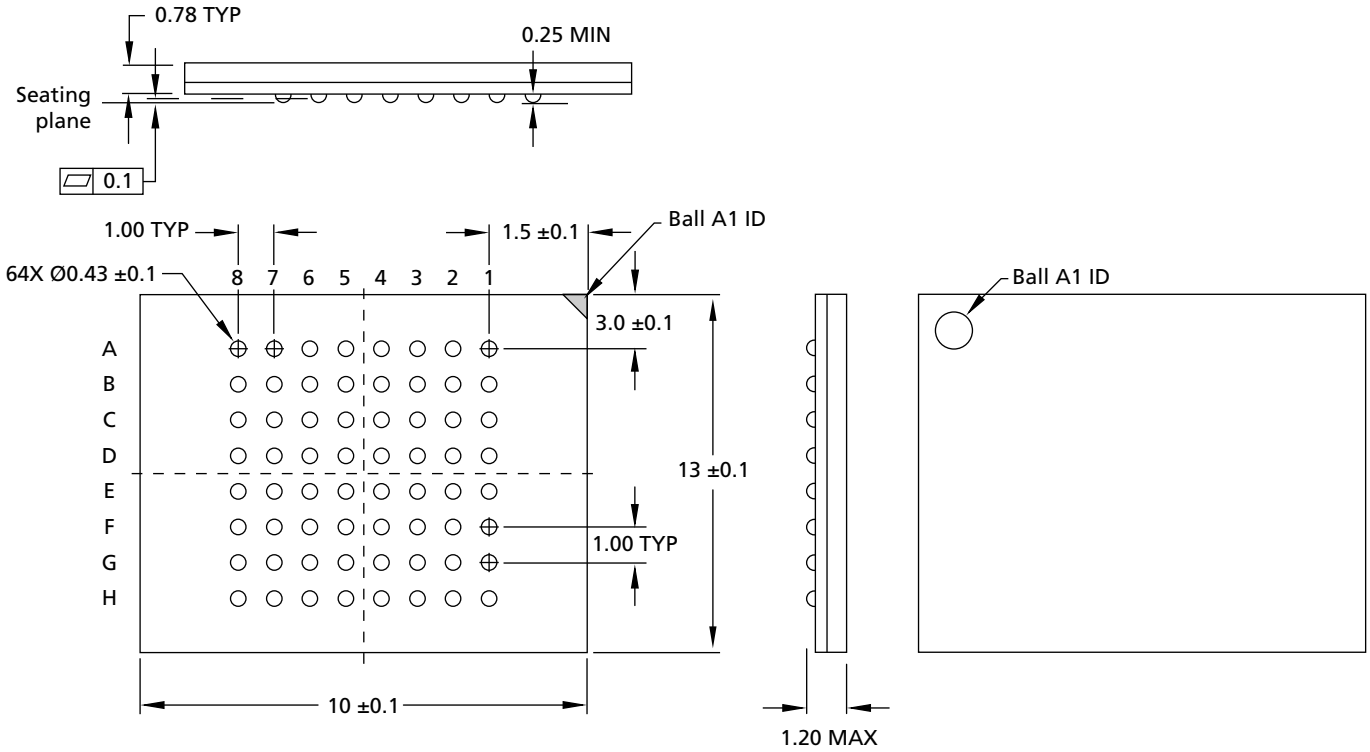
Package Dimensions

Figure 4: 56-Pin TSOP – 14mm x 20mm



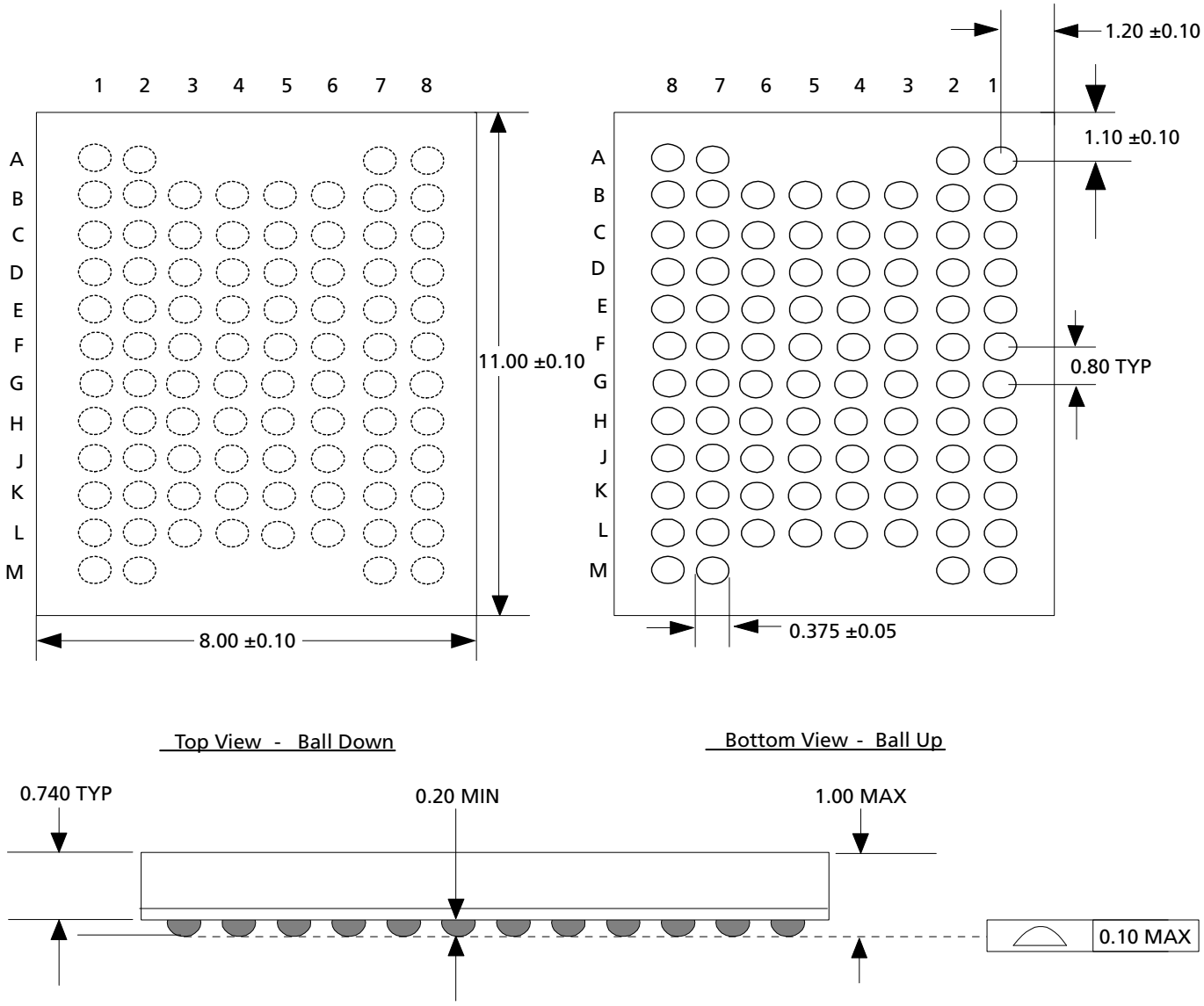
Notes:
1. All dimensions are in millimeters. Drawing not to scale.
2. One dimple on package denotes pin 1; if two dimples, then the larger dimple denotes pin 1. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.
3. For the lead width value of 0.22 ±0.05, there is also a legacy value of 0.15 ±0.05.

Figure 5: 64-Ball Easy BGA – 10mm x 13mm x 1.2mm



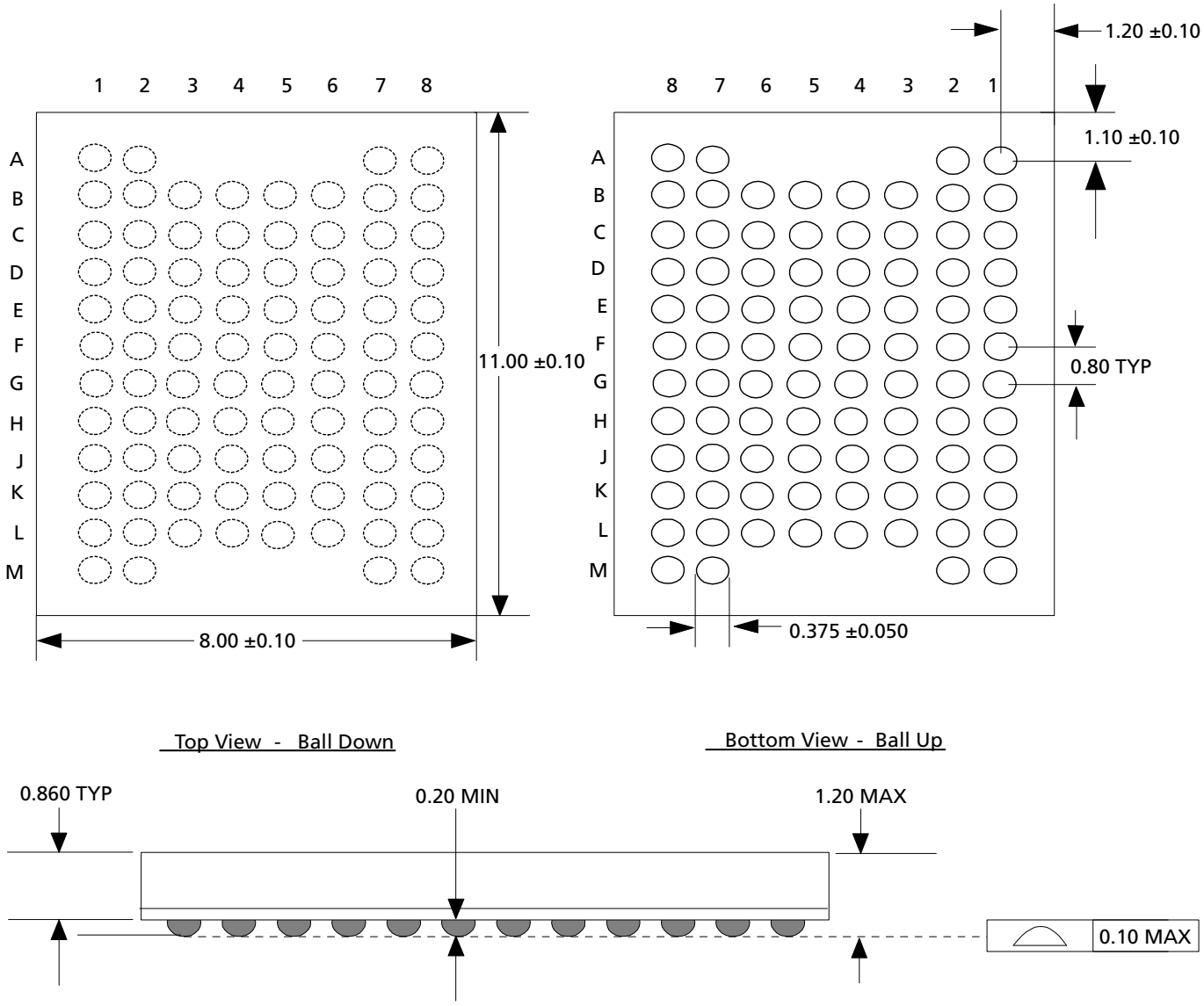
Note: 1. All dimensions are in millimeters. Drawing not to scale.

Figure 6: 88-Ball QUAD+ – 8mm x 11mm x 1.0mm: 256Mb Only



Note: 1. All dimensions are in millimeters. Drawing not to scale.

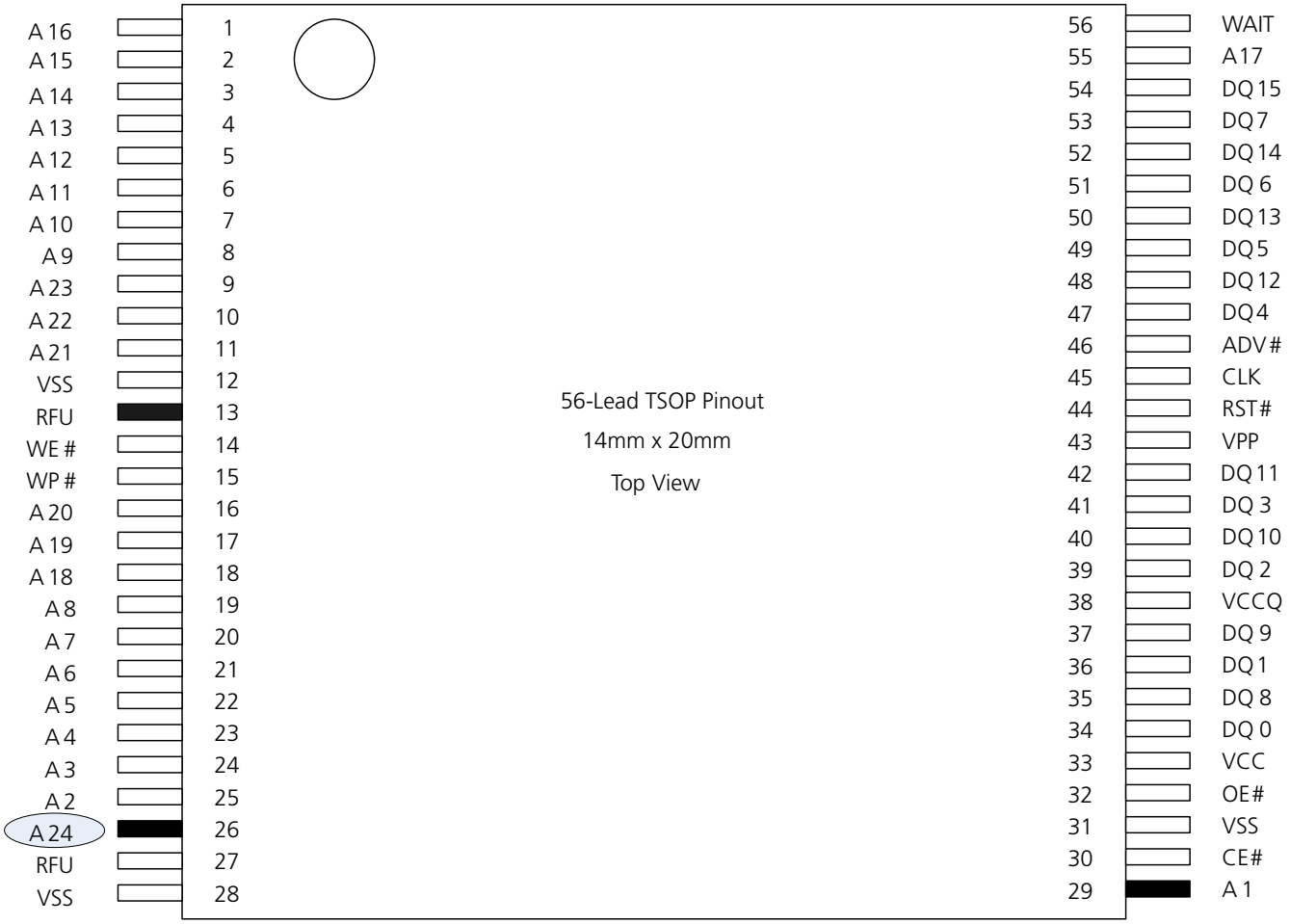
Figure 7: 88-Ball QUAD+ – 8mm x 11mm x 1.2mm: 512Mb Only



Note: 1. All dimensions are in millimeters. Drawing not to scale.

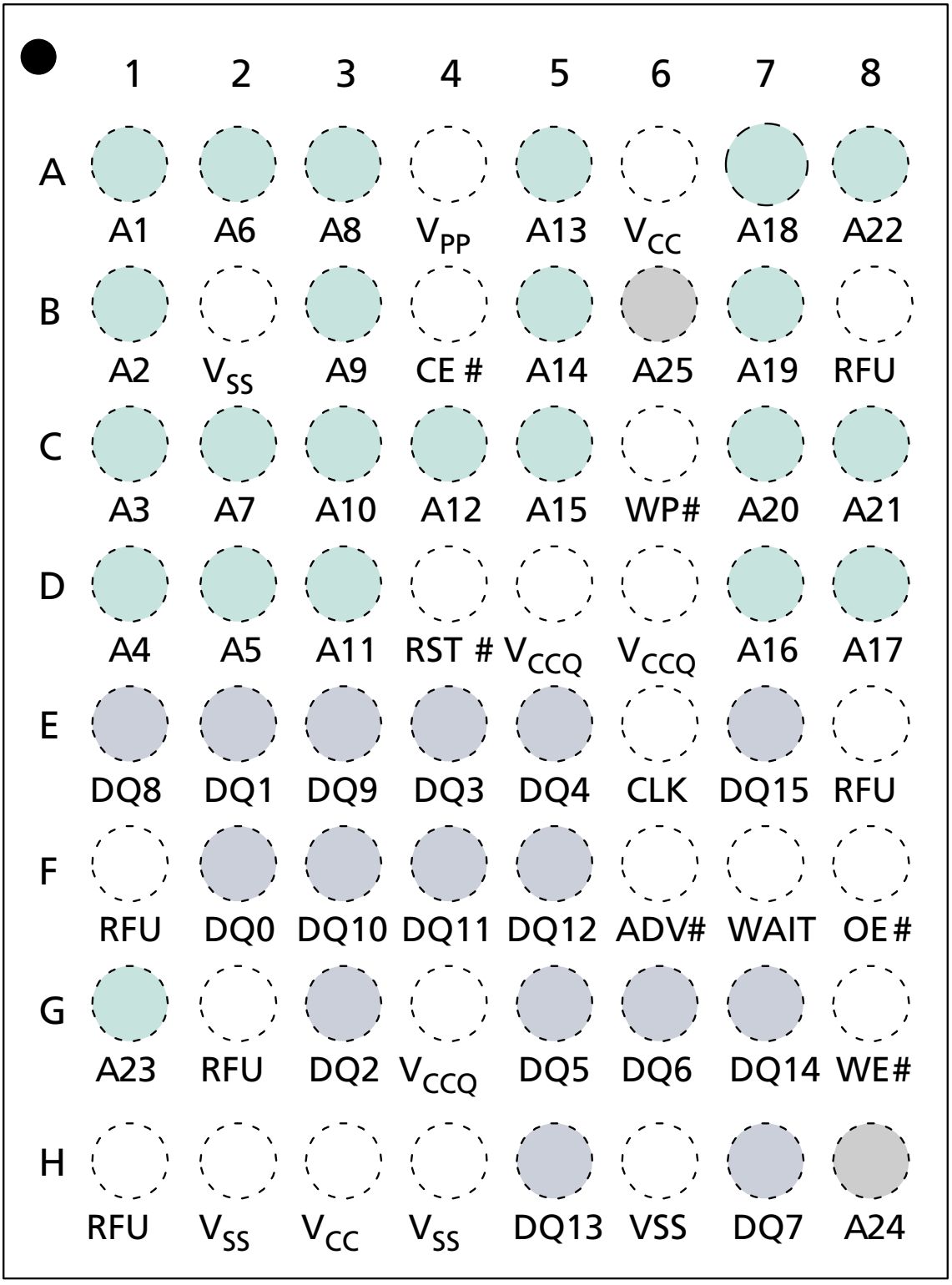
Pinouts and Ballouts

Figure 8: 56-Lead TSOP Pinout – 256Mb



Notes:
1. A1 is the least significant address bit.
2. A24 is valid for 256Mb densities; otherwise, it is a no connect (NC).
3. No internal connection on Pin 13; it may be driven or floated. For legacy designs, it is a V_{CC} pin and can be tied to V_{CC}.
4. One dimple on package denotes Pin 1 which will always be in the upper left corner of the package, in reference to the product mark.

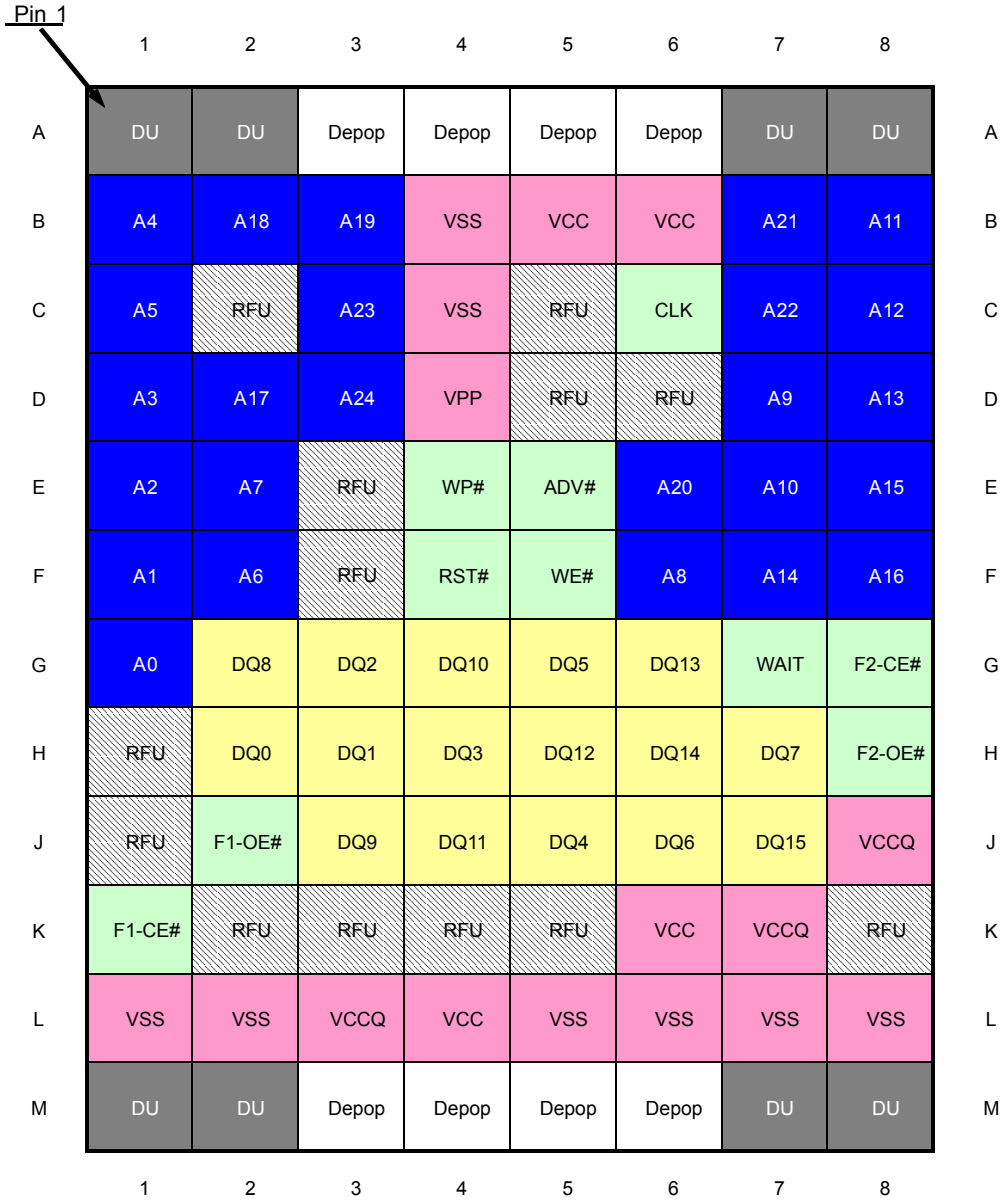
Figure 9: 64-Ball Easy BGA Ballout – 256Mb, 512Mb



Notes: 1. A1 is the least significant address bit.

2. A24 is valid for 256Mb densities and above; otherwise, it is a no connect (NC).
3. A25 is valid for 512Mb densities; otherwise, it is a no connect.
4. One dimple on package denotes A1 pin, which will always be in the upper-left corner of the package, in reference to the product mark.

Figure 10: QUAD+ MCP Ballout



Notes:
1. A23 is valid for 256Mb densities and above; otherwise, it is a no connect.
2. A24 is valid for 512Mb densities and above; otherwise, it is a no connect.
3. F2-CE# and F2-OE# are no connect for all densities.
4. A0 is LSB for Address.

Signal Descriptions

Table 7: TSOP and Easy BGA Signal Descriptions

Symbol	Type	Name and Function
A[MAX:1]	Input	**Address inputs:** Device address inputs. **Note:** Unused active address pins should not be left floating; tie them to V_{CCQ} or V_{SS} according to specific design requirements.
ADV#	Input	**Address valid:** Active LOW input. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. In asynchronous mode, the address is latched when ADV# goes HIGH or continuously flows through if ADV# is held LOW. **Note:** Designs not using ADV# must tie it to V_{SS} to allow addresses to flow through.
CE#	Input	**Chip enable:** Active LOW input. CE# LOW selects the associated die. When asserted, internal control logic, input buffers, decoders, and sense amplifiers are active. When de-asserted, the associated die is deselected, power is reduced to standby levels, data and wait outputs are placed in High-Z. **Note:** CE# must be driven HIGH when device is not in use.
CLK	Input	**Clock:** Synchronizes the device with the system bus frequency in synchronous-read mode. During synchronous READs, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. **Note:**Designs not using CLK for synchronous read mode must tie it to V_{CCQ} or V_{SS}.
OE#	Input	**Output enable:** Active LOW input. OE# LOW enables the device's output data buffers during READ cycles. OE# HIGH places the data outputs and WAIT in High-Z.
RST#	Input	**Reset:** Active LOW input. RST# resets internal automation and inhibits WRITE operations. This provides data protection during power transitions. RST# HIGH enables normal operation. Exit from reset places the device in asynchronous read array mode.
WP#	Input	**Write protect:** Active LOW input. WP# LOW enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the Unlock command. WP# HIGH overrides the lock-down function enabling blocks to be erased or programmed using software commands. **Note:** Designs not using WP# for protection could tie it to V_{CCQ} or V_{SS} without additional capacitor.
WE#	Input	**Write enable:** Active LOW input. WE# controls writes to the device. Address and data are latched on the rising edge of WE# or CE#, whichever occurs first.
V_{PP}	Power/Input	**Erase and program power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system PROGRAM and ERASE operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as $V_{PPL,min}$. V_{PP} must remain above $V_{PPL,min}$ to perform in-system modification. V_{PP} may be 0V during READ operations. V_{PP} can be connected to 9V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9V may reduce block cycling capability.
DQ[15:0]	Input/Output	**Data input/output:** Inputs data and commands during WRITE cycles; outputs data during memory, status register, protection register, and read configuration register reads. Data balls float when the CE# or OE# are de-asserted. Data is internally latched during writes.

Table 7: TSOP and Easy BGA Signal Descriptions (Continued)

Symbol	Type	Name and Function
WAIT	Output	**Wait:** Indicates data valid in synchronous array or non-array burst reads. Read configuration register bit 10 (RCR.10, WT) determines its polarity when asserted. This signal's active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is High-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, this signal indicates invalid data when asserted and valid data when de-asserted. • In asynchronous page mode, and all write modes, this signal is de-asserted.
V_{CC}	Power	**Device core power supply:** Core (logic) source voltage. Writes to the array are inhibited when $V_{CC} \le V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	Power	**Output power supply:** Output-driver source voltage.
V_{SS}	Power	**Ground:** Connect to system ground. Do not float any V_{SS} connection.
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a DU signal.
DU	—	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No connect:** No internal connection; can be driven or floated.

Table 8: QUAD+ SCSP Signal Descriptions

Symbol	Type	Name and Function
A[MAX:0]	Input	**Address inputs:** Device address inputs. 256Mb: A[23:0]; 512Mb: A[24:0]. **Note:** The virtual selection of the 256Mb top parameter die in the dual-die 512Mb configuration is accomplished by setting A24 HIGH. **Note:** The address pins unused in design should not be left floating; tie them to V_{CCQ} or V_{SS} according to specific design requirements. **Note:** When handling the QUAD + SCSP package, note that LSB is A0; address conversion is necessary.
ADV#	Input	**Address valid:** Active LOW input. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. In asynchronous mode, the address is latched when ADV# goes HIGH or continuously flows through if ADV# is held LOW. **Note:** Designs not using ADV# must tie it to V_{SS} to allow addresses to flow through.
F1-CE#	Input	**Flash chip enable:** Active LOW input. F1-CE# LOW selects the associated die. When asserted, internal control logic, input buffers, decoders, and sense amplifiers are active. When de-asserted, the associated die is deselected, power is reduced to standby levels, data and wait outputs are placed in High-Z. **Note:** F1-CE# must be driven HIGH when device is not in use.
CLK	Input	**Clock:** Synchronizes the device with the system bus frequency in synchronous-read mode. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. **Note:** Designs not using CLK for synchronous read mode must tie it to V_{CCQ} or V_{SS}.
F1-OE#	Input	**Output enable:** Active LOW input. F1-OE# LOW enables the device's output data buffers during READ cycles. F1-OE# HIGH places the data outputs and wait in High-Z.

Table 8: QUAD+ SCSP Signal Descriptions (Continued)

Symbol	Type	Name and Function
RST#	Input	**Reset:** Active LOW input. RST# resets internal automation and inhibits WRITE operations. This provides data protection during power transitions. RST# HIGH enables normal operation. Exit from reset places the device in asynchronous read array mode.
WE#	Input	**Write enable:** Active LOW input. WE# controls writes to the device. Address and data are latched on the rising edge of WE# or CE#, whichever occurs first.
WP#	Input	**Write protect:** Active LOW input. WP# LOW enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the UNLOCK command. WP# HIGH overrides the lock-down function enabling blocks to be erased or programmed using software commands. **Note:** Designs not using WP# for protection could tie it to V_{CCQ} or V_{SS} without additional capacitor.
V_{PP}	Power/Input	**Erase and program power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system PROGRAM and ERASE operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as $V_{PPL,min}$. V_{PP} must remain above $V_{PPL,min}$ to perform in-system flash modification. V_{PP} may be 0V during READ operations. V_{PPH} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. V_{PP} can be connected to 9V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9V may reduce block cycling capability.
DQ[15:0]	Input/Output	**Data input/output:** Inputs data and commands during WRITE cycles; outputs data during memory, status register, protection register, and read configuration register reads. Data balls float when the CE# or OE# are de-asserted. Data is internally latched during writes.
WAIT	Output	**Wait:** Indicates data valid in synchronous array or non-array burst reads. Read configuration register bit 10 (RCR.10, WT) determines its polarity when asserted. The active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is High-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, WAIT indicates invalid data when asserted and valid data when de-asserted. • In asynchronous page mode, and all write modes, WAIT is de-asserted.
V_{CC}	Power	**Device core power supply:** Core (logic) source voltage. Writes to the array are inhibited when $V_{CC} \le V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	Power	**Output power supply:** Output driver source voltage.
V_{SS}	Power	**Ground:** Connect to system ground. Do not float any V_{SS} connection.
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a DU signal.
DU	—	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No connect:** No internal connection; can be driven or floated.

Bus Operations

CE# LOW and RST# HIGH enable READ operations. The device internally decodes upper address inputs to determine the accessed block. ADV# LOW opens the internal address latches. OE# LOW activates the outputs and gates selected data onto the I/O bus.

Bus cycles to/from the device conform to standard microprocessor bus operations. Bus operations and the logic levels that must be applied to the device control signal inputs are shown here.

Table 9: Bus Operations

Bus Operation		RST#	CLK	ADV#	CE#	OE#	WE#	WAIT	DQ[15:0]	Notes
READ	Asynchronous	H	X	L	L	L	H	De-asserted	Output	-
	Synchronous	H	Running	L	L	L	H	Driven	Output	-
WRITE		H	X	L	L	H	L	High-Z	Input	1
OUTPUT DISABLE		H	X	X	L	H	H	High-Z	High-Z	2
STANDBY		H	X	X	H	X	X	High-Z	High-Z	2
RESET		L	X	X	X	X	X	High-Z	High-Z	2, 3

Notes:
1. Refer to the Device Command Bus Cycles for valid DQ[15:0] during a WRITE operation.
2. X = "Don't Care" (H or L).
3. RST# must be at V_{SS} ± 0.2V to meet the maximum specified power-down current.

Read

To perform a READ operation, RST# and WE# must be de-asserted while CE# and OE# are asserted. CE# is the device-select control. When asserted, it enables the device. OE# is the data-output control. When asserted, the addressed flash memory data is driven onto the I/O bus.

Write

To perform a WRITE operation, both CE# and WE# are asserted while RST# and OE# are de-asserted. During a WRITE operation, address and data are latched on the rising edge of WE# or CE#, whichever occurs first. The Command Bus Cycles table shows the bus cycle sequence for each of the supported device commands, while the Command Codes and Definitions table describes each command.

Note: WRITE operations with invalid V_{CC} and/or V_{PP} voltages can produce spurious results and should not be attempted.

Output Disable

When OE# is de-asserted, device outputs DQ[15:0] are disabled and placed in High-Z state, WAIT is also placed in High-Z.

Standby

When CE# is de-asserted the device is deselected and placed in standby, substantially reducing power consumption. In standby, the data outputs are placed in High-Z, inde-

pendent of the level placed on OE#. Standby current (I_{CCS}) is the average current measured over any 5ms time interval, 5µs after CE# is de-asserted. During standby, average current is measured over the same time interval 5µs after CE# is de-asserted.

When the device is deselected (while CE# is de-asserted) during a PROGRAM or ERASE operation, it continues to consume active power until the PROGRAM or ERASE operation is completed.

Reset

As with any automated device, it is important to assert RST# when the system is reset. When the system comes out of reset, the system processor attempts to read from the device if it is the system boot device. If a CPU reset occurs with no device reset, improper CPU initialization may occur because the device may be providing status information rather than array data. Micron devices enable proper CPU initialization following a system reset through the use of the RST# input. RST# should be controlled by the same low-true reset signal that resets the system CPU.

After initial power-up or reset, the device defaults to asynchronous read array mode, and the status register is set to 0x80. Asserting RST# de-energizes all internal circuits, and places the output drivers in High-Z. When RST# is asserted, the device shuts down the operation in progress, a process which takes a minimum amount of time to complete. When RST# has been de-asserted, the device is reset to asynchronous read array state.

When device returns from a reset (RST# de-asserted), a minimum wait is required before the initial read access outputs valid data. Also, a minimum delay is required after a reset before a write cycle can be initiated. After this wake-up interval passes, normal operation is restored.

Note: If RST# is asserted during a PROGRAM or ERASE operation, the operation is terminated and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, because the data may have been only partially written or erased.