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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9RS08KA2
MC9RS08KA1

Data Sheet

RS08
Microcontrollers

MC9RS08KA2
Rev. 4
12/2008

freescale.com

MC9RS08KA2 Features

8-Bit RS08 Central Processor Unit (CPU)

- Simplified S08 instruction set with added high-performance instructions
  - LDA, STA, and CLR instructions support the short addressing mode; address $0000 to $001F can be accessed via a single-byte instruction
  - ADD, SUB, INC, and DEC instructions support the tiny addressing mode; address $0000 to $000F can be accessed via a single-byte instruction with reduced instruction cycle
  - Shadow PC register instructions: SHA and SLA
- Pending interrupt indication
- Index addressing via D[X] and X register
- Direct page access to the entire memory map through paging window

Memory

- On-chip Flash EEPROM
  - MC9RS08KA2: 2048 bytes
  - MC9RS08KA1: 1024 bytes
- 63 bytes on-chip RAM

Power-Saving Modes

- Wait and stop
- Wakeup from power-saving modes using real-time interrupt (RTI), KBI, or ACMP

Clock Source

- **ICS** — Trimmable 20-MHz internal clock source
  - Up to 10-MHz internal bus operation
  - 0.2% trimmable resolution, 2% deviation over temperature and voltage range

System Protection

- Computer operating properly (COP) reset running off bus-independent clock source
- Low-voltage detection with reset or stop wakeup

Peripherals

- **MTIM** — 8-bit modulo timer
- **ACMP** — Analog comparator
  - Full rail-to-rail supply operation
  - Option to compare to fixed internal bandgap reference voltage
  - Can operate in stop mode
- **KBI** — Keyboard interrupt ports
  - Three KBI ports in 6-pin package
  - Five KBI ports in 8-pin package

Development Support

- Background debug system
- Breakpoint capability to allow single breakpoint setting during in-circuit debug

Package Options

- 6-pin dual flat no lead (DFN) package
  - Two general-purpose input/output (I/O) pins
  - One general-purpose input pin
  - One general-purpose output pin
- 8-pin plastic dual in-line pin (PDIP) package
  - Four general-purpose input/output (I/O) pins
  - One general-purpose input pin
  - One general-purpose output pin
- 8-pin narrow body SOIC package
  - Four general-purpose input/output (I/O) pins
  - One general-purpose input pin
  - One general-purpose output pin

MC9RS08KA2 Series Data Sheet

Covers: MC9RS08KA2
MC9RS08KA1

MC9RS08KA2
Rev. 4
12/2008

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1.0	04/2006	Initial public release version
2	12/2006	Added MC9RS08KA1
3	09/2007	Corrected Instruction Set Summary LDX ,X row operand to read 0E 0F. Revised the Analog Comparator Electrical Specifications including the ACMP Bandgap reference voltage values. Corrected a transposition in the DFN drawing no. Updated the ICS Characteristic table in the Electricals Appendix to include the ICS factory trim and reference the parameters t_{ir_wu} and t_{fll_wu} that are discussed in the ICS chapter.
4	12/2008	Revised Figure 1-2. Updated “How to Reach Us” information. Changed the mechanical drawing of 6-pin DFN in the Appendix B, “Ordering Information and Mechanical Drawings.”

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Appendix A
Electrical Characteristics

Appendix B
Ordering Information and Mechanical Drawings

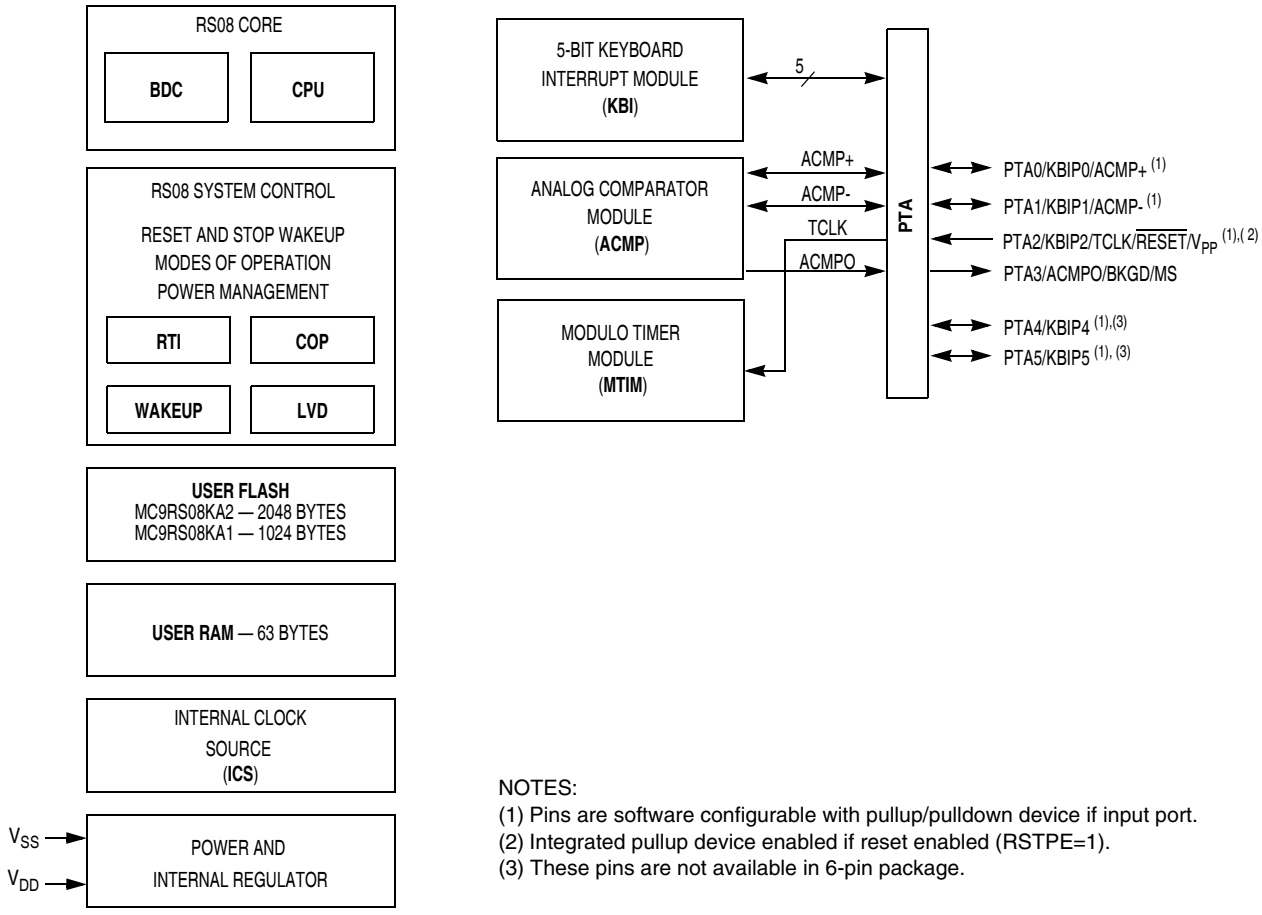
Chapter 1
MC9RS08KA2 Series Device Overview

1.1 Overview

The MC9RS08KA2 Series microcontroller unit (MCU) is an extremely low-cost, small pin count device for home appliances, toys, and small geometry applications. This device is composed of standard on-chip modules including, a very small and highly efficient RS08 CPU core, 63 bytes RAM, 2K bytes Flash, an 8-bit modulo timer, keyboard interrupt, and analog comparator. The device is available in small 6- and 8-pin packages.

1.2 MCU Block Diagram

The block diagram, Figure 1-1, shows the structure of the MC9RS08KA2 Series MCU.



NOTES:
(1) Pins are software configurable with pullup/pulldown device if input port.
(2) Integrated pullup device enabled if reset enabled (RSTPE=1).
(3) These pins are not available in 6-pin package.

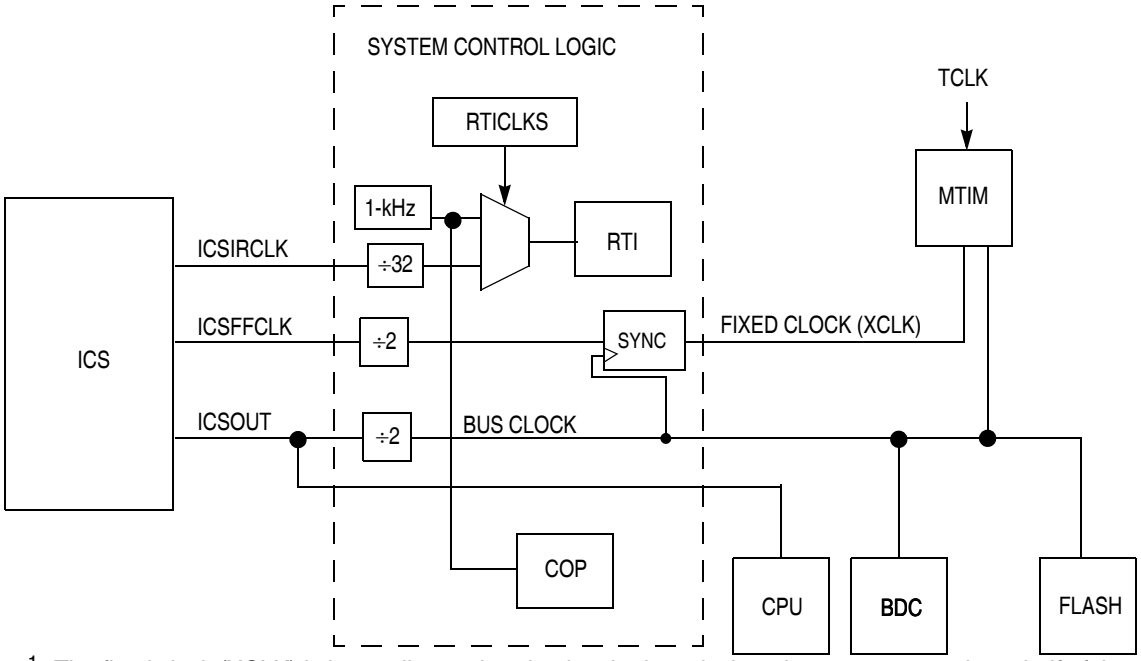
Figure 1-1. MC9RS08KA2 Series Block Diagram

Table 1-1 provides the functional versions of the on-chip modules.

Table 1-1. Block Versions

Module	Version
Analog Comparator (ACMP)	1
Keyboard Interrupt (KBI)	1
Modulo Timer (MTIM)	1
Internal Clock Source (ICS)	1

1.3 System Clock Distribution



1 The fixed clock (XCLK) is internally synchronized to the bus clock and must not exceed one half of the bus clock frequency

Figure 1-2. System Clock Distribution Diagram

Figure 1-2 shows a simplified clock connection diagram for the MCU. The bus clock frequency is half of the ICS output frequency and is used by all of the internal modules.

Chapter 2
Pins and Connections

2.1 Introduction

This chapter describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and a detailed discussion of signals.

2.2 Device Pin Assignment

Figure 2-1 and Figure 2-3 show the pin assignments in the packages available for the MC9RS08KA2 Series.

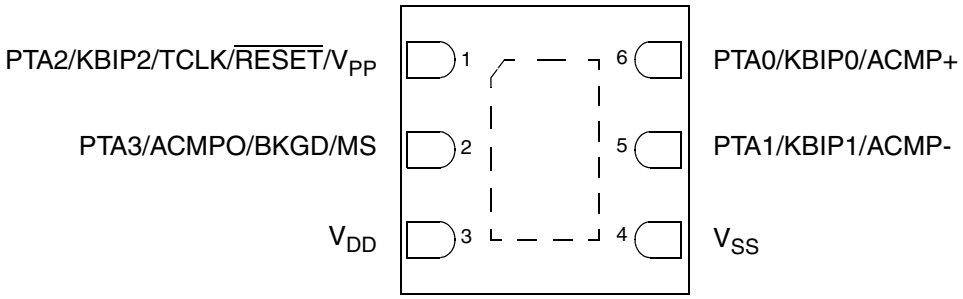


Figure 2-1. MC9RS08KA2 Series in 6-Pin DFN

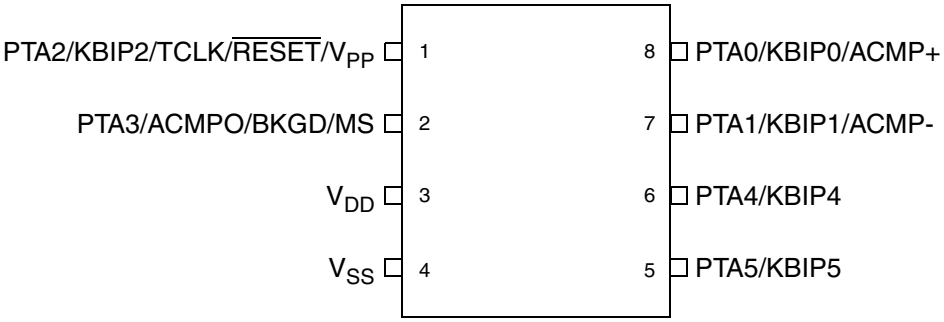


Figure 2-2. MC9RS08KA2 Series in 8-Pin PDIP

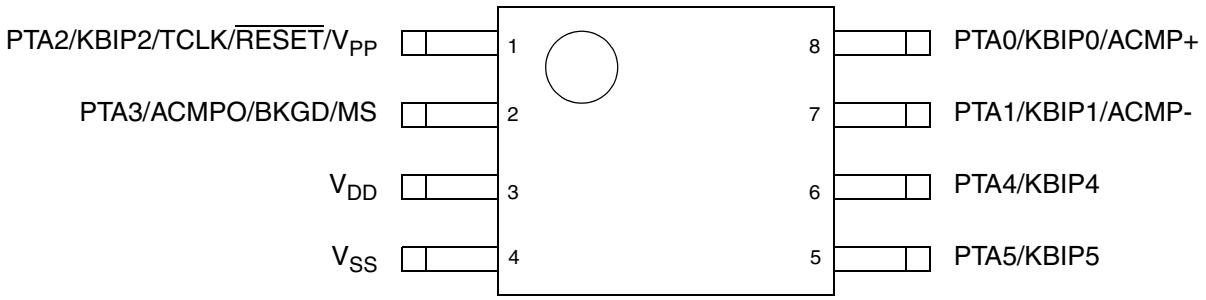


Figure 2-3. MC9RS08KA2 Series in 8-Pin Narrow Body SOIC

2.3 Recommended System Connections

Figure 2-4 shows reference connection for background debug and Flash programming.

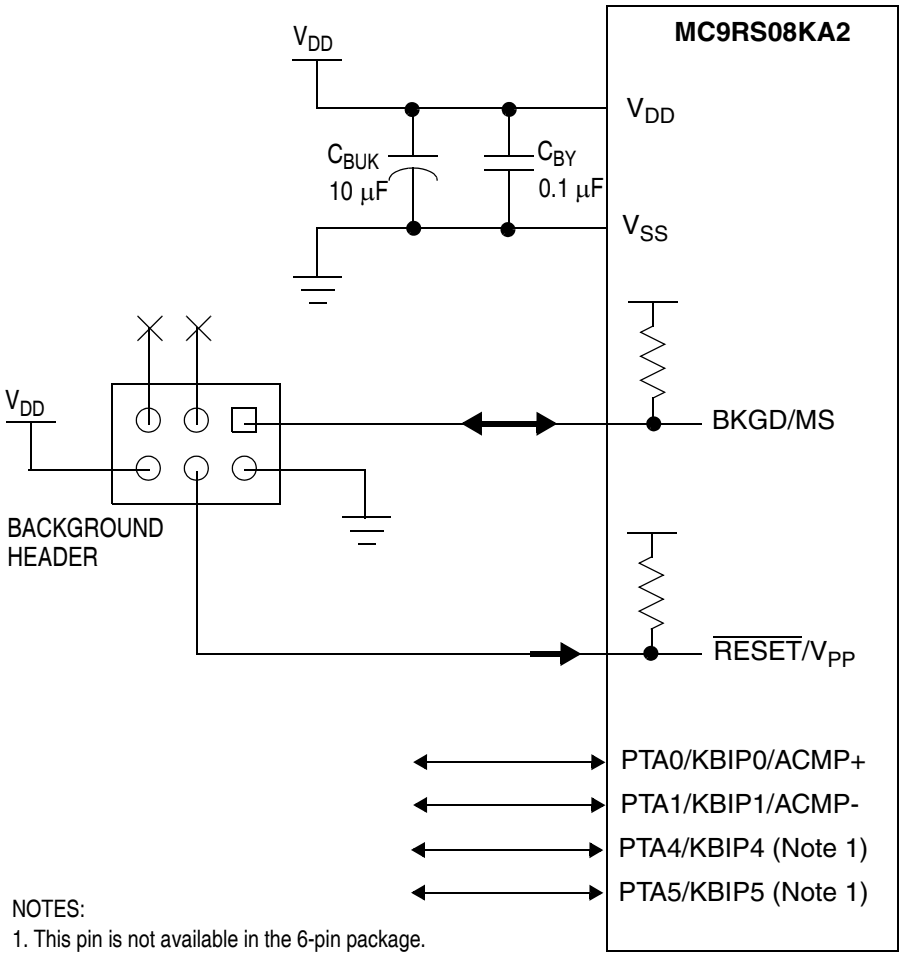


Figure 2-4. Reference System Connection Diagram

2.4 Pin Detail

This section provides a detailed description of system connections.

2.4.1 Power

V_{DD} and V_{SS} are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry and to an internal voltage regulator. The internal voltage regulator provides a regulated lower-voltage source to the CPU and other internal circuitry of the MCU.

Typically, application systems have two separate capacitors across the power pins: a bulk electrolytic capacitor, such as a 10-µF tantalum capacitor, to provide bulk charge storage for the overall system, and a bypass capacitor, such as a 0.1-µF ceramic capacitor, located as near to the MCU power pins as practical to suppress high-frequency noise.

2.4.2 PTA2/KBIP2/TCLK/$\overline{\text{RESET}}$/V_{PP}

After a power-on reset (POR) into user mode, the PTA2/KBIP2/TCLK/$\overline{\text{RESET}}$/V_{PP} pin defaults to a general-purpose input port pin, PTA2. Setting RSTPE in SOPT configures the pin to be the $\overline{\text{RESET}}$ input pin. After configured as $\overline{\text{RESET}}$, the pin will remain as $\overline{\text{RESET}}$ until the next POR. The $\overline{\text{RESET}}$ pin can be used to reset the MCU from an external source when the pin is driven low. When enabled as the $\overline{\text{RESET}}$ pin (RSTPE = 1), the internal pullup device is automatically enabled.

External V_{PP} voltage (typically 12 V, see Section A.10, “FLASH Specifications”) is required on this pin when performing Flash programming or erasing. The V_{PP} connection is always connected to the internal Flash module regardless of the pin function. To avoid over stressing the Flash, external V_{PP} voltage must be removed and voltage higher than V_{DD} must be avoided when Flash programming or erasing is not taking place.

NOTE

This pin does not contain a clamp diode to V_{DD} and should not be driven above V_{DD} when Flash programming or erasing is not taking place.

2.4.3 PTA3/ACMPO/BKGD/MS

The background / mode select function is shared with an output-only pin on PTA3 pin and the optional analog comparator output. While in reset, the pin functions as a mode select pin. Immediately after reset rises, the pin functions as the background pin and can be used for background debug communication. While functioning as a background / mode select pin, this pin has an internal pullup device enabled. To use as an output-only port, BKGDPE in SOPT must be cleared.

If nothing is connected to this pin, the MCU will enter normal operating mode at the rising edge of reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during the power-on-reset, which forces the MCU to active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU’s BDC clock per bit time. The target MCU’s BDC clock equals the bus clock rate; therefore, no significant capacitance should connected to the BKGD/MS pin that could interfere with background serial communications.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise times. Small capacitances from

cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

2.4.4 General-Purpose I/O and Peripheral Ports

The remaining pins are shared among general-purpose I/O and on-chip peripheral functions such as timers and analog comparator. Immediately after reset, all of these pins are configured as high-impedance general-purpose inputs with internal pullup/pulldown devices disabled.

NOTE

To avoid extra current drain from floating input pins, the reset initialization routine in the application program should either enable on-chip pullup/pulldown devices or change the direction of unused pins to outputs.

Table 2-1. Pin Sharing Reference

Pin Name	Direction	Pullup/Pulldown[1]	Alternative Functions[2]	
V_{DD}	—	—	Power	
V_{SS}	—	—	Ground	
PTA0	I/O	SWC	PTA0 KBIP0 ACMP+	General-purpose input/output (GPIO) Keyboard interrupt (stop/wait wakeup only) Analog comparator input
PTA1	I/O	SWC	PTA1 KBIP1 ACMP-	General-purpose input/output (GPIO) Keyboard interrupt (stop/wait wakeup only) Analog comparator input
PTA2	I	SWC[4]	PTA2 KBIP2 TCLK $\overline{\text{RESET}}$ V_{PP}	General-purpose input Keyboard interrupt (stop/wait wakeup only) Modulo timer clock source Reset V_{PP}
PTA3	I/O[3]	—[4]	PTA3 ACMPO BKGD MS	General-purpose output Analog comparator output Background debug data Mode select
PTA4[5]	I/O	SWC	PTA4 KBIP4	General-purpose input/output (GPIO) Keyboard interrupt (stop/wait wakeup only)
PTA5[5]	I/O	SWC	PTA5 KBIP5	General-purpose input/output (GPIO) Keyboard interrupt (stop/wait wakeup only)

1 SWC is software-controlled pullup/pulldown resistor; the register is associated with the respective port.

2 Alternative functions are listed lowest priority first. For example, GPIO is the lowest priority alternative function of the PTA0 pin; ACMP+ is the highest priority alternative function of the PTA0 pin.

3 Output-only when configured as PTA3 function.

4 When PTA2 or PTA3 is configured as $\overline{\text{RESET}}$ or BKGD/MS, respectively, pullup is enabled. When V_{PP} is attached, pullup/pulldown is disabled automatically.

5 This pin is not available in 6-pin package. Enabling either the pullup or pulldown device is recommended to prevent extra current leakage from the floating input pin.

Chapter 3
Modes of Operation

3.1 Introduction

This chapter describes the operating modes of the MC9RS08KA2 Series are described in this chapter. It also details entry into each mode, exit from each mode, and functionality while in each of the modes.

3.2 Features

- Active background mode for code development
- Wait mode:
  - CPU shuts down to conserve power
  - System clocks continue to run
  - Full voltage regulation is maintained
- Stop mode:
  - System clocks are stopped; voltage regulator in standby
  - All internal circuits remain powered for fast recovery

3.3 Run Mode

This is the normal operating mode for the MC9RS08KA2 Series. This mode is selected when the BKGD/MS pin is high at the rising edge of reset. In this mode, the CPU executes code from internal memory with execution beginning at the address $3FFD. A JMP instruction (opcode $BC) with operand located at $3FFE–$3FFF must be programmed for correct reset operation into the user application. The operand defines the location at which the user program will start. Instead of using the vector fetching process as in HC08/S08 families, the user program is responsible for performing a JMP instruction to relocate the program counter to the correct user program start location.

3.4 Active Background Mode

The active background mode functions are managed through the background debug controller (BDC) in the RS08 core. The BDC provides the means for analyzing MCU operation during software development.

Active background mode is entered in any of four ways:

- When the BKGD/MS pin is low during power-on-reset (POR) or immediately after issuing a background debug force reset (BDC_RESET) command
- When a BACKGROUND command is received through the BKGD pin
- When a BGND instruction is executed

- When a BDC breakpoint is encountered

After active background mode is entered, the CPU is held in a suspended state waiting for serial background commands rather than executing instructions from the user application program.

Background commands are of two types:

- Non-intrusive commands, defined as commands that can be issued while the user program is running, can be issued through the BKGD pin while the MCU is in run mode. Non-intrusive commands can also be executed when the MCU is in the active background mode. Non-intrusive commands include:
  - Memory access commands
  - Memory-access-with-status commands
  - BACKGROUND command
- Active background commands, which can be executed only while the MCU is in active background mode, include commands to:
  - Read or write CPU registers
  - Trace one user program instruction at a time
  - Leave active background mode to return to the user application program (GO)

Active background mode is used to program user application code into the Flash program memory before the MCU is operated in run mode for the first time. When the MC9RS08KA2 Series is shipped from the Freescale Semiconductor factory, the Flash program memory is usually erased so there is no program that could be executed in run mode until the Flash memory is initially programmed. The active background mode can also be used to erase and reprogram the Flash memory after it has been previously programmed.

For additional information about the active background mode, refer to the Development Support chapter of this data sheet.

3.5 Wait Mode

Wait mode is entered by executing a WAIT instruction. Upon execution of the WAIT instruction, the CPU enters a low-power state in which it is not clocked. The program counter (PC) is halted at the position where the WAIT instruction is executed. When an interrupt request occurs:

1. MCU exits wait mode and resumes processing.
2. PC is incremented by one and fetches the next instruction to be processed.

It is the responsibility of the user program to probe the corresponding interrupt source that woke the MCU, because no vector fetching process is involved.

While the MCU is in wait mode, not all background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available when the MCU is in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from wait mode and enter active background mode.

Table 3-1 summarizes the behavior of the MCU in wait mode.

Table 3-1. Wait Mode Behavior

Mode	CPU	Digital Peripherals	ICS	ACMP	Regulator	I/O Pins	RTI
Wait	Standby	Optionally on	On	Optionally on	On	States held	Optionally on

3.6 Stop Mode

Stop mode is entered upon execution of a STOP instruction when the STOPE bit in the system option register is set. In stop mode, all internal clocks to the CPU and the modules are halted. If the STOPE bit is not set when the CPU executes a STOP instruction, the MCU will not enter stop mode and an illegal opcode reset is forced.

Table 3-2 summarizes the behavior of the MCU in stop mode.

Table 3-2. Stop Mode Behavior

Mode	CPU	Digital Peripherals	ICS[1]	ACMP[2]	Regulator	I/O Pins	RTI[3]
Stop	Standby	Standby	Optionally on	Optionally on	Standby	States held	Optionally on

1 ICS requires IREFSTEN = 1 and LVDE and LVDSE must be set to allow operation in stop.

2 If bandgap reference is required, the LVDE and LVDSE bits in the SPMSC1 must both be set before entering stop.

3 If the 32-kHz trimmed clock in the ICS module is selected as the clock source for the RTI, LVDE and LVDSE bits in the SPMSC1 must both be set before entering stop.

Upon entering stop mode, all of the clocks in the MCU are halted. The ICS is turned off by default when the IREFSTEN bit is cleared and the voltage regulator is put in standby. The states of all of the internal registers and logic, as well as the RAM content, are maintained. The I/O pin states are held.

Exit from stop is done by asserting $\overline{\text{RESET}}$, any asynchronous interrupt that has been enabled, or the real-time interrupt. The asynchronous interrupts are the KBI pins, LVD interrupt, or the ACMP interrupt.

If stop is exited by asserting the $\overline{\text{RESET}}$ pin, the MCU will be reset and program execution starts at location $3FFD. If exited by means of an asynchronous interrupt or real-time interrupt, the next instruction after the location where the STOP instruction was executed will be executed accordingly. It is the responsibility of the user program to probe for the corresponding interrupt source that woke the CPU.

A separate self-clocked source (≈1 kHz) for the real-time interrupt allows a wakeup from stop mode with no external components. When RTIS = 000, the real-time interrupt function and the 1-kHz source are disabled. Power consumption is lower when the 1-kHz source is disabled, but in that case, the real-time interrupt cannot wake the MCU from stop.

The trimmed 32-kHz clock in the ICS module can also be enabled for the real-time interrupt to allow a wakeup from stop mode with no external components. The 32-kHz clock reference is enabled by setting