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PCA21125

SPI-bus Real-Time Clock and calendar

Rev. 2 — 25 November 2014 Product data sheet

1. General description

The PCA21125 is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low-power consumption and an operating temperature up to 125 °C. Data is transferred via a Serial Peripheral Interface (SPI-bus) with a maximum data rate of 6.0 Mbit/s. Alarm and timer functions are also available with the possibility to generate a wake-up signal on the interrupt pin.

For a selection of NXP Real-Time Clocks, see Table 46 on page 41

2. Features and benefits

- AEC Q100 compliant for automotive applications.
- Provides year, month, day, weekday, hours, minutes, and seconds based on 32.768 kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.3 V to 5.5 V
- Low supply current: typical 0.8 μA at T_{amb} = 25 °C
- 4-line SPI-bus with separate, but combinable data input and output
- Serial interface at V_{DD} = 1.6 V to 5.5 V
- 1 second or 1 minute interrupt output
- Freely programmable timer with interrupt capability
- Freely programmable alarm function with interrupt capability
- Integrated oscillator capacitor
- Internal Power-On Reset (POR)
- Open-drain interrupt pin

3. Applications

- Automotive time keeping
- Metering

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA21125T	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCA21125T/Q900/1	PCA21125T/Q900/1,1	935290408118	tape and reel, 13 inch	1

5. Marking

Table 3. Marking codes

Type number	Marking code
PCA21125T/Q900/1	PC21125

6. Block diagram

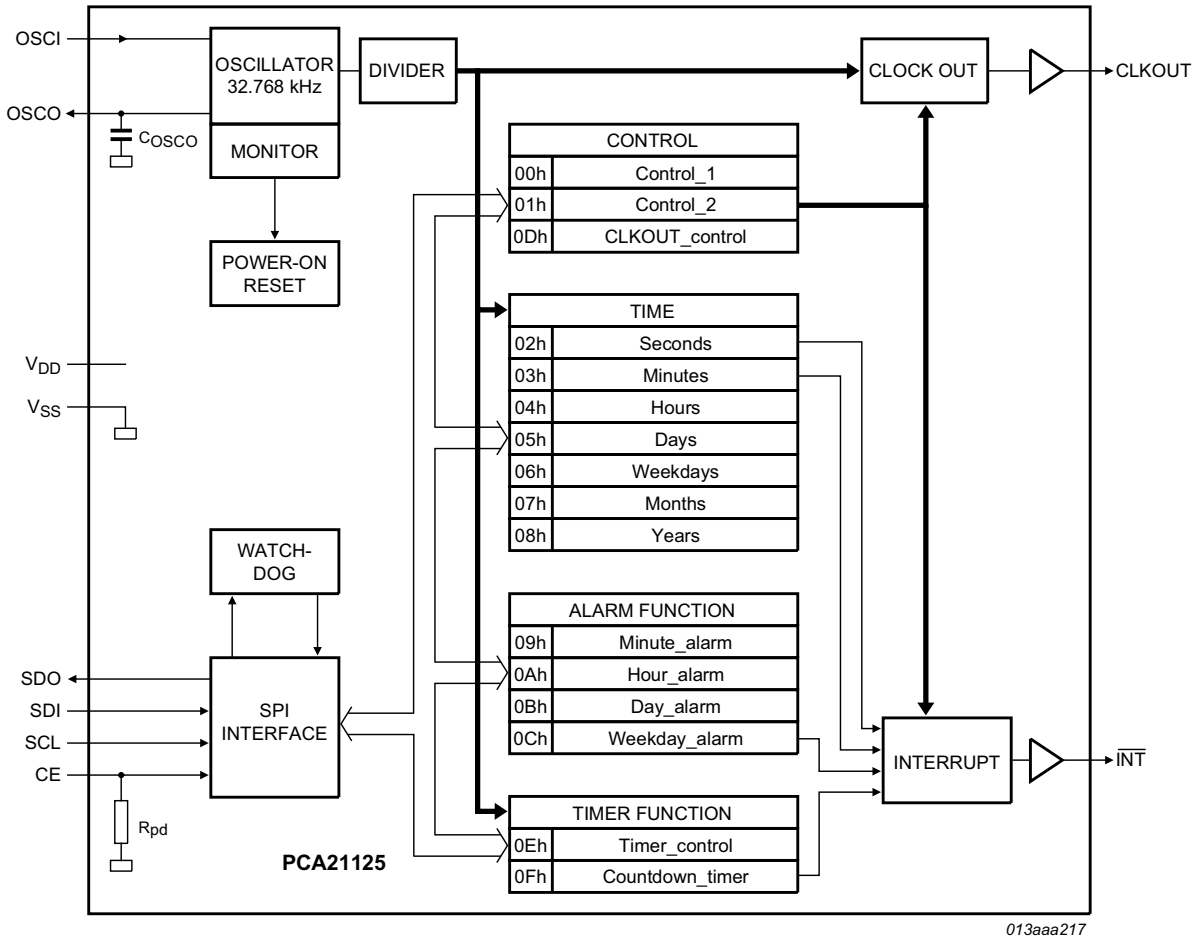


Fig 1. Block diagram of PCA21125

7. Pinning information

7.1 Pinning

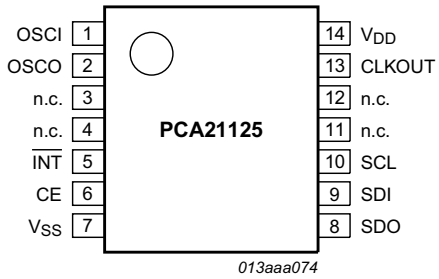


Fig 2. Pin configuration for TSSOP14

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
n.c.	3, 4	not connected; do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
$\overline{INT}$	5	interrupt output (open-drain; active LOW)
CE	6	chip enable input (active HIGH) with 200 kΩ pull-down resistor
V_{SS}	7	ground supply voltage
SDO	8	serial data output, push-pull
SDI	9	serial data input; might float when CE inactive
SCL	10	serial clock input; might float when CE inactive
n.c.	11, 12	not connected; do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
CLKOUT	13	clock output (open-drain)
V_{DD}	14	supply voltage

8. Functional description

The PCA21125 contains 16 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the RTC, a programmable clock output, and a 6 MHz SPI-bus.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented:

- The first two registers at addresses 00h and 01h (Control_1 and Control_2) are used as control and status registers.
- Registers at addresses 02h to 08h (Seconds, Minutes, Hours, Days, Weekdays, Months, Years) are used as counters for the clock function. Seconds, minutes, hours, days, months, and years are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all counters are frozen. Therefore, faulty writing or reading of time and date during a carry condition is prevented.
- Registers at addresses 09h to 0Ch (Minute_alarm, Hour_alarm, Day_alarm, and Weekday_alarm) define the alarm condition.
- The register at address 0Dh (CLKOUT_control) defines the clock output mode.
- Registers at addresses 0Eh and 0Fh (Timer_control and Countdown_timer) are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours (see Table 30). There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control_2 (01h).

8.1 Register overview

The time, date, and alarm registers are encoded in BCD to simplify application use. Other registers are either bit-wise or standard binary.

Table 5. Register overview

Bits labeled - are not implemented and return logic 0 when read. Bit positions labeled N should always be written with logic 0. After reset, all registers are set according to Table 38 on page 26.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control and status registers									
00h	Control_1	EXT_TEST	N	STOP	N	POR_OVRD	12_24	N	N
01h	Control_2	MI	SI	MSF	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	Seconds	RF	SECONDS (0 to 59)						
03h	Minutes	-	MINUTES (0 to 59)						
04h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode				
		-	-	HOURS (0 to 23) in 24-hour mode					
05h	Days	-	-	DAYS (1 to 31)					
06h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		
07h	Months	-	-	-	MONTHS (1 to 12)				
08h	Years	YEARS (0 to 99)							
Alarm registers									
09h	Minute_alarm	AEN_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AEN_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
			-	HOUR_ALARM (0 to 23) in 24-hour mode					
0Bh	Day_alarm	AEN_D	-	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
CLKOUT control register									
0Dh	CLKOUT_control	-	-	-	-	-	COF[2:0]		
Timer registers									
0Eh	Timer_control	TE	-	-	-	-	-	CTD[1:0]	
0Fh	Countdown_timer	T[7:0]							

8.2 Control and status registers

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0[1]	normal mode	Section 8.8
		1	external clock test mode	
6	N	0	unused	-
5	STOP	0[1]	RTC source clock runs	Section 8.9
		1	RTC clock is stopped[2]	
4	N	0	unused	-
3	POR_OVRD	0	Power-On Reset Override facility is disabled; **Remark:** set logic 0 for normal operation	Section 8.10.1
		1[1]	Power-On Reset Override sequence reception enabled	
2	12_24	0[1]	24-hour mode selected	Table 11 and Table 19
		1	12-hour mode selected	
1 to 0	N	00	unused	-

[1] Default value.

[2] CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available; divider chain flip-flops are asynchronously set logic 0.

8.2.2 Register Control_2

Table 7. Control_2 - control and status register 2 (address 01h) bit description

Bit	Symbol	Value	Description	Reference
7	MI	0[1]	minute interrupt disabled	Section 8.6.1
		1	minute interrupt enabled	
6	SI	0[1]	second interrupt disabled	Section 8.6.1
		1	second interrupt enabled	
5	MSF	0[1]	no minute or second interrupt generated	Section 8.6.1
		1	flag set when minute or second interrupt generated	
4	TI_TP	0[1]	interrupt pin follows TF and MSF (see Figure 9)	Section 8.6 et seq. and Section 8.7 et seq.
		1	interrupt pin generates a pulse	
3	AF	0[1]	no alarm interrupt generated	Section 8.4.5
		1	flag set when alarm triggered; **Remark:** flag must be cleared to clear interrupt	
2	TF	0[1]	no countdown timer interrupt generated	Section 8.6 et seq. and Section 8.7 et seq.
		1	flag set when countdown timer interrupt generated	
1	AIE	0[1]	no interrupt generated from alarm flag	Section 8.7.3
		1	interrupt generated when alarm flag set	
0	TIE	0[1]	no interrupt generated from countdown timer flag	Section 8.7
		1	interrupt generated when countdown timer flag set	

[1] Default value.

8.3 Time and date registers

Most of these registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for register Seconds in Table 9.

Loading these registers with values outside of the given range results in unpredictable time and date generation (see Figure 3 “Data flow of the time function”).

8.3.1 Register Seconds

Table 8. Seconds - seconds and clock integrity status register (address 02h) bit description

Bit	Symbol	Value	Description
7	RF	0	clock integrity is guaranteed
		1[1]	clock integrity is not guaranteed; chip reset has occurred since flag was last cleared
6 to 4	SECONDS	0 to 5	ten’s place
3 to 0		0 to 9	unit place

[1] Start-up value.

Table 9. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten’s place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.3.2 Register Minutes

Table 10. Minutes - minutes register (address 03h) bit description

Bit	Symbol	Value	Description
7	-	0	unused
6 to 4	MINUTES	0 to 5	ten’s place
3 to 0		0 to 9	unit place

8.3.3 Register Hours

Table 11. Hours - hours register (address 04h) bit description

Bit	Symbol	Value	Description
7 to 6	-	00	unused
12-hour mode[1]			
5	AMPM	0	indicates AM
		1	indicates PM
4	HOURS	0 to 1	ten's place
3 to 0		0 to 9	unit place
24-hour mode[1]			
5 to 4	HOURS	0 to 2	ten's place
3 to 0		0 to 9	unit place

[1] Hour mode is set by bit 12_24 in register Control_1 (see Table 6).

8.3.4 Register Days

Table 12. Days - days register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	00	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCA21125 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

8.3.5 Register Weekdays

Table 13. Weekdays - weekdays register (address 06h) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday, values see Table 14

Table 14. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be reassigned by the user.

8.3.6 Register Months

Table 15. Months - months register (address 07h) bit description

Bit	Symbol	Value	Description
7 to 5	-	000	unused
4	MONTHS	0 to 1	ten's place
3 to 0		0 to 9	unit place

Table 16. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.3.7 Register Years

Table 17. Years - years register (08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

8.3.8 Setting and reading the time

Figure 3 shows the data flow and data dependencies starting from the 1 Hz clock tick.

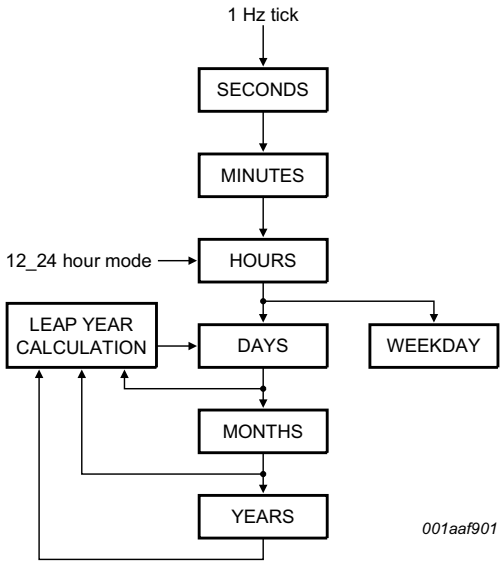


Fig 3. Data flow of the time function

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 4).

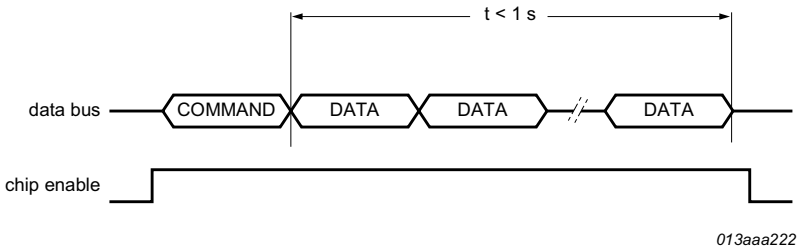


Fig 4. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

8.4 Alarm registers

When one or several alarm registers are loaded with a valid minute, hour, day, or weekday value and its corresponding alarm enable bit (AEN_X) is logic 0, then that information is compared with the current minute, hour, day, and weekday value.

8.4.1 Register Minute_alarm

Table 18. Minute_alarm - minute alarm register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.4.2 Register Hour_alarm

Table 19. Hour_alarm - hour alarm register (address 0Ah) bit description

Bit	Symbol	Value	Description
7	AEN_H	0	hour alarm is enabled
		1[1]	hour alarm is disabled
6	-	0	unused
12-hour mode[2]			
5	AMPM	0	indicates AM
		1	indicates PM
4	HOUR_ALARM	0 to 1	ten's place
3 to 0		0 to 9	unit place
24-hour mode[2]			
5 to 4	HOURS	0 to 2	ten's place
3 to 0		0 to 9	unit place

[1] Default value.

[2] Hour mode is set by bit 12_24 in register Control_1 (see Table 6).

8.4.3 Register Day_alarm

Table 20. Day_alarm - day alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	0	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.4.4 Register Weekday_alarm

Table 21. Weekday_alarm - weekday alarm register (address 0Ch) bit description

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	0000	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information coded in BCD format

[1] Default value.

8.4.5 Alarm flag

By clearing the MSB, AEN_X (Alarm Enable), of one or more of the alarm registers the corresponding alarm condition(s) are active. When an alarm occurs, AF (register Control_2, see Table 7) is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared by command.

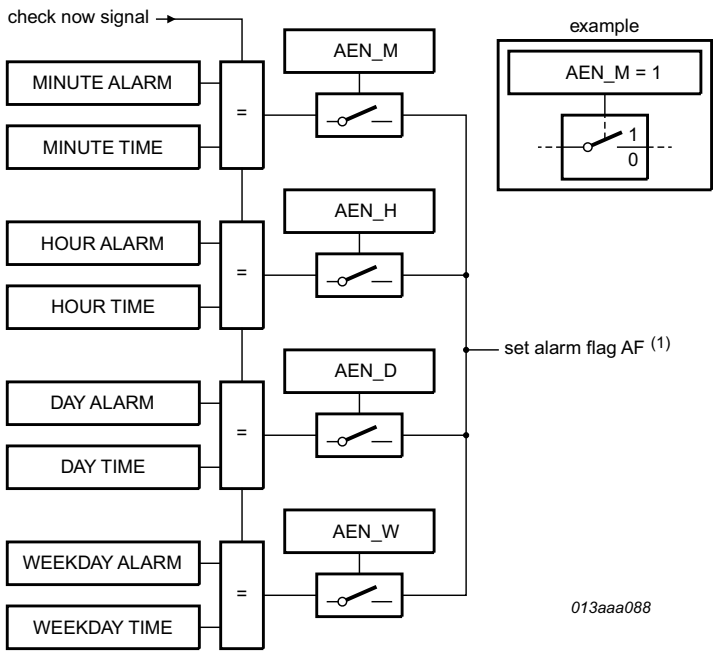


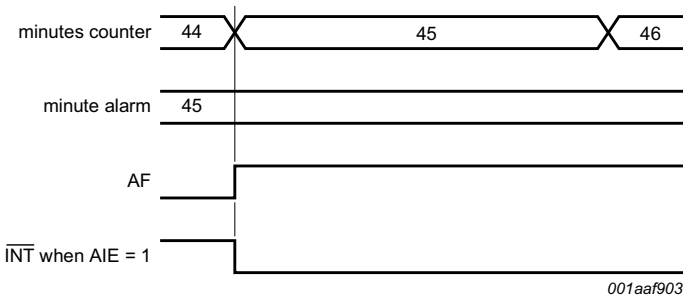
Fig 5. Alarm function block diagram

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day, or weekday, and its corresponding Alarm Enable bit (AEN_X) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (register Control_2, see Table 7). If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF remains set until cleared by the interface. Once AF has been cleared, it is only set again when the time increments to match the alarm condition once more. Alarm registers which have their AEN_X bit logic 1 are ignored.

Generation of interrupts from the alarm function is described in Section 8.7.3.

Figure 6, Table 22 and Table 23 show an example for clearing bit AF, but leaving bit MSF and bit TF unaffected. The flags are cleared by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly rewriting these bits has no influence on the functional behavior.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 6. Alarm flag timing

To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Table 22. Flag location in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 23 shows what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

Table 23. Example to clear only AF (bit 3) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	1	-	0	1	-	-

8.5 Register CLKOUT_control and clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by control bits COF[2:0] in register CLKOUT_control (0Dh); see Table 24. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Table 24. CLKOUT_control - CLKOUT control register (address 0Dh) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	unused
2 to 0	COF[2:0]	see Table 25	frequency output at pin CLKOUT

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is LOW.

The duty cycle of the selected clock is not controlled, but due to the nature of the clock generation, all clock frequencies, except 32.768 kHz, have a duty cycle of 50 : 50.

The stop function can also affect the CLKOUT signal, depending on the selected frequency. When STOP is active, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped. For more details, see Section 8.9.

Table 25. CLKOUT frequency selection

Bits COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1] (%)	Effect of STOP
000[2]	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW
101	1024	50 : 50	CLKOUT = LOW
110	1	50 : 50	CLKOUT = LOW
111	CLKOUT = LOW		

[1] Duty cycle definition: HIGH-level time (%) : LOW-level time (%).

[2] Default value.

8.6 Timer registers

The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours (see Table 30). There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute.

Registers Control_2 (01h), Timer_control (0Eh), and Countdown_timer (0Fh) are used to control the timer function and output.

Table 26. Timer_control - timer control register (address 0Eh) bit description

Bit	Symbol	Value	Description	Reference
7	TE	0[1]	countdown timer is disabled	Section 8.6.2
		1	countdown timer is enabled	
6 to 2	-	00000	unused	
1 to 0	CTD[1:0]	00	4.096 kHz countdown timer source clock	
		01	64 Hz countdown timer source clock	
		10	1 Hz countdown timer source clock	
		11[1]	$^1/_{60}$ Hz countdown timer source clock	

[1] Default value.

Table 27. Countdown_timer - countdown timer register (address 0Fh) bit description

Bit	Symbol	Value	Description	Reference
7 to 0	T[7:0]	0h to FFh	countdown timer value[1]	Section 8.6.2

[1] Countdown period in seconds: $CountdownPeriod = \frac{T}{SourceClockFrequency}$ where T is the countdown value.

8.6.1 Second and minute interrupt

The second and minute interrupts (bits SI and MI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently of one another, however a minute interrupt enabled on top of a second interrupt is not distinguishable since it occurs at the same time; see Figure 7.

The minute and second flag (MSF) is set logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the $\overline{INT}$ pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an $\overline{INT}$ pulse will still be generated.

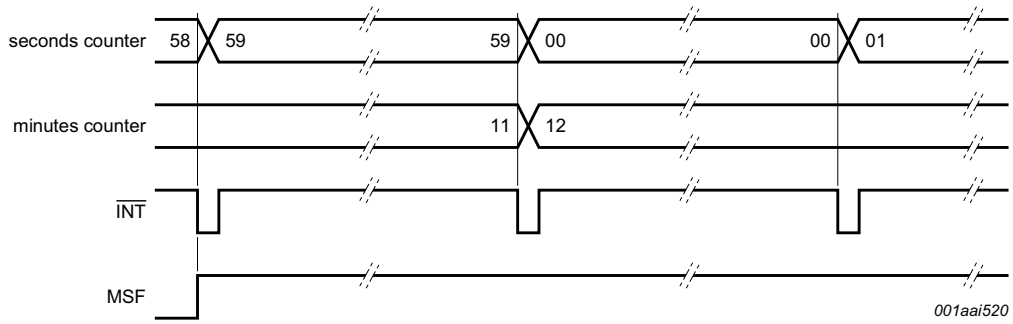
Table 28. Effect of bits MI and SI on $\overline{INT}$ generation

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	no interrupt generated
1	0	an interrupt once per minute
0	1	an interrupt once per second
1	1	an interrupt once per second

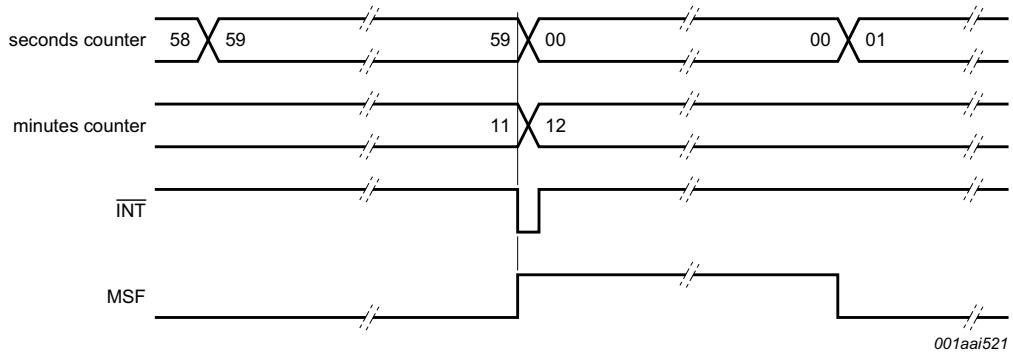
Table 29. Effect of bits MI and SI on bit MSF

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	MSF never set
1	0	MSF set when **minutes** counter increments[1]
0	1	MSF set when **seconds** counter increments
1	1	MSF set when **seconds** counter increments

[1] If bit MI = 1 and bit SI = 0, bit MSF is cleared automatically after 1 second.



a. $\overline{INT}$ and MSF when SI enabled (MSF flag not cleared after an interrupt)



b. $\overline{INT}$ and MSF when only MI enabled

Bit TI_TP is set logic 1 resulting in $^{1}/_{64}$ Hz wide interrupt pulse.

Fig 7. $\overline{INT}$ example for bits SI and MI

The purpose of the flag is to allow the controlling system to interrogate the PCA21125 and identify the source of the interrupt such as the minute/second or countdown timer.

8.6.2 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $^{1}/_{60}$ Hz) and enables or disables the timer.

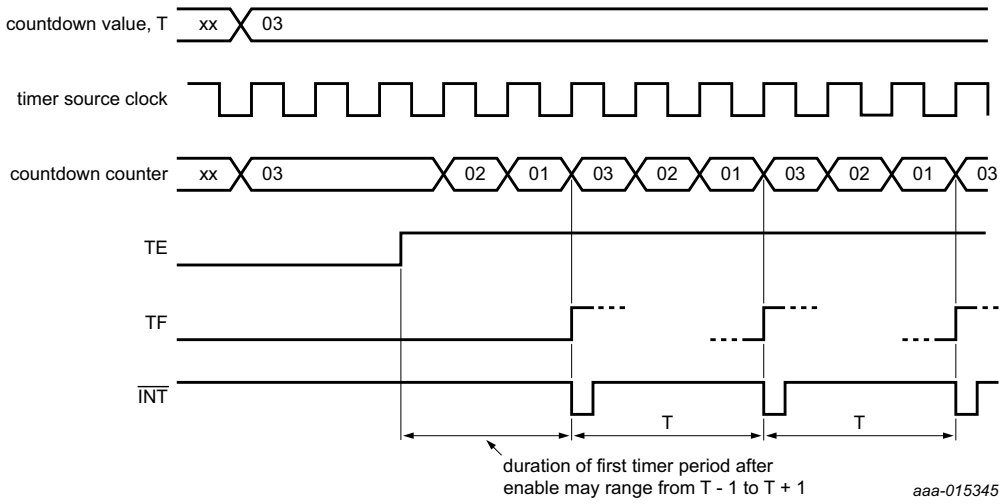
Table 30. CTD[1:0] for timer frequency selection and countdown timer durations

CTD[1:0]	Timer source clock frequency	Delay	
		Minimum timer duration T = 1	Maximum timer duration T = 255
00	4.096 kHz	244 μs	62.256 ms
01	64 Hz	15.625 ms	3.984 s
10	1 Hz	1 s	255 s
11	$^{1}/_{60}$ Hz	60 s[1]	4 h 15 min

[1] When not in use, CTD[1:0] must be set to $^{1}/_{60}$ Hz for power saving.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency results in a corresponding deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value T. Loading the counter with 0 effectively stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF in register Control_2, see Table 7) will be set and the counter automatically reloads and starts the next timer period. Reading the timer returns the current value of the countdown counter; see Figure 8.



In the example, it is assumed that the timer flag is cleared before the next countdown period expires and that the $\overline{INT}$ is set to pulsed mode.

Fig 8. General countdown timer behavior

If a new value of T is written before the end of the current timer period, then this new value takes immediate effect. It is not recommended to change T without first disabling the counter (by setting bit TE = 0). The update of T is asynchronous with the timer clock, therefore changing it without setting bit TE = 0 results in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value T will however be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ is generated, if this mode is enabled. See Section 8.7.2 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous with the timer source clock. Subsequent timer periods have no such delay. The amount of delay for the first timer period depends on the chosen source clock; see Table 31.

Table 31. First period delay for timer counter value T

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	T	T + 1
64 Hz	T	T + 1
1 Hz	(T – 1) + $^1/_{64}$ Hz	T + $^1/_{64}$ Hz
$^1/_{60}$ Hz	(T – 1) + $^1/_{64}$ Hz	T + $^1/_{64}$ Hz

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt ($\overline{INT}$). The interrupt can be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output can be disabled with bit TIE.

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

8.6.3 Timer flags

When a minute or second interrupt occurs, bit MSF (register Control_2, see Table 7) is set logic 1. Similarly, at the end of a timer countdown bit TF is set logic 1. These bits maintain their value until overwritten by command. If both countdown timer and minute/second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Three examples are given for clearing the flags. Flags MSF and TF are cleared by a write command, therefore bits 7, 6, 4, 1, and 0 must be written with their previous values. Repeatedly rewriting these bits has no influence on the functional behavior.

Table 32. Flag location in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 33, Table 34, and Table 35 show what instruction must be sent to clear the appropriate flag.

Table 33. Example to clear only TF (bit 2) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	1	-	1	0	-	-

Table 34. Example to clear only MSF (bit 5) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	0	-	1	1	-	-

Table 35. Example to clear both TF and MSF (bits 2 and 5) in register Control_2

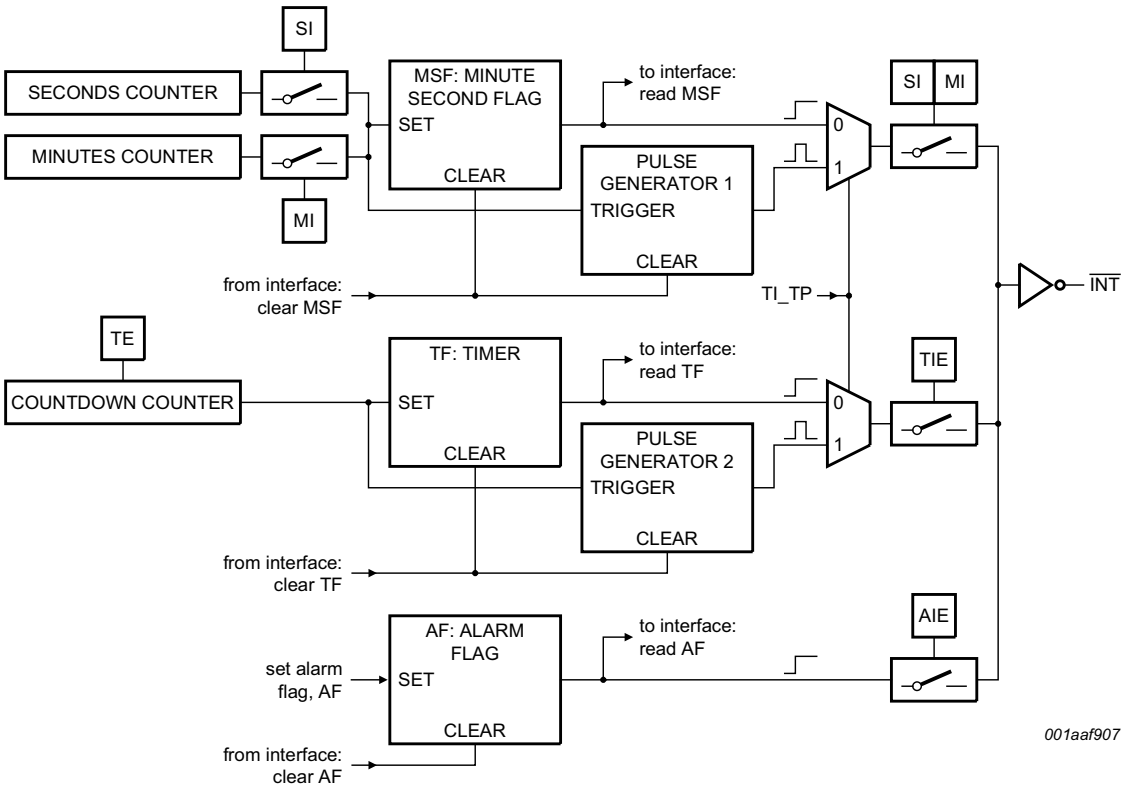
Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	0	-	1	0	-	-

Clearing the alarm flag (bit AF) operates in the same way; see Section 8.4.5.

8.7 Interrupt output

An active LOW interrupt signal is available at pin $\overline{INT}$. Operation is controlled via the bits of register Control_2. Interrupts can be sourced from three places: second/minute timer, countdown timer, and alarm function.

Bit TI_TP configures the timer generated interrupts to be either a pulse or to follow the status of the interrupt flags (bits TF and MSF).



When bits SI, MI, TIE and AIE are all disabled, pin $\overline{INT}$ remains high-impedance.

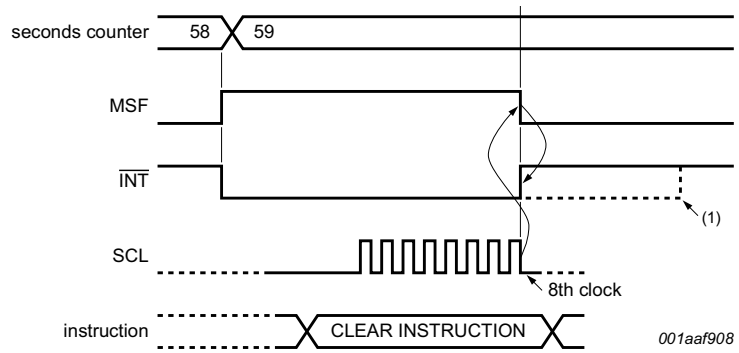
Fig 9. Interrupt scheme

Remark: Note that the interrupts from the three groups are wired-OR, meaning they will mask one another; see Figure 9.

8.7.1 Minute and second interrupts

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of $^1/_{64}$ second duration.

If the MSF flag is clear before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing; see Figure 10. Instructions for clearing MSF are given in Section 8.6.3.



(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1).

Fig 10. Example of shortening the $\overline{INT}$ pulse by clearing the MSF flag

The timing shown for clearing bit MSF in Figure 10 is also valid for the non-pulsed interrupt mode, i.e., when bit TI_TP = 0, where the pulse can be shortened by setting both bits MI and SI logic 0.

8.7.2 Countdown timer interrupts

Generation of interrupts from the countdown timer is controlled via bit TIE (register Control_2, see Table 7).

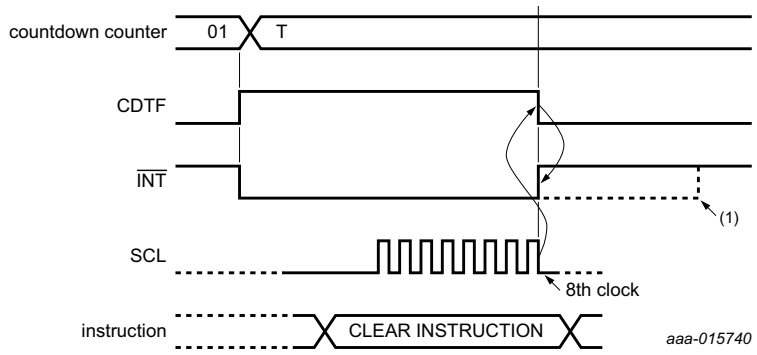
The pulse generator for the countdown timer interrupt also uses an internal clock which is dependent on the selected source clock for the countdown timer and on the countdown value T. As a consequence, the width of the interrupt pulse varies; see Table 36.

Table 36. $\overline{INT}$ operation (bit TI_TP = 1)

Source clock (Hz)	$\overline{INT}$ period (s)	
	T = 1[1]	T > 1
4096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] T = loaded countdown value. Timer stopped when T = 0.

If the TF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing; see Figure 11. Instructions for clearing TF are given in Section 8.6.3.



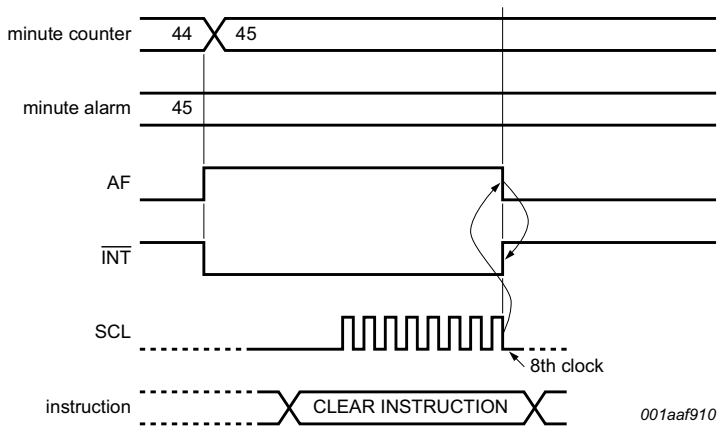
(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1).

Fig 11. Example of shortening the $\overline{INT}$ pulse by clearing the TF flag

The timing shown for clearing bit TF in Figure 11 is also valid for the non-pulsed interrupt mode, i.e., when bit TI_TP = 0, where the pulse can be shortened by setting bit TIE = 0.

8.7.3 Alarm interrupts

Generation of interrupts from the alarm function is controlled via bit AIE (register Control_2, see Table 7). If bit AIE is enabled, the $\overline{INT}$ pin follows the status of bit AF. Clearing bit AF immediately clears $\overline{INT}$. No pulse generation is possible for alarm interrupts; see Figure 12.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 12. AF timing

8.8 External clock test mode

A test mode is available which allows for on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting the EXT_TEST bit in register Control_1 (see Table 6). The CLKOUT pin then becomes an input. The test mode replaces the internal signal with the signal applied to pin CLKOUT.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal clock, now sourced from pin CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a prescaler; see Section 8.9. The prescaler can be set into a known state by using the STOP bit. When the STOP bit is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (register Control_1, bit STOP = 1).
3. Clear STOP (register Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

8.9 STOP bit function

The STOP bit function (register Control_1, see Table 6) allows the accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F_2 to F_{14}) to be held at reset, thus no 1 Hz ticks are generated. The time circuits can then be set and do not increment until STOP is released; see Figure 13. STOP does not affect the output of 32.768 kHz, 16.384 kHz, or 8.192 kHz; see Section 8.5.

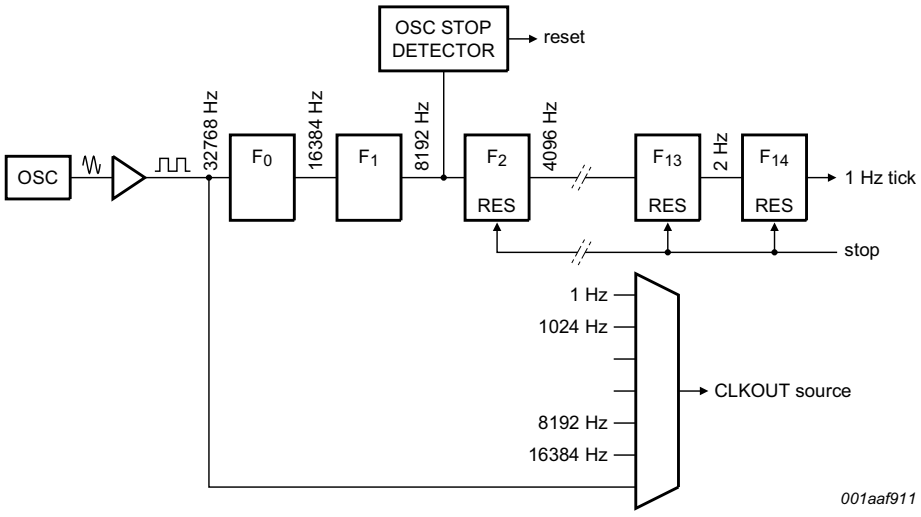


Fig 13. STOP bit functional diagram

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between 0 and one 8.192 kHz cycle; see Figure 14. The first increment of the time circuits is between 0.499878 s and 0.500000 s after STOP is released. The uncertainty is caused by prescaler bits F0 and F1 not being reset; see Table 37.

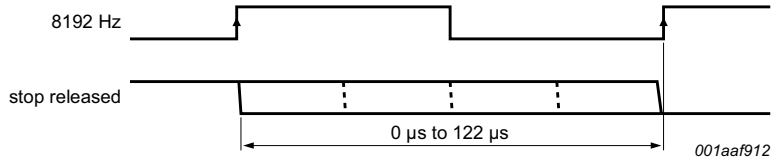
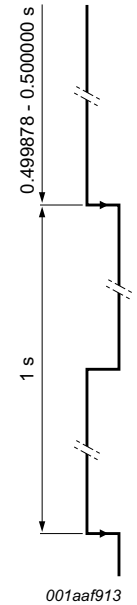


Fig 14. STOP bit release timing

Table 37. Example: first increment of time circuits after STOP release

Bit STOP	Prescaler bits F_0F_1-F_2 to F_{14}[1]	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP is activated by user. F0F1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F14 increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	:
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F14 increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

8.10 Reset

The PCA21125 includes an internal reset circuit which is active whenever the oscillator is stopped; see Figure 15. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground.

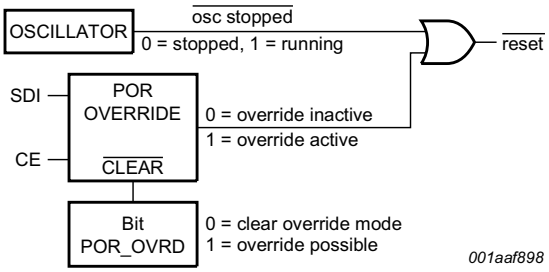


Fig 15. Reset system

The oscillator is considered to be stopped during the time between power-on and stable crystal resonance; see Figure 16. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature and supply voltage. Whenever an internal reset occurs, the reset flag RF (register Seconds, see Table 8) is set.

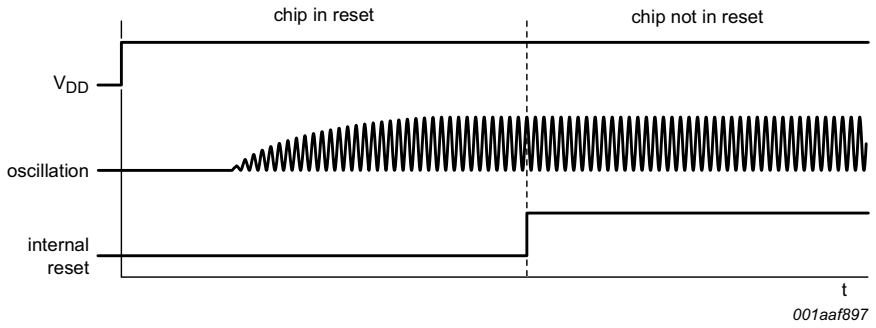


Fig 16. Power-On Reset (POR)