

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# PCA2129

Automotive accurate RTC with integrated quartz crystal

Rev. 5 — 19 December 2014

Product data sheet

## 1. General description

The PCA2129 is a CMOS<sup>1</sup> Real Time Clock (RTC) and calendar with an integrated Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal optimized for very high accuracy and very low power consumption. The PCA2129 has a selectable I<sup>2</sup>C-bus or SPI-bus, a backup battery switch-over circuit, a programmable watchdog function, a timestamp function, and many other features.

For a selection of NXP Real-Time Clocks, see [Table 83 on page 73](#)

## 2. Features and benefits

- AEC-Q100 compliant for automotive applications
- Operating temperature range from -40 °C to +85 °C
- Temperature Compensated Crystal Oscillator (TCXO) with integrated capacitors
- Typical accuracy: ±3 ppm from -30 °C to +80 °C
- Integration of a 32.768 kHz quartz crystal and oscillator in the same package
- Provides year, month, day, weekday, hours, minutes, seconds, and leap year correction
- Timestamp function
  - ◆ with interrupt capability
  - ◆ detection of two different events on one multilevel input pin (for example, for tamper detection)
- Two line bidirectional 400 kHz Fast-mode I<sup>2</sup>C-bus interface
- 3 line SPI-bus with separate data input and output (maximum speed 6.5 Mbit/s)
- Battery backup input pin and switch-over circuitry
- Battery backed output voltage
- Battery low detection function
- Power-On Reset Override (PORO)
- Oscillator stop detection function
- Interrupt output (open-drain)
- Programmable 1 second or 1 minute interrupt
- Programmable watchdog timer with interrupt
- Programmable alarm function with interrupt capability
- Programmable square output
- Clock operating voltage: 1.8 V to 4.2 V
- Low supply current: typical 0.70 μA at V<sub>DD</sub> = 3.3 V

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 21](#).



### 3. Applications

- Electronic metering for electricity, water, and gas
- Precision timekeeping
- Access to accurate time of the day
- GPS equipment to reduce time to first fix
- Applications that require an accurate process timing
- Products with long automated unattended operation time

### 4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA2129T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

#### 4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCA2129T/Q900/2	PCA2129T/Q900/2,51	935296923518	tape and reel, 13 inch, dry pack	2

### 5. Marking

Table 3. Marking codes

Product type number	Marking code
PCA2129T/Q900/2	PCA2129T/Q

6. Block diagram

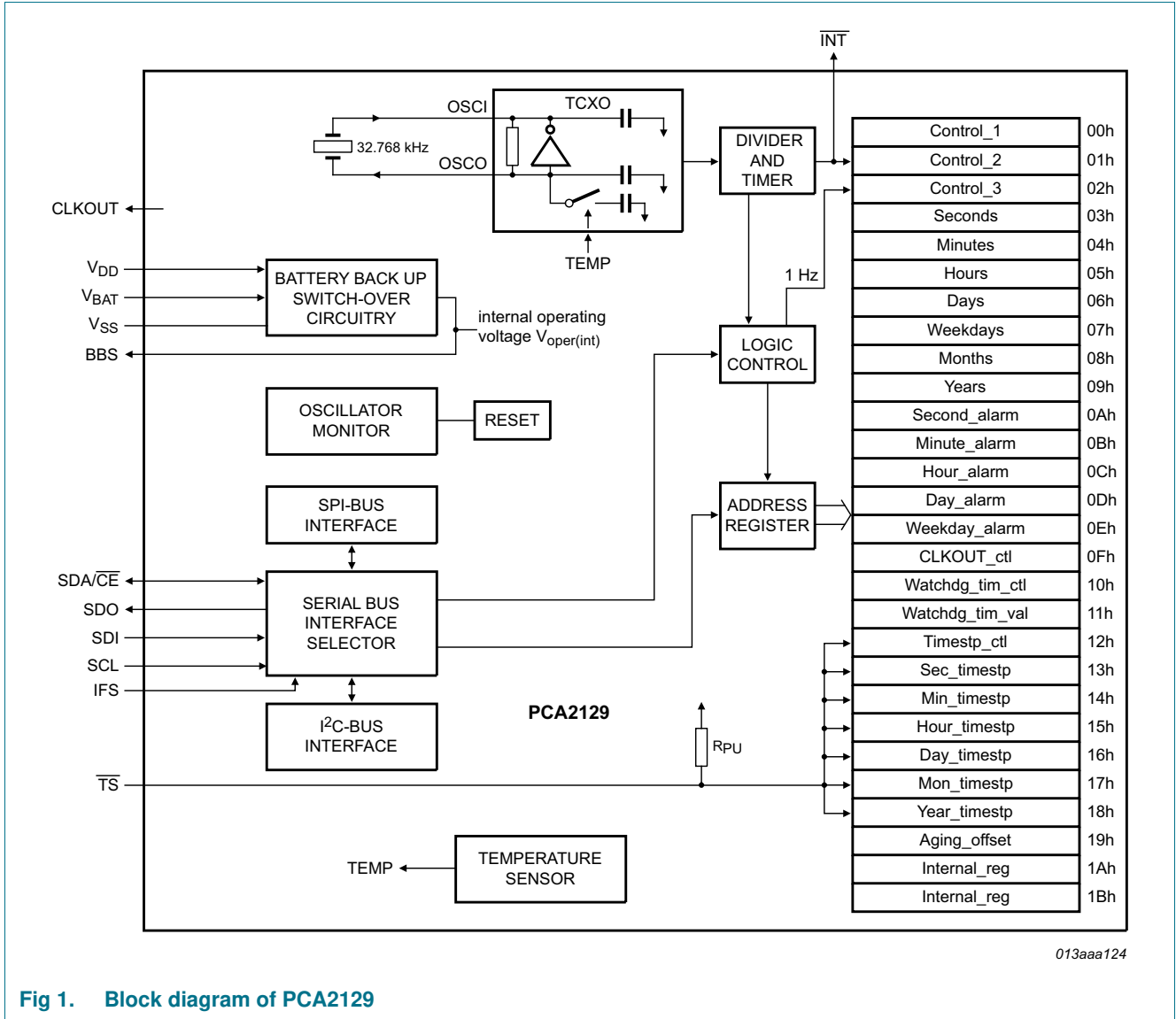
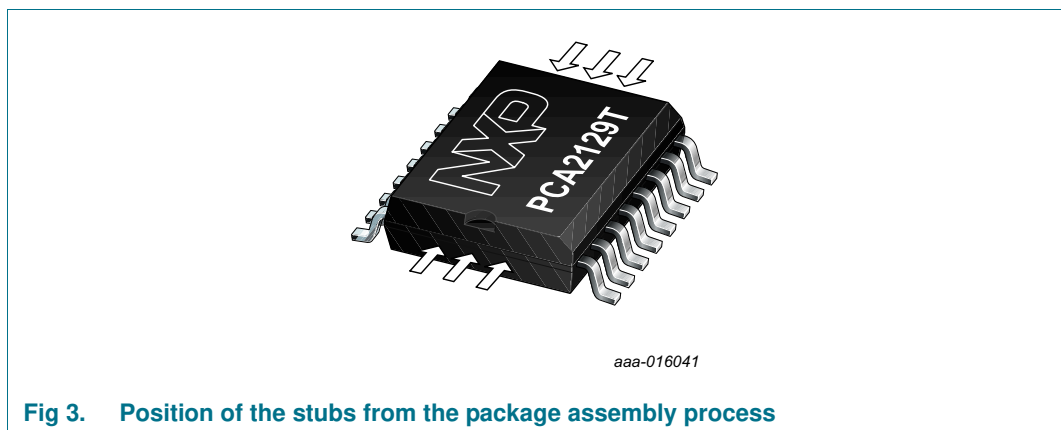
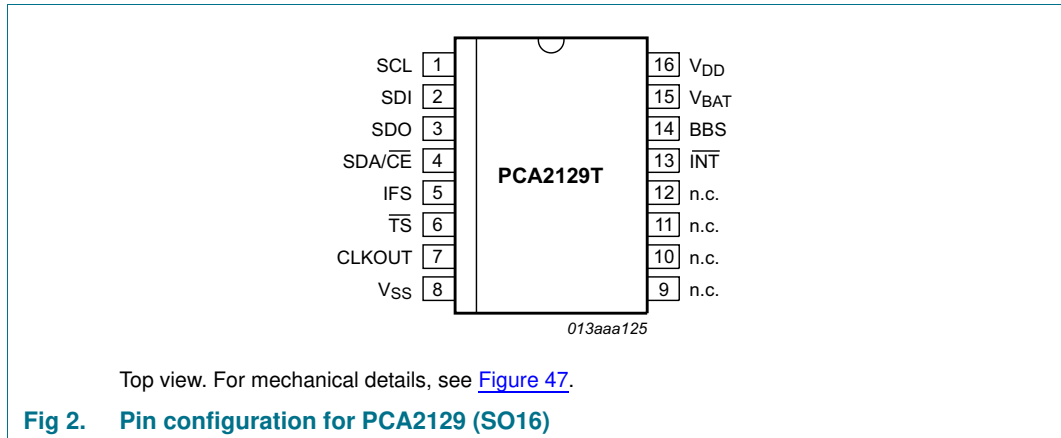


Fig 1. Block diagram of PCA2129

## 7. Pinning information

### 7.1 Pinning



After lead forming and cutting, there remain stubs from the package assembly process. These stubs are present at the edge of the package as illustrated in [Figure 3](#). The stubs are at an electrical potential. To avoid malfunction of the PCA2129, it has to be ensured that they are not shorted with another electrical potential (e.g. by condensation).

## 7.2 Pin description

**Table 4. Pin description of PCA2129**

*Input or input/output pins must always be at a defined level ( $V_{SS}$  or  $V_{DD}$ ) unless otherwise specified.*

Symbol	Pin	Description
SCL	1	combined serial clock input for both I <sup>2</sup> C-bus and SPI-bus
SDI	2	serial data input for SPI-bus connect to pin $V_{SS}$ if I <sup>2</sup> C-bus is selected
SDO	3	serial data output for SPI-bus, push-pull
SDA/ $\overline{\text{CE}}$	4	combined serial data input and output for the I <sup>2</sup> C-bus and chip enable input (active LOW) for the SPI-bus
IFS	5	interface selector input connect to pin $V_{SS}$ to select the SPI-bus connect to pin BBS to select the I <sup>2</sup> C-bus
$\overline{\text{TS}}$	6	timestamp input (active LOW) with 200 k $\Omega$ internal pull-up resistor ( $R_{PU}$ )
CLKOUT	7	clock output (open-drain)
$V_{SS}$	8	ground supply voltage
n.c.	9 to 12	not connected; do not connect; do not use as feed through
$\overline{\text{INT}}$	13	interrupt output (open-drain; active LOW)
BBS	14	output voltage (battery backed)
$V_{BAT}$	15	battery supply voltage (backup) connect to $V_{SS}$ if battery switch over is not used
$V_{DD}$	16	supply voltage

## 8. Functional description

The PCA2129 is a Real Time Clock (RTC) and calendar with an on-chip Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal integrated into the same package (see [Section 8.3.3](#)).

Address and data are transferred by a selectable 400 kHz Fast-mode I<sup>2</sup>C-bus or a 3 line SPI-bus with separate data input and output (see [Section 9](#)). The maximum speed of the SPI-bus is 6.5 Mbit/s.

The PCA2129 has a backup battery input pin and backup battery switch-over circuit which monitors the main power supply. The backup battery switch-over circuit automatically switches to the backup battery when a power failure condition is detected (see [Section 8.5.1](#)). Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery (see [Section 8.5.2](#)). When the battery voltage drops below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

### 8.1 Register overview

The PCA2129 contains an auto-incrementing address register: the built-in address register will increment automatically after each read or write of a data byte up to the register 1Bh. After register 1Bh, the auto-incrementing will wrap around to address 00h (see [Figure 4](#)).

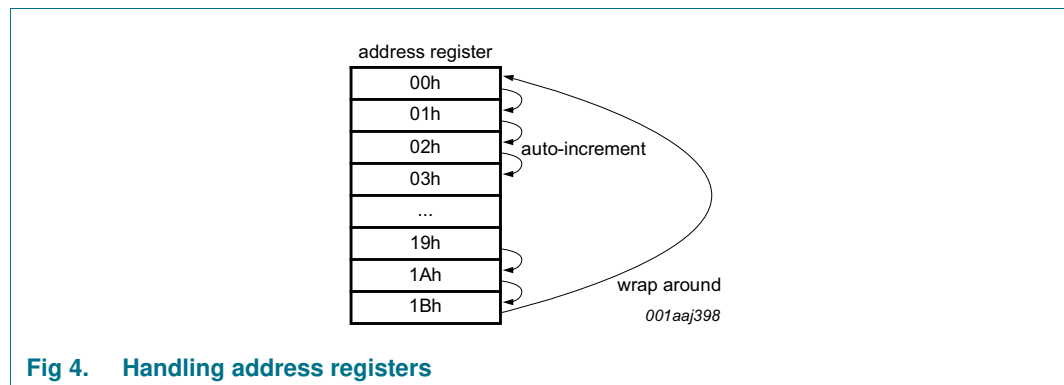


Fig 4. Handling address registers

- The first three registers (memory address 00h, 01h, and 02h) are used as control registers (see [Section 8.2](#)).
- The memory addresses 03h through to 09h are used as counters for the clock function (seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see [Section 8.8](#)).
- The registers at addresses 0Ah through 0Eh define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see [Section 8.9](#)).
- The register at address 0Fh defines the temperature measurement period and the clock out mode. The temperature measurement can be selected from every 4 minutes (default) down to every 30 seconds (see [Table 14](#)). CLKOUT frequencies of

32.768 kHz (default) down to 1 Hz for use as system clock, microcontroller clock, and so on, can be chosen (see [Table 15](#)).

- The registers at addresses 10h and 11h are used for the watchdog timer functions. The watchdog timer has four selectable source clocks allowing for timer periods from less than 1 ms to greater than 4 hours (see [Table 52](#)). An interrupt is generated when the watchdog times out.
- The registers at addresses 12h to 18h are used for the timestamp function. When the trigger event happens, the actual time is saved in the timestamp registers (see [Section 8.11](#)).
- The register at address 19h is used for the correction of the crystal aging effect (see [Section 8.4.1](#)).
- The registers at addresses 1Ah and 1Bh are for internal use only.
- The registers Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

When one of the RTC registers is written or read, the content of all counters is temporarily frozen. This prevents a faulty writing or reading of the clock and calendar during a carry condition (see [Section 8.8.8](#)).



**Table 5. Register overview**

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
<b>Control registers</b>											
00h	Control_1	EXT_TEST	T	STOP	TSF1	POR_OVRD	12_24	MI	SI	0000 1000	<a href="#">Table 7 on page 10</a>
01h	Control_2	MSF	WDTF	TSF2	AF	T	TSIE	AIE	T	0000 0000	<a href="#">Table 9 on page 11</a>
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE	0000 0000	<a href="#">Table 11 on page 12</a>
<b>Time and date registers</b>											
03h	Seconds	OSF	SECONDS (0 to 59)						1XXX XXXX	<a href="#">Table 22 on page 25</a>	
04h	Minutes	-	MINUTES (0 to 59)						- XXX XXXX	<a href="#">Table 25 on page 26</a>	
05h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode			- - XX XXXX	<a href="#">Table 27 on page 27</a>		
				HOURS (0 to 23) in 24-hour mode			- - XX XXXX				
06h	Days	-	-	DAYS (1 to 31)				- - XX XXXX	<a href="#">Table 29 on page 27</a>		
07h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		- - - - XXX	<a href="#">Table 31 on page 28</a>	
08h	Months	-	-	-	MONTHS (1 to 12)			- - - X XXXX	<a href="#">Table 34 on page 29</a>		
09h	Years	YEARS (0 to 99)						XXXX XXXX	<a href="#">Table 37 on page 30</a>		
<b>Alarm registers</b>											
0Ah	Second_alarm	AE_S	SECOND_ALARM (0 to 59)						1XXX XXXX	<a href="#">Table 39 on page 33</a>	
0Bh	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)						1XXX XXXX	<a href="#">Table 41 on page 33</a>	
0Ch	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode			1 - XX XXXX	<a href="#">Table 43 on page 34</a>		
				HOUR_ALARM (0 to 23) in 24-hour mode			1 - XX XXXX				
0Dh	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)				1 - XX XXXX	<a href="#">Table 45 on page 34</a>		
0Eh	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		1 - - - - XXX	<a href="#">Table 47 on page 35</a>	
<b>CLKOUT control register</b>											
0Fh	CLKOUT_ctl	TCR[1:0]		OTPR	-	-	COF[2:0]		00X - - 000	<a href="#">Table 13 on page 12</a>	
<b>Watchdog registers</b>											
10h	Watchdg_tim_ctl	WD_CD	T	TI_TP	-	-	-	TF[1:0]		000 - - - 11	<a href="#">Table 49 on page 36</a>
11h	Watchdg_tim_val	WATCHDGD_TIM_VAL[7:0]						XXXX XXXX	<a href="#">Table 51 on page 36</a>		
<b>Timestamp registers</b>											
12h	Timestamp_ctl	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]			00 - X XXXX	<a href="#">Table 58 on page 41</a>		

**Table 5. Register overview ...continued**

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference	
		7	6	5	4	3	2	1	0			
13h	Sec_timestp	-	SECOND_TIMESTP (0 to 59)								- XXX XXXX	<a href="#">Table 60 on page 41</a>
14h	Min_timestp	-	MINUTE_TIMESTP (0 to 59)								- XXX XXXX	<a href="#">Table 62 on page 42</a>
15h	Hour_timestp	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				-	- XX XXXX	<a href="#">Table 64 on page 42</a>	
				HOUR_TIMESTP (0 to 23) in 24-hour mode				- - XX XXXX				
16h	Day_timestp	-	-	DAY_TIMESTP (1 to 31)						- - XX XXXX	<a href="#">Table 66 on page 43</a>	
17h	Mon_timestp	-	-	-	MONTH_TIMESTP (1 to 12)				- - - X XXXX	<a href="#">Table 68 on page 43</a>		
18h	Year_timestp	YEAR_TIMESTP (0 to 99)								XXXX XXXX	<a href="#">Table 70 on page 43</a>	
<b>Aging offset register</b>												
19h	Aging_offset	-	-	-	-	AO[3:0]			- - - - 1000	<a href="#">Table 17 on page 14</a>		
<b>Internal registers</b>												
1Ah	Internal_reg	-	-	-	-	-	-	-	-	- - - - - - - -	-	
1Bh	Internal_reg	-	-	-	-	-	-	-	-	- - - - - - - -	-	

## 8.2 Control registers

The first 3 registers of the PCA2129, with the addresses 00h, 01h, and 02h, are used as control registers.

### 8.2.1 Register Control\_1

**Table 6. Control\_1 - control and status register 1 (address 00h) bit allocation**

Bits labeled as T must always be written with logic 0.

Bit	7	6	5	4	3	2	1	0
Symbol	EXT_TEST	T	STOP	TSF1	POR_OVRD	12_24	MI	SI
Reset value	0	0	0	0	1	0	0	0

**Table 7. Control\_1 - control and status register 1 (address 00h) bit description**

Bits labeled as T must always be written with logic 0.

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0	normal mode	<a href="#">Section 8.13</a>
		1	external clock test mode	
6	T	0	unused	-
5	STOP	0	RTC source clock runs	<a href="#">Section 8.14</a>
		1	RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available	
4	TSF1	0	no timestamp interrupt generated	<a href="#">Section 8.11.1</a>
		1	flag set when $\overline{TS}$ input is driven to an intermediate level between power supply and ground; flag must be cleared to clear interrupt	
3	POR_OVRD	0	Power-On Reset Override (PORO) facility disabled; <b>set logic 0 for normal operation</b>	<a href="#">Section 8.7.2</a>
		1	Power-On Reset Override (PORO) sequence reception enabled	
2	12_24	0	24-hour mode selected	<a href="#">Table 27,</a> <a href="#">Table 43,</a> <a href="#">Table 64</a>
		1	12-hour mode selected	
1	MI	0	minute interrupt disabled	<a href="#">Section 8.12.1</a>
		1	minute interrupt enabled	
0	SI	0	second interrupt disabled	
		1	second interrupt enabled	

## 8.2.2 Register Control\_2

**Table 8. Control\_2 - control and status register 2 (address 01h) bit allocation**

Bits labeled as T must always be written with logic 0.

Bit	7	6	5	4	3	2	1	0
Symbol	MSF	WDTF	TSF2	AF	T	TSIE	AIE	T
Reset value	0	0	0	0	0	0	0	0

**Table 9. Control\_2 - control and status register 2 (address 01h) bit description**

Bits labeled as T must always be written with logic 0.

Bit	Symbol	Value	Description	Reference
7	MSF	0	no minute or second interrupt generated	<a href="#">Section 8.12</a>
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
6	WDTF	0	no watchdog timer interrupt or reset generated	<a href="#">Section 8.12.3</a>
		1	flag set when watchdog timer interrupt or reset generated; flag cannot be cleared by command (read-only)	
5	TSF2	0	no timestamp interrupt generated	<a href="#">Section 8.11.1</a>
		1	flag set when $\overline{TS}$ input is driven to ground; flag must be cleared to clear interrupt	
4	AF	0	no alarm interrupt generated	<a href="#">Section 8.9.6</a>
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
3	T	0	unused	-
2	TSIE	0	no interrupt generated from timestamp flag	<a href="#">Section 8.12.5</a>
		1	interrupt generated when timestamp flag set	
1	AIE	0	no interrupt generated from the alarm flag	<a href="#">Section 8.12.4</a>
		1	interrupt generated when alarm flag set	
0	T	0	unused	-

### 8.2.3 Register Control\_3

**Table 10. Control\_3 - control and status register 3 (address 02h) bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
Reset value	0	0	0	0	0	0	0	0

**Table 11. Control\_3 - control and status register 3 (address 02h) bit description**

Bit	Symbol	Value	Description	Reference
7 to 5	PWRMNG[2:0]	see <a href="#">Table 19</a>	control of the battery switch-over, battery low detection, and extra power fail detection functions	<a href="#">Section 8.5</a>
4	BTSE	0	no timestamp when battery switch-over occurs	<a href="#">Section 8.11.4</a>
		1	time-stamped when battery switch-over occurs	
3	BF	0	no battery switch-over interrupt generated	<a href="#">Section 8.5.1</a> and <a href="#">Section 8.11.4</a>
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt	
2	BLF	0	battery status ok; no battery low interrupt generated	<a href="#">Section 8.5.2</a>
		1	battery status low; flag cannot be cleared by command	
1	BIE	0	no interrupt generated from the battery flag (BF)	<a href="#">Section 8.12.6</a>
		1	interrupt generated when BF is set	
0	BLIE	0	no interrupt generated from battery low flag (BLF)	<a href="#">Section 8.12.7</a>
		1	interrupt generated when BLF is set	

### 8.3 Register CLKOUT\_ctl

**Table 12. CLKOUT\_ctl - CLKOUT control register (address 0Fh) bit allocation**

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	TCR[1:0]		OTPR	-	-	COF[2:0]		
Reset value	0	0	X	-	-	0	0	0

**Table 13. CLKOUT\_ctl - CLKOUT control register (address 0Fh) bit description**

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7 to 6	TCR[1:0]	see <a href="#">Table 14</a>	temperature measurement period
5	OTPR	0	no OTP refresh
		1	OTP refresh performed
4 to 3	-	-	unused
2 to 0	COF[2:0]	see <a href="#">Table 15</a>	CLKOUT frequency selection

### 8.3.1 Temperature compensated crystal oscillator

The frequency of tuning fork quartz crystal oscillators is temperature-dependent. In the PCA2129, the frequency deviation caused by temperature variation is corrected by adjusting the load capacitance of the crystal oscillator.

The load capacitance is changed by switching between two load capacitance values using a modulation signal with a programmable duty cycle. In order to compensate the spread of the quartz parameters every chip is factory calibrated.

The frequency accuracy can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT. However, the selection of  $f_{CLKOUT} = 32.768$  kHz (default value) leads to inaccurate measurements. Accurate frequency measurement occurs when  $f_{CLKOUT} = 16.384$  kHz or lower is selected (see [Table 15](#)).

#### 8.3.1.1 Temperature measurement

The PCA2129 has a temperature sensor circuit used to perform the temperature compensation of the frequency. The temperature is measured immediately after power-on and then periodically with a period set by the temperature conversion rate TCR[1:0] in the register CLKOUT\_ctl.

**Table 14. Temperature measurement period**

TCR[1:0]	Temperature measurement period
00	<a href="#">[1]</a> 4 min
01	2 min
10	1 min
11	30 seconds

[1] Default value.

#### 8.3.2 OTP refresh

Each IC is calibrated during production and testing of the device. The calibration parameters are stored on EPROM cells called One Time Programmable (OTP) cells. It is recommended to process an OTP refresh once after the power is up and the oscillator is operating stable. The OTP refresh takes less than 100 ms to complete.

To perform an OTP refresh, bit OTPR has to be cleared (set to logic 0) and then set to logic 1 again.

#### 8.3.3 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] control bits in register CLKOUT\_ctl. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as system clock, microcontroller clock, charge pump input, or for calibrating the oscillator.

CLKOUT is an open-drain output and enabled at power-on. When disabled, the output is high-impedance.

**Table 15. CLKOUT frequency selection**

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle <sup>[1]</sup>
000 <sup>[2][3]</sup>	32768	60 : 40 to 40 : 60
001	16384	50 : 50
010	8192	50 : 50
011	4096	50 : 50
100	2048	50 : 50
101	1024	50 : 50
110	1	50 : 50
111	CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] The specified accuracy of the RTC can be only achieved with CLKOUT frequencies not equal to 32.768 kHz or if CLKOUT is disabled.

The duty cycle of the selected clock is not controlled, however, due to the nature of the clock generation all but the 32.768 kHz frequencies are 50 : 50.

## 8.4 Register Aging\_offset

**Table 16. Aging\_offset - crystal aging offset register (address 19h) bit allocation**

Bit positions labeled as - are not implemented and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	AO[3:0]			
Reset value	-	-	-	-	1	0	0	0

**Table 17. Aging\_offset - crystal aging offset register (address 19h) bit description**

Bit positions labeled as - are not implemented and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	-	-	unused
3 to 0	AO[3:0]	see <a href="#">Table 18</a>	aging offset value

### 8.4.1 Crystal aging correction

The PCA2129 has an offset register Aging\_offset to correct the crystal aging effects<sup>2</sup>.

The accuracy of the frequency of a quartz crystal depends on its aging. The aging offset adds an adjustment, positive or negative, in the temperature compensation circuit which allows correcting the aging effect.

At 25 °C, the aging offset bits allow a frequency correction of typically 1 ppm per AO[3:0] value, from -7 ppm to +8 ppm.

2. For further information, refer to the application note [Ref. 3 "AN11186"](#).

Table 18. Frequency correction at 25 °C, typical

AO[3:0]		ppm
Decimal	Binary	
0	0000	+8
1	0001	+7
2	0010	+6
3	0011	+5
4	0100	+4
5	0101	+3
6	0110	+2
7	0111	+1
8	1000	<a href="#">[1]</a> 0
9	1001	-1
10	1010	-2
11	1011	-3
12	1100	-4
13	1101	-5
14	1110	-6
15	1111	-7

[1] Default value.



## 8.5 Power management functions

The PCA2129 has two power supplies:

$V_{DD}$  — the main power supply

$V_{BAT}$  — the battery backup supply

Internally, the PCA2129 is operating with the internal operating voltage  $V_{oper(int)}$  which is also available as  $V_{BBS}$  on the battery backed output voltage pin, BBS. Depending on the condition of the main power supply and the selected power management function,  $V_{oper(int)}$  is either on the potential of  $V_{DD}$  or  $V_{BAT}$  (see [Section 8.5.3](#)).

Two power management functions are implemented:

**Battery switch-over function** — monitoring the main power supply  $V_{DD}$  and switching to  $V_{BAT}$  in case a power fail condition is detected (see [Section 8.5.1](#)).

**Battery low detection function** — monitoring the status of the battery,  $V_{BAT}$  (see [Section 8.5.2](#)).

The power management functions are controlled by the control bits PWRMNG[2:0] (see [Table 19](#)) in register Control\_3 (see [Table 11](#)):

**Table 19. Power management control bit description**

PWRMNG[2:0]	Function
000	<a href="#">[1]</a> battery switch-over function is enabled in standard mode; battery low detection function is enabled
001	battery switch-over function is enabled in standard mode; battery low detection function is disabled
010	battery switch-over function is enabled in standard mode; battery low detection function is disabled
011	battery switch-over function is enabled in direct switching mode; battery low detection function is enabled
100	battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
101	battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
111	<a href="#">[2]</a> battery switch-over function is disabled, only one power supply ( $V_{DD}$ ); battery low detection function is disabled

[1] Default value.

[2] When the battery switch-over function is disabled, the PCA2129 works only with the power supply  $V_{DD}$ .  $V_{BAT}$  must be put to ground and the battery low detection function is disabled.

### 8.5.1 Battery switch-over function

The PCA2129 has a backup battery switch-over circuit which monitors the main power supply  $V_{DD}$ . When a power failure condition is detected, it automatically switches to the backup battery.

One of two operation modes can be selected:

**Standard mode** — the power failure condition happens when:

$$V_{DD} < V_{BAT} \text{ AND } V_{DD} < V_{th(sw)bat}$$

$V_{th(sw)bat}$  is the battery switch threshold voltage. Typical value is 2.5 V. The battery switch-over in standard mode works only for  $V_{DD} > 2.5$  V

**Direct switching mode** — the power failure condition happens when  $V_{DD} < V_{BAT}$ . Direct switching from  $V_{DD}$  to  $V_{BAT}$  without requiring  $V_{DD}$  to drop below  $V_{th(sw)bat}$

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BF (register Control\_3) is set logic 1.
2. An interrupt is generated if the control bit BIE (register Control\_3) is enabled (see [Section 8.12.6](#)).
3. If the control bit BTSE (register Control\_3) is logic 1, the timestamp registers store the time and date when the battery switch occurred (see [Section 8.11.4](#)).
4. The battery switch flag BF is cleared by command; it must be cleared to clear the interrupt.

The interface is disabled in battery backup operation:

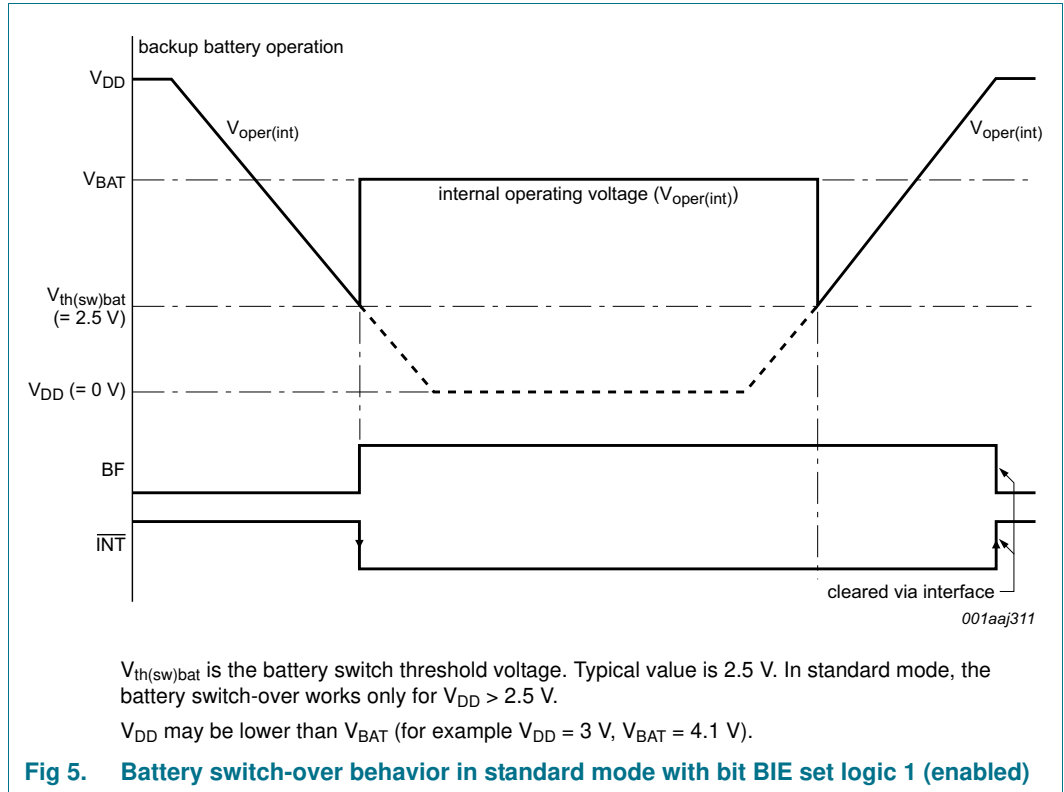
- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

For further information about I<sup>2</sup>C-bus communication and battery backup operation, see [Section 9.3 on page 56](#).

8.5.1.1 Standard mode

If  $V_{DD} > V_{BAT}$  OR  $V_{DD} > V_{th(sw)bat}$ :  $V_{oper(int)}$  is at  $V_{DD}$  potential.

If  $V_{DD} < V_{BAT}$  AND  $V_{DD} < V_{th(sw)bat}$ :  $V_{oper(int)}$  is at  $V_{BAT}$  potential.

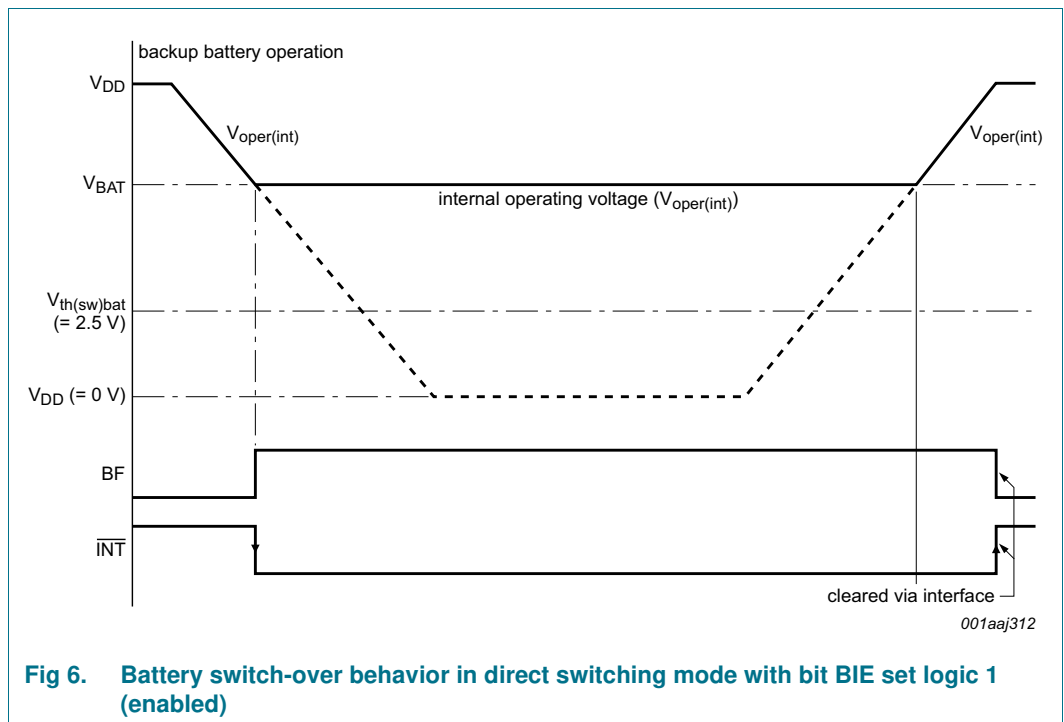


**8.5.1.2 Direct switching mode**

If  $V_{DD} > V_{BAT}$ :  $V_{oper(int)}$  is at  $V_{DD}$  potential.

If  $V_{DD} < V_{BAT}$ :  $V_{oper(int)}$  is at  $V_{BAT}$  potential.

The direct switching mode is useful in systems where  $V_{DD}$  is always higher than  $V_{BAT}$ . This mode is not recommended if the  $V_{DD}$  and  $V_{BAT}$  values are similar (for example,  $V_{DD} = 3.3\text{ V}$ ,  $V_{BAT} \geq 3.0\text{ V}$ ). In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of  $V_{DD}$  and  $V_{th(sw)bat}$  is not performed.



**8.5.1.3 Battery switch-over disabled: only one power supply ( $V_{DD}$ )**

When the battery switch-over function is disabled:

- The power supply is applied on the  $V_{DD}$  pin
- The  $V_{BAT}$  pin must be connected to ground
- $V_{oper(int)}$  is at  $V_{DD}$  potential
- The battery flag (BF) is always logic 0

8.5.1.4 Battery switch-over architecture

The architecture of the battery switch-over circuit is shown in [Figure 7](#).

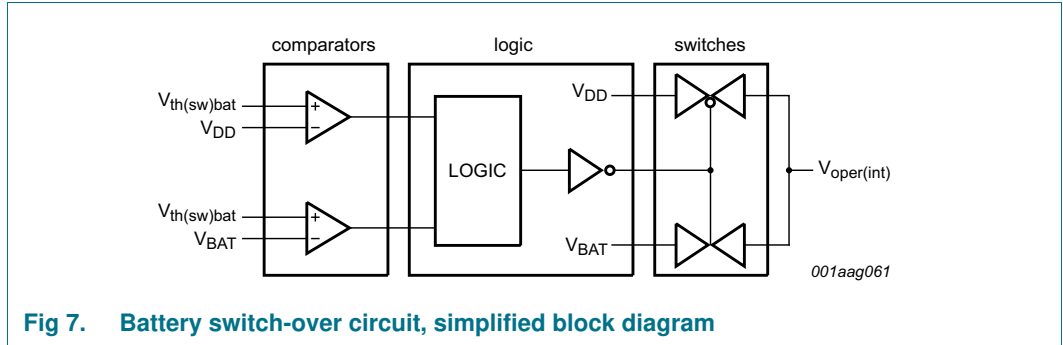


Fig 7. Battery switch-over circuit, simplified block diagram

$V_{oper(int)}$  is at  $V_{DD}$  or  $V_{BAT}$  potential.

**Remark:** It has to be assured that there are decoupling capacitors on the pins  $V_{DD}$ ,  $V_{BAT}$ , and BBS.

8.5.2 Battery low detection function

The PCA2129 has a battery low detection circuit which monitors the status of the battery  $V_{BAT}$ .

When  $V_{BAT}$  drops below the threshold value  $V_{th(bat)low}$  (typically 2.5 V), the BLF flag (register Control\_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery cannot prevent that the supply voltage drops below  $V_{low}$  (typical 1.2 V) and with that the data integrity gets lost. (For further information about  $V_{low}$  see [Section 8.6.](#))

When  $V_{BAT}$  drops below the threshold value  $V_{th(bat)low}$ , the following sequence occurs (see [Figure 8](#)):

1. The battery low flag BLF is set logic 1.
2. An interrupt is generated if the control bit BLIE (register Control\_3) is enabled (see [Section 8.12.7](#)).
3. The flag BLF remains logic 1 until the battery is replaced. BLF cannot be cleared by command. It is automatically cleared by the battery low detection circuit when the battery is replaced or when the voltage rises again above the threshold value. This could happen if a super capacitor is used as a backup source and the main power is applied again.

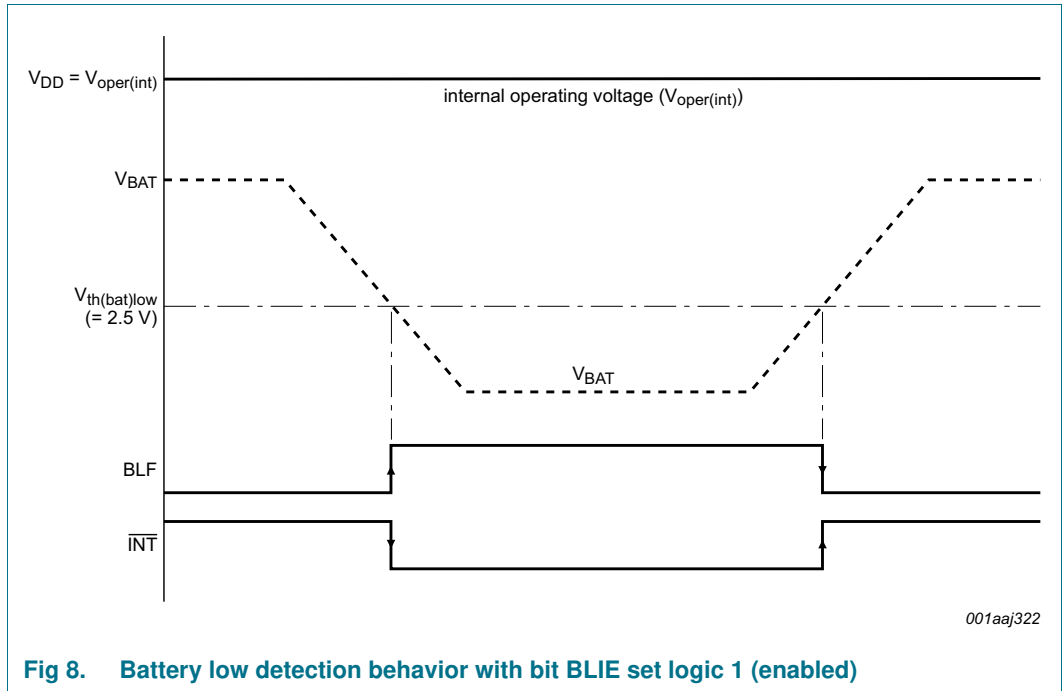


Fig 8. Battery low detection behavior with bit BLIE set logic 1 (enabled)

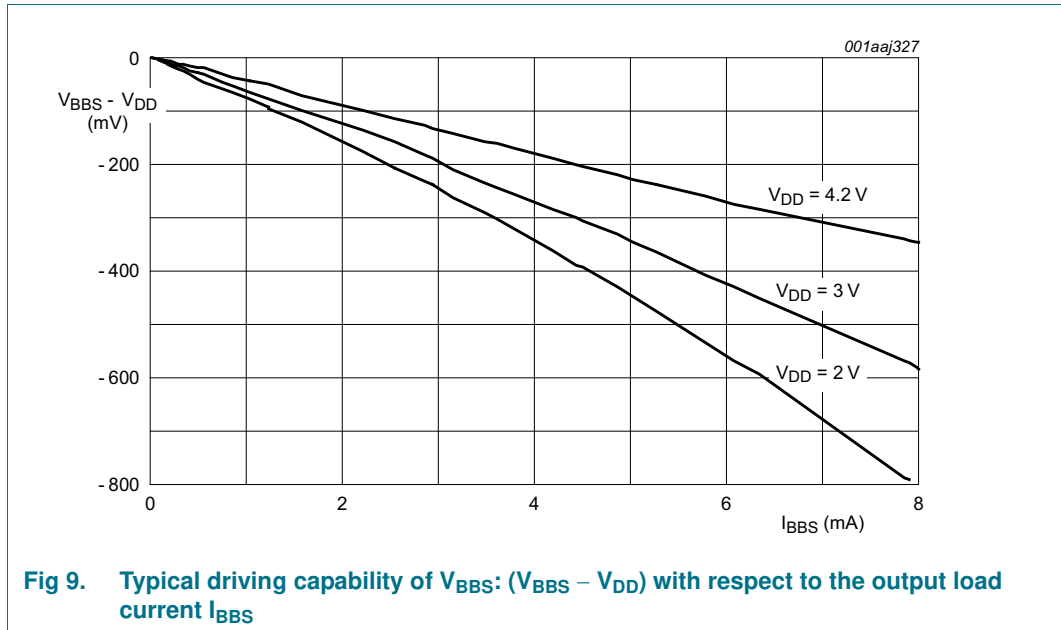
### 8.5.3 Battery backup supply

The  $V_{BBS}$  voltage on the output pin BBS is at the same potential as the internal operating voltage  $V_{oper(int)}$ , depending on the selected battery switch-over function mode:

Table 20. Output pin BBS

Battery switch-over function mode	Conditions	Potential of $V_{oper(int)}$ and $V_{BBS}$
standard	$V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$	$V_{DD}$
	$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$	$V_{BAT}$
direct switching	$V_{DD} > V_{BAT}$	$V_{DD}$
	$V_{DD} < V_{BAT}$	$V_{BAT}$
disabled	only $V_{DD}$ available, $V_{BAT}$ must be put to ground	$V_{DD}$

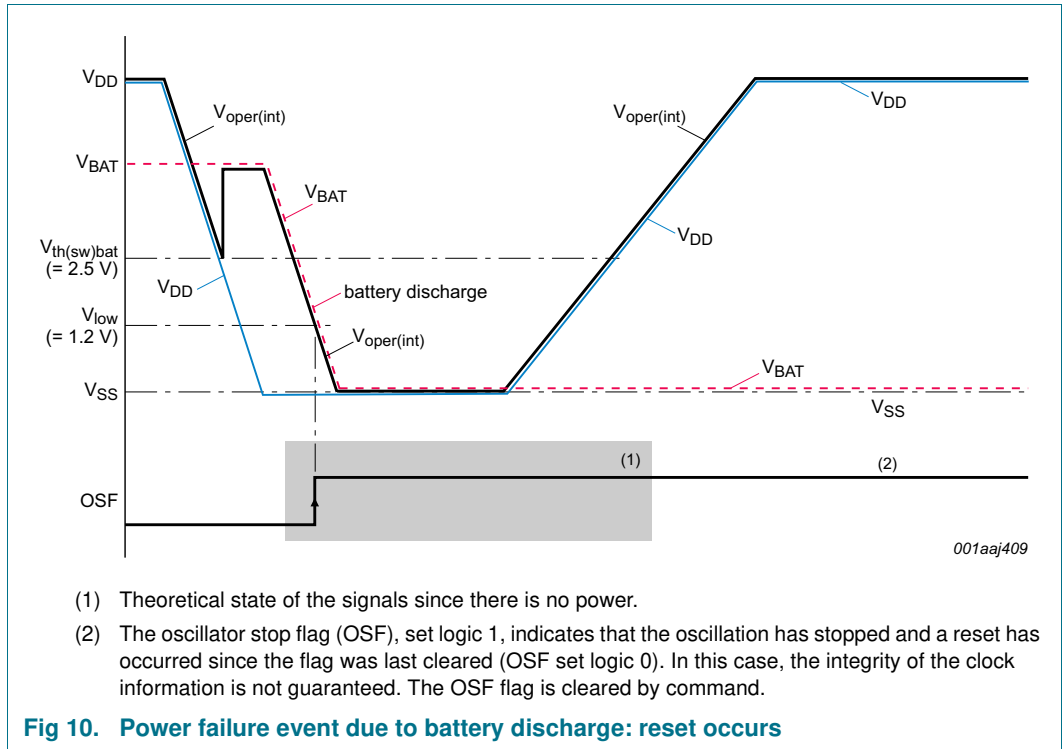
The output pin BBS can be used as a supply for external devices with battery backup needs, such as SRAM (see [Ref. 3 "AN11186"](#)). For this case, [Figure 9](#) shows the typical driving capability when  $V_{BBS}$  is driven from  $V_{DD}$ .



### 8.6 Oscillator stop detection function

The PCA2129 has an on-chip oscillator detection circuit which monitors the status of the oscillation: whenever the oscillation stops, a reset occurs and the oscillator stop flag OSF (in register Seconds) is set logic 1.

- **Power-on:**
  - a. The oscillator is not running, the chip is in reset (OSF is logic 1).
  - b. When the oscillator starts running and is stable after power-on, the chip exits from reset.
  - c. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.
- **Power supply failure:**
  - a. When the power supply of the chip drops below a certain value ( $V_{low}$ ), typically 1.2 V, the oscillator stops running and a reset occurs.
  - b. When the power supply returns to normal operation, the oscillator starts running again, the chip exits from reset.
  - c. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.



## 8.7 Reset function

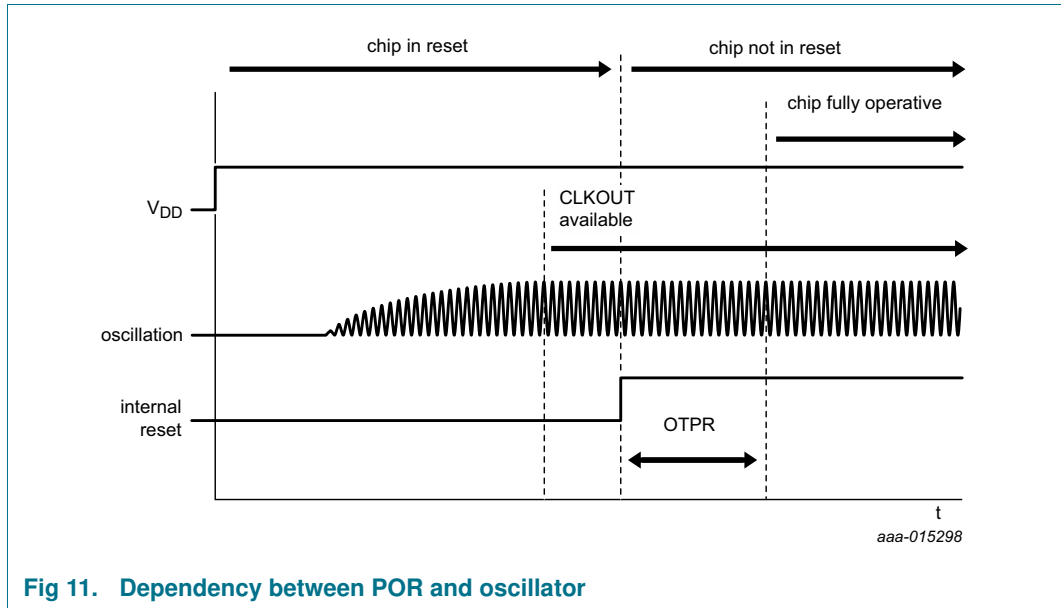
The PCA2129 has a Power-On Reset (POR) and a Power-On Reset Override (PORO) function implemented.

### 8.7.1 Power-On Reset (POR)

The POR is active whenever the oscillator is stopped. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance (see [Figure 11](#)). This time may be in the range of 200 ms to 2 s depending on temperature and supply voltage. Whenever an internal reset occurs, the oscillator stop flag is set (OSF set logic 1).

The OTP refresh (see [Section 8.3.2 on page 13](#)) should ideally be executed as the first instruction after start-up and also after a reset due to an oscillator stop.





**Fig 11. Dependency between POR and oscillator**

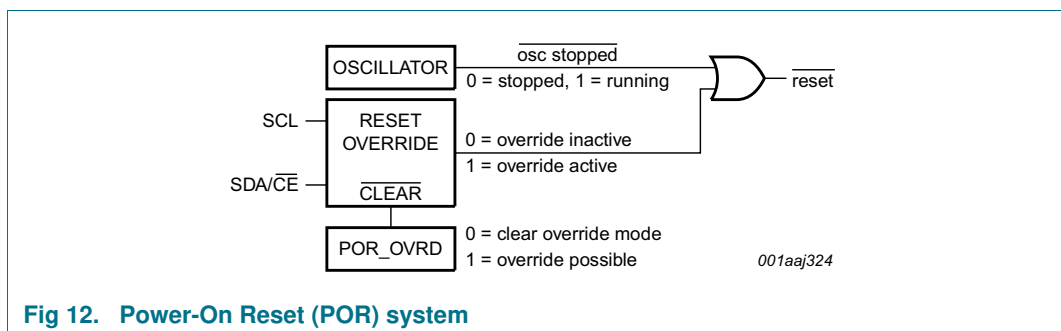
After POR, the following mode is entered:

- 32.768 kHz CLKOUT active
- Power-On Reset Override (PORO) available to be set
- 24-hour mode is selected
- Battery switch-over is enabled
- Battery low detection is enabled

The register values after power-on are shown in [Table 5 on page 8](#).

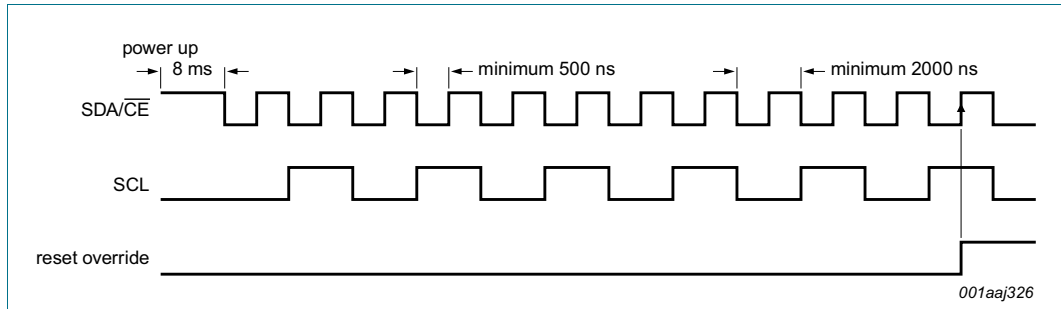
### 8.7.2 Power-On Reset Override (PORO)

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and therefore speed up the on-board test of the device.



**Fig 12. Power-On Reset (POR) system**

The setting of the PORO mode requires that POR\_OVRD in register Control\_1 is set logic 1 and that the signals at the interface pins SDA/CLE and SCL are toggled as illustrated in [Figure 13](#). All timings shown are required minimum.



**Fig 13. Power-On Reset Override (PORO) sequence, valid for both I<sup>2</sup>C-bus and SPI-bus**

Once the override mode is entered, the device is immediately released from the reset state and the set-up operation can commence.

The PORO mode is cleared by writing logic 0 to POR\_OVRD. POR\_OVRD must be logic 1 before a re-entry into the override mode is possible. Setting POR\_OVRD logic 0 during normal operation has no effect except to prevent accidental entry into the PORO mode.

## 8.8 Time and date function

Most of these registers are coded in the Binary Coded Decimal (BCD) format.

### 8.8.1 Register Seconds

**Table 21. Seconds - seconds and clock integrity register (address 03h) bit allocation**

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	OSF	SECONDS (0 to 59)						
Reset value	1	X	X	X	X	X	X	X

**Table 22. Seconds - seconds and clock integrity register (address 03h) bit description**

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	OSF	0	-	clock integrity is guaranteed
		1	-	clock integrity is not guaranteed: oscillator has stopped and chip reset has occurred since flag was last cleared
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	