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PCA85063A

Automotive tiny Real-Time Clock/calendar with alarm function and I²C-bus

Rev. 4 — 30 March 2018

Product data sheet

1. General description

The PCA85063A is a CMOS¹ Real-Time Clock (RTC) and calendar optimized for low power consumption. An offset register allows fine-tuning of the clock. All addresses and data are transferred serially via the two-line bidirectional I²C-bus. Maximum data rate is 400 kbit/s. The register address is incremented automatically after each written or read data byte.

For a selection of NXP Real-Time Clocks, see [Table 45 on page 50](#)

2. Features and benefits

- AEC-Q100 grade 2 compliant for automotive applications
- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Low current; typical 0.25 μ A at $V_{DD} = 3.0$ V and $T_{amb} = 25$ °C
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz, and 1 Hz)
- Alarm function
- Minute and half minute interrupt
- Internal Power-On Reset (POR)
- High temperature operation range: -40 °C to $+105$ °C
- Clock operating voltage: 0.9 V to 5.5 V
- 400 kHz two-line I²C-bus interface (at $V_{DD} = 1.8$ V to 5.5 V)
- Selectable integrated oscillator load capacitors for $C_L = 7$ pF or $C_L = 12.5$ pF
- Countdown timer
- Oscillator stop detection function
- Programmable offset register for frequency adjustment

3. Applications

- Tracking time of the day
- Dashboard
- Air condition
- Telematics
- Accurate timing
- Infotainment unit
- Center stack
- Body control and battery management

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 22](#).



4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|---------|---|----------|
| | Name | Description | Version |
| PCA85063ATT | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |

4.1 Ordering options

Table 2. Ordering options

| Product type number | Orderable part number | Sales item (12NC) | Delivery form | IC revision |
|---------------------|-----------------------|-------------------|------------------------|-------------|
| PCA85063ATT/A | PCA85063ATT/AJ | 935305541118 | tape and reel, 13 inch | 1 |

5. Marking

Table 3. Marking codes

| Product type number | Marking code |
|---------------------|--------------|
| PCA85063ATT/A | 063Q |

6. Block diagram

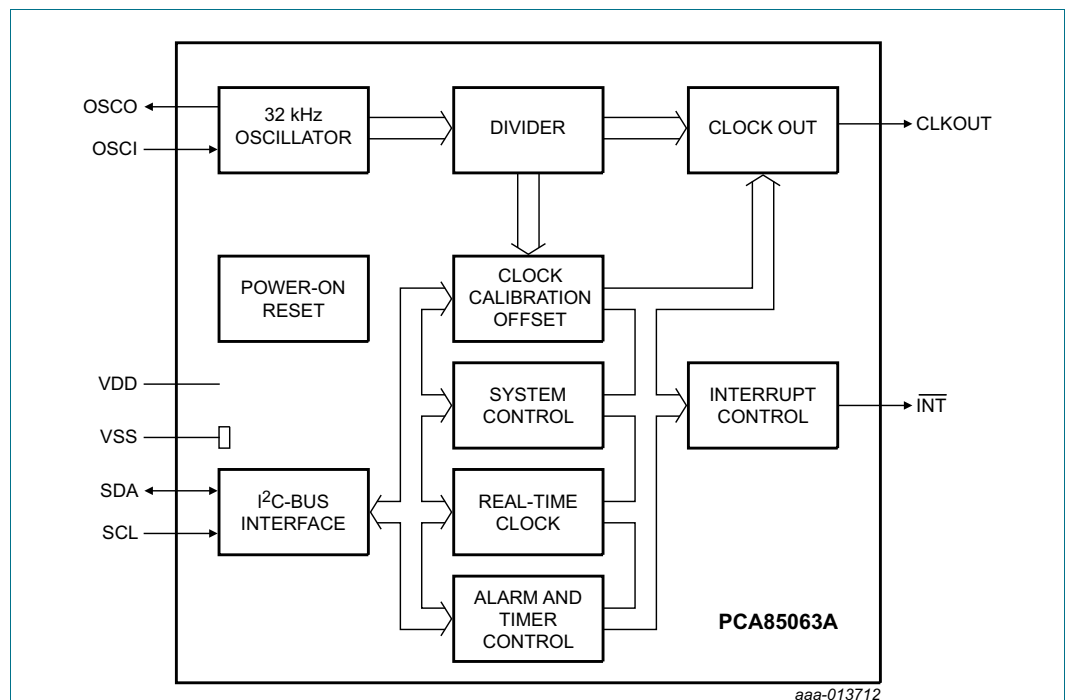
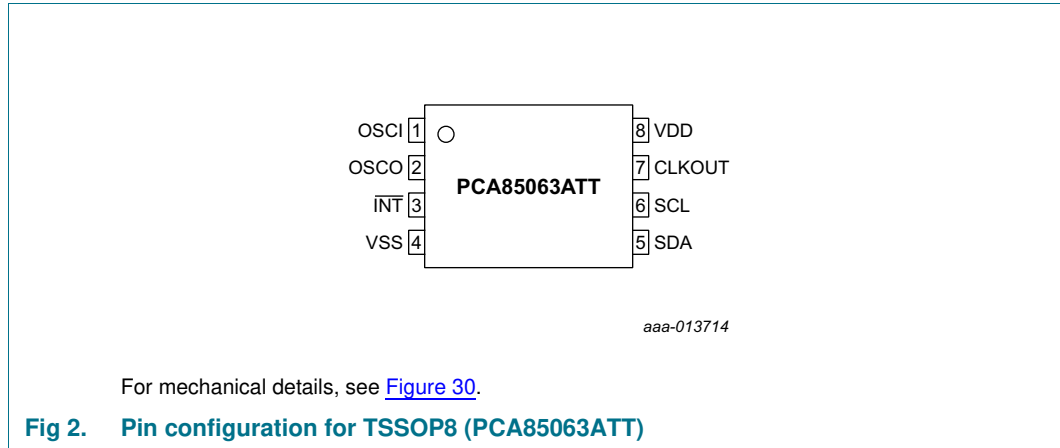


Fig 1. Block diagram of PCA85063A

7. Pinning information

7.1 Pinning



7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

| Symbol | Pin | Type | Description |
|--|-------------|--------------|-------------------------------|
| | PCA85063ATT | | |
| OSCI | 1 | input | oscillator input |
| OSCO | 2 | output | oscillator output |
| $\overline{\text{INT}}$ ^[1] | 3 | output | interrupt output (open-drain) |
| VSS | 4 | supply | ground supply voltage |
| SDA ^[1] | 5 | input/output | serial data line |
| SCL ^[1] | 6 | input | serial clock input |
| CLKOUT | 7 | output | clock output (push-pull) |
| VDD | 8 | supply | supply voltage |

[1] NXP recommends tying VDD of the device and VDD of all the external pull-up resistors to the same Power Supply.

8. Functional description

The PCA85063A contains 18 8-bit registers with an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calendar, and an I²C-bus interface with a maximum data rate of 400 kbit/s.

The built-in address register will increment automatically after each read or write of a data byte up to the register 11h. After register 11h, the auto-incrementing will wrap around to address 00h (see [Figure 3](#)).

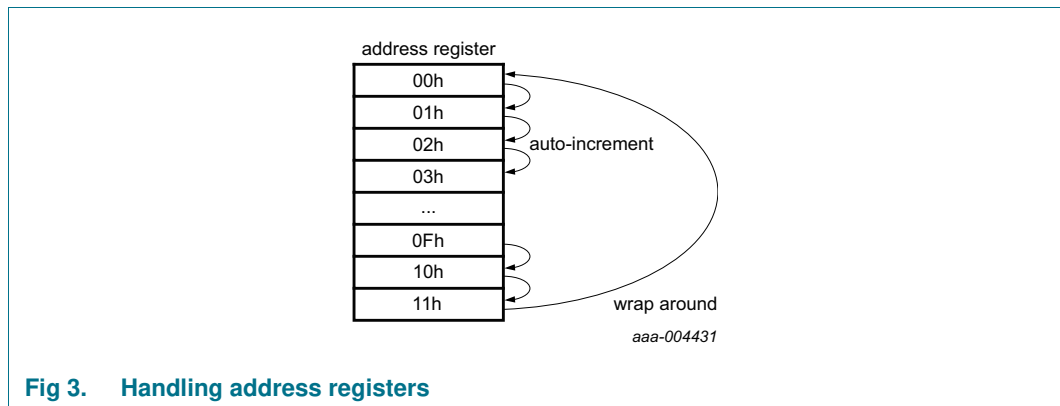


Fig 3. Handling address registers

All registers (see [Table 5](#)) are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and status register. The register at address 02h is an offset register allowing the fine-tuning of the clock; and at 03h is a free RAM byte. The addresses 04h through 0Ah are used as counters for the clock function (seconds up to years counters). Address locations 0Bh through 0Fh contain alarm registers which define the conditions for an alarm. The registers at 10h and 11h are for the timer function.

The Seconds, Minutes, Hours, Days, Months, and Years as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented. For details on maximum access time, see [Section 8.4 on page 23](#).

8.1 Registers organization

Table 5. Registers overview

Bit positions labeled as - are not implemented. After reset, all registers are set according to [Table 8 on page 10](#).

| Address | Register name | Bit | | | | | | | | Reference | |
|-------------------------------------|---------------|-----------------|------------------------|--------------------------------------|--------------------------------------|----|------------------------|-------|---------|-------------------------------|-------------------------------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Control and status registers | | | | | | | | | | | |
| 00h | Control_1 | EXT_TEST | - | STOP | SR | - | CIE | 12_24 | CAP_SEL | Section 8.2.1 | |
| 01h | Control_2 | AIE | AF | MI | HMI | TF | COF[2:0] | | | Section 8.2.2 | |
| 02h | Offset | MODE | OFFSET[6:0] | | | | | | | | Section 8.2.3 |
| 03h | RAM_byte | B[7:0] | | | | | | | | | Section 8.2.4 |
| Time and date registers | | | | | | | | | | | |
| 04h | Seconds | OS | SECONDS (0 to 59) | | | | | | | | Section 8.3.1 |
| 05h | Minutes | - | MINUTES (0 to 59) | | | | | | | | Section 8.3.2 |
| 06h | Hours | - | - | AMPM | HOURS (1 to 12) in 12-hour mode | | | | | | Section 8.3.3 |
| | | | | HOURS (0 to 23) in 24-hour mode | | | | | | | |
| 07h | Days | - | - | DAYS (1 to 31) | | | | | | | Section 8.3.4 |
| 08h | Weekdays | - | - | - | - | - | WEEKDAYS (0 to 6) | | | | Section 8.3.5 |
| 09h | Months | - | - | - | MONTHS (1 to 12) | | | | | | Section 8.3.6 |
| 0Ah | Years | YEARS (0 to 99) | | | | | | | | | Section 8.3.7 |
| Alarm registers | | | | | | | | | | | |
| 0Bh | Second_alarm | AEN_S | SECOND_ALARM (0 to 59) | | | | | | | | Section 8.5.1 |
| 0Ch | Minute_alarm | AEN_M | MINUTE_ALARM (0 to 59) | | | | | | | | Section 8.5.2 |
| 0Dh | Hour_alarm | AEN_H | - | AMPM | HOUR_ALARM (1 to 12) in 12-hour mode | | | | | | Section 8.5.3 |
| | | | | HOUR_ALARM (0 to 23) in 24-hour mode | | | | | | | |
| 0Eh | Day_alarm | AEN_D | - | DAY_ALARM (1 to 31) | | | | | | | Section 8.5.4 |
| 0Fh | Weekday_alarm | AEN_W | - | - | - | - | WEEKDAY_ALARM (0 to 6) | | | | Section 8.5.5 |
| Timer registers | | | | | | | | | | | |
| 10h | Timer_value | T[7:0] | | | | | | | | | Section 8.6.1 |
| 11h | Timer_mode | - | - | - | TCF[1:0] | | TE | TIE | TI_TP | Section 8.6.2 | |

8.2 Control registers

To ensure that all control registers will be set to their default values, the V_{DD} level must be at zero volts at initial power-up. If this is not possible, a reset must be initiated with the software reset command when power is stable. Refer to [Section 8.2.1.3](#) for details.

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

| Bit | Symbol | Value | Description | Reference |
|-----|----------|------------------|--|--|
| 7 | EXT_TEST | | external clock test mode | Section 8.2.1.1 |
| | | 0 ^[1] | normal mode | |
| | | 1 | external clock test mode | |
| 6 | - | 0 | unused | - |
| 5 | STOP | | STOP bit | Section 8.2.1.2 |
| | | 0 ^[1] | RTC clock runs | |
| | | 1 | RTC clock is stopped; all RTC divider chain flip-flops are asynchronously set logic 0 | |
| 4 | SR | | software reset | Section 8.2.1.3 |
| | | 0 ^[1] | no software reset | |
| | | 1 | initiate software reset ^[2] ; this bit always returns a 0 when read | |
| 3 | - | 0 | unused | - |
| 2 | CIE | | correction interrupt enable | Section 8.2.3 |
| | | 0 ^[1] | no correction interrupt generated | |
| | | 1 | interrupt pulses are generated at every correction cycle | |
| 1 | 12_24 | | 12 or 24-hour mode | Section 8.3.3 Section 8.5.3 |
| | | 0 ^[1] | 24-hour mode is selected | |
| | | 1 | 12-hour mode is selected | |
| 0 | CAP_SEL | | internal oscillator capacitor selection for quartz crystals with a corresponding load capacitance | - |
| | | 0 ^[1] | 7 pF | |
| | | 1 | 12.5 pF | |

[1] Default value.

[2] For a software reset, 01011000 (58h) must be sent to register Control_1 (see [Section 8.2.1.3](#)).

8.2.1.1 EXT_TEST: external clock test mode

A test mode is available which allows for on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST in register Control_1. Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal with the signal applied to pin CLKOUT.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1 000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2⁶ divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (register Control_1, bit STOP = 1).
3. Clear STOP (register Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

8.2.1.2 STOP: STOP bit function

The function of the STOP bit (see [Figure 4](#)) is to allow for accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F₂ to F₁₄) to be held in reset and thus no 1 Hz ticks are generated. It also stops the output of clock frequencies below 8 kHz on pin CLKOUT.

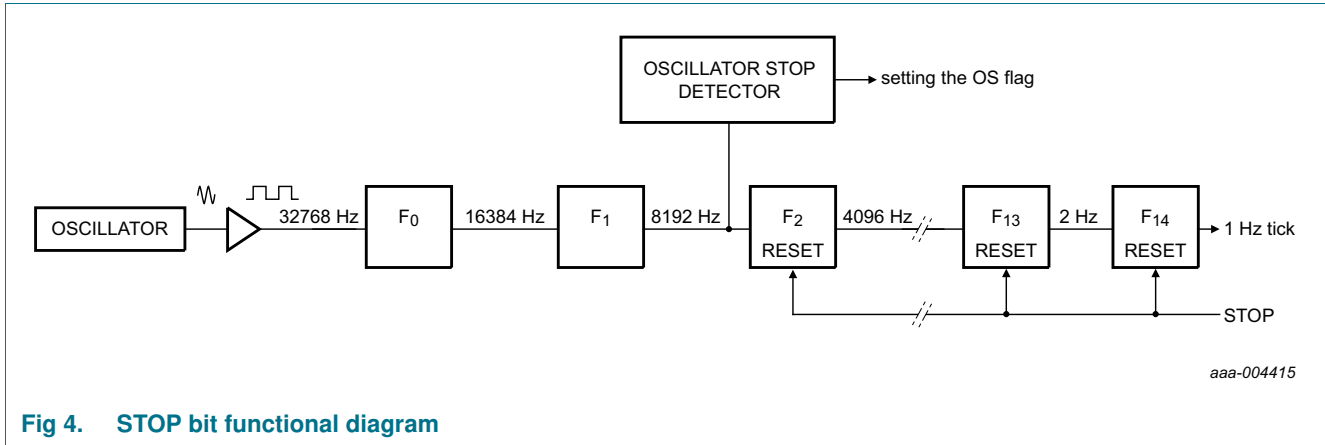


Fig 4. STOP bit functional diagram

The time circuits can then be set and do not increment until the STOP bit is released (see [Figure 5](#) and [Table 7](#)).

Table 7. First increment of time circuits after STOP bit release

| Bit | Prescaler bits | [1] 1 Hz tick | Time | Comment |
|--|--|---------------|----------|---|
| STOP | F ₀ F ₁ -F ₂ to F ₁₄ | | hh:mm:ss | |
| Clock is running normally | | | | |
| 0 | 01-0 0001 1101 0100 | | 12:45:12 | prescaler counting normally |
| STOP bit is activated by user. F₀F₁ are not reset and values cannot be predicted externally | | | | |
| 1 | XX-0 0000 0000 0000 | | 12:45:12 | prescaler is reset; time circuits are frozen |
| New time is set by user | | | | |
| 1 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is reset; time circuits are frozen |
| STOP bit is released by user | | | | |
| 0 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is now running |
| | XX-1 0000 0000 0000 | | 08:00:00 | - |
| | XX-0 1000 0000 0000 | | 08:00:00 | - |
| | XX-1 1000 0000 0000 | | 08:00:00 | - |
| | : | | : | - |
| | 11-1 1111 1111 1110 | | 08:00:00 | - |
| | 00-0 0000 0000 0001 | | 08:00:01 | 0 to 1 transition of F ₁₄ increments the time circuits |
| | 10-0 0000 0000 0001 | | 08:00:01 | - |
| | : | | : | - |
| | 11-1 1111 1111 1111 | | 08:00:01 | - |
| | 00-0 0000 0000 0000 | | 08:00:01 | - |
| | 10-0 0000 0000 0000 | | 08:00:01 | - |
| | : | | : | - |
| | 11-1 1111 1111 1110 | | 08:00:01 | - |
| | 00-0 0000 0000 0001 | | 08:00:02 | 0 to 1 transition of F ₁₄ increments the time circuits |

[1] F₀ is clocked at 32.768 kHz.

The lower two stages of the prescaler (F₀ and F₁) are not reset. And because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle (see [Figure 5](#)).

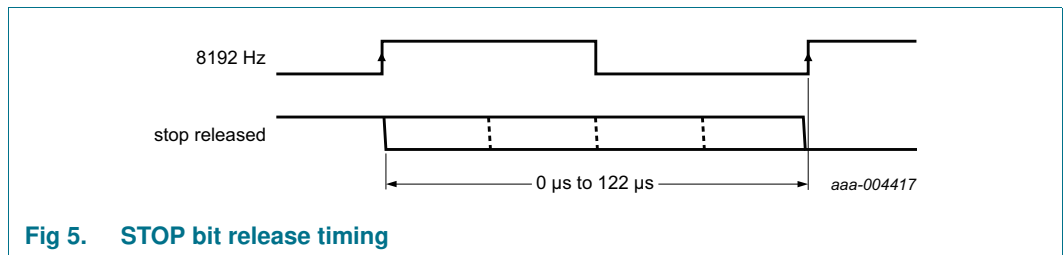
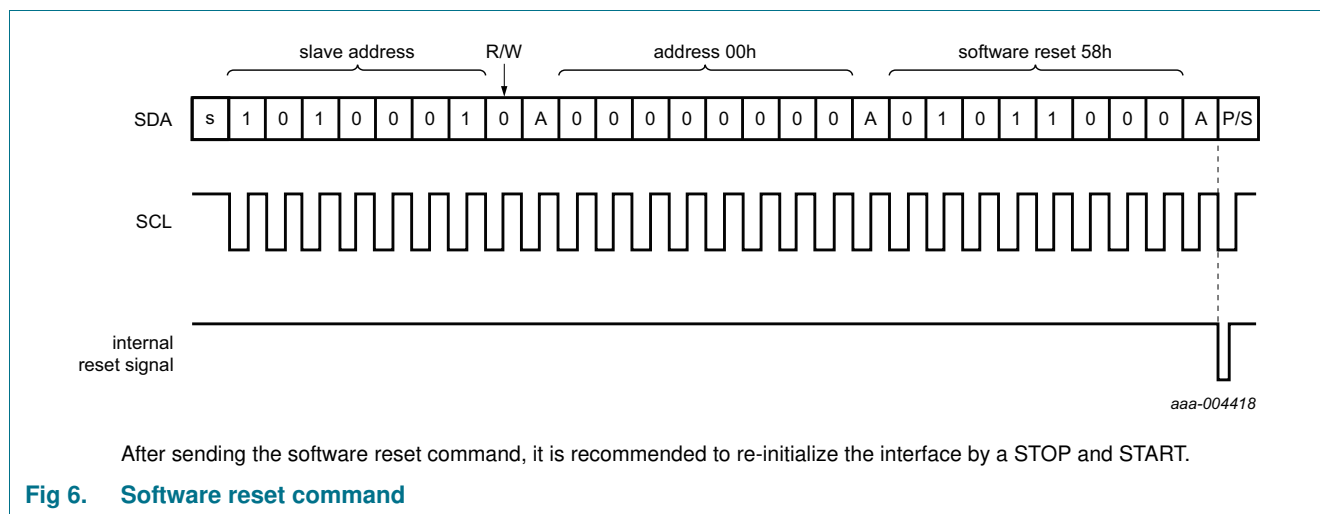


Fig 5. STOP bit release timing

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F₀ and F₁ not being reset (see [Table 7](#)) and the unknown state of the 32 kHz clock.

8.2.1.3 Software reset

A reset is automatically generated at power-on. There is a low probability that some devices will have corruption of the registers after the automatic power-on reset if the device is powered up with a residual V_{DD} level. It is required that the V_{DD} starts at zero volts at power up or upon power cycling to ensure that there is no corruption of the registers. If this is not possible, a reset must be initiated after power-up (i.e. when power is stable) with the software reset command. Software reset command means setting bits 6, 4, and 3 in register Control_1 (00h) logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see [Figure 6](#).



In reset state, all registers are set according to [Table 8](#) and the address pointer returns to address 00h.

Table 8. Registers reset values

| Address | Register name | Bit | | | | | | | |
|---------|---------------|-----|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00h | Control_1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01h | Control_2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | Offset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03h | RAM_byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | Seconds | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05h | Minutes | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06h | Hours | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07h | Days | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 08h | Weekdays | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 09h | Months | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0Ah | Years | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | Second_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ch | Minute_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | Hour_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Eh | Day_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 8. Registers reset values ...continued

| Address | Register name | Bit | | | | | | | |
|---------|---------------|-----|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0Fh | Weekday_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10h | Timer_value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11h | Timer_mode | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

The PCA85063A resets to:

Time — 00:00:00

Date — 20000101

Weekday — Saturday

8.2.2 Register Control_2

Table 9. Control_2 - control and status register 2 (address 01h) bit description

| Bit | Symbol | Value | Description | Reference |
|--------|----------|------------------------------|---|---|
| 7 | AIE | | alarm interrupt | Section 8.2.2.1 Section 8.5.6 |
| | | 0 ^[1] | disabled | |
| | | 1 | enabled | |
| 6 | AF | | alarm flag | Section 8.2.2.1 Section 8.5.6 |
| | | 0 ^[1] | read: alarm flag inactive write: alarm flag is cleared | |
| | | 1 | read: alarm flag active | |
| | | | write: alarm flag remains unchanged | |
| 5 | MI | | minute interrupt | Section 8.2.2.2 Section 8.2.2.3 |
| | | 0 ^[1] | disabled | |
| | | 1 | enabled | |
| 4 | HMI | | half minute interrupt | Section 8.2.2.2 Section 8.2.2.3 |
| | | 0 ^[1] | disabled | |
| | | 1 | enabled | |
| 3 | TF | | timer flag | Section 8.2.2.1 Section 8.2.2.3 Section 8.6.3 |
| | | 0 ^[1] | no timer interrupt generated | |
| | | 1 | flag set when timer interrupt generated | |
| 2 to 0 | COF[2:0] | see Table 11 | CLKOUT control | Section 8.2.2.4 |

[1] Default value.

8.2.2.1 Alarm interrupt

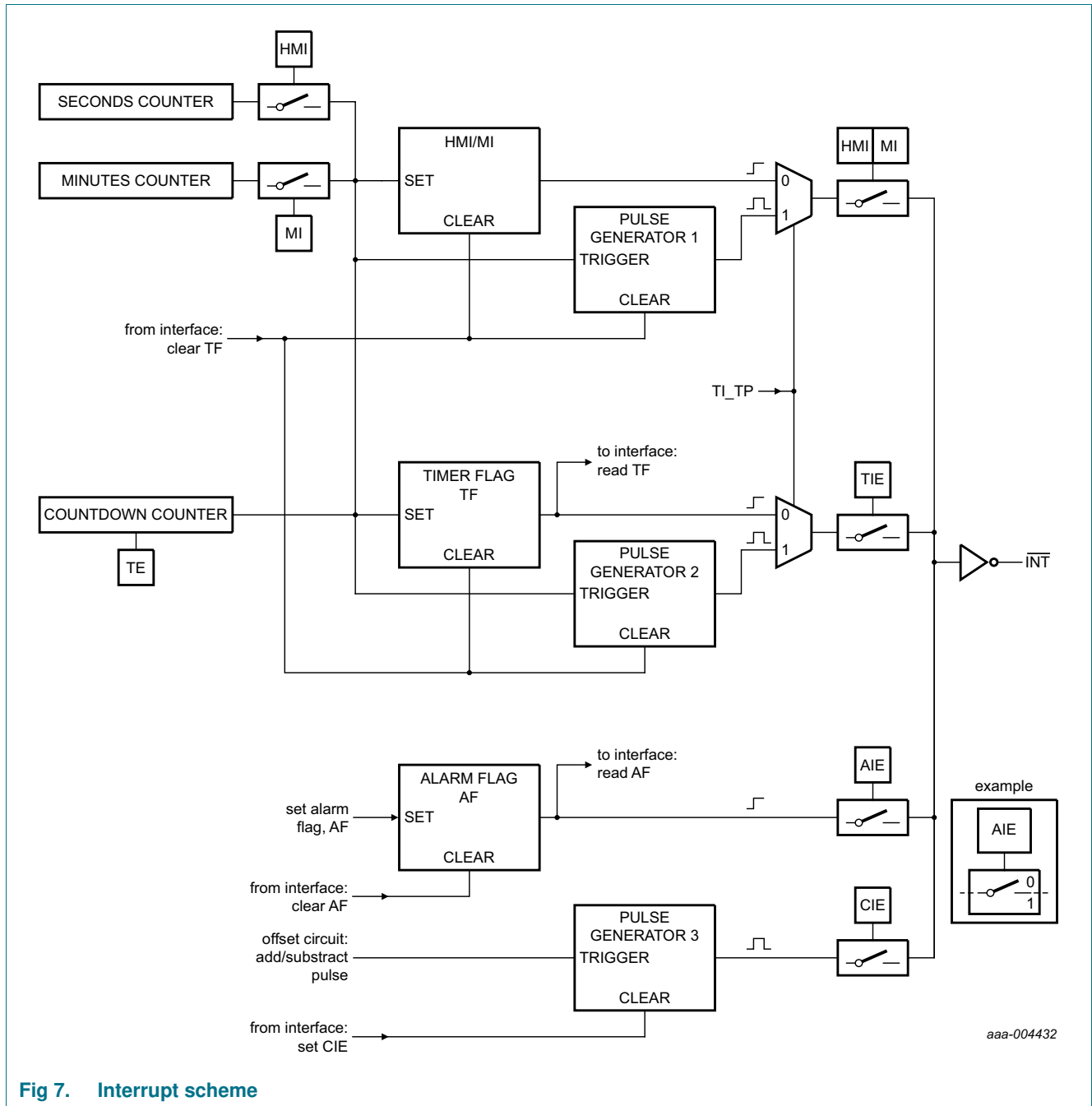


Fig 7. Interrupt scheme

AIE: This bit activates or deactivates the generation of an interrupt when AF is asserted, respectively.

AF: When an alarm occurs, AF is set logic 1. This bit maintains its value until overwritten by command. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

8.2.2.2 MI and HMI: minute and half minute interrupt

The minute interrupt (bit MI) and half minute interrupt (bit HMI) are pre-defined timers for generating interrupt pulses on pin $\overline{\text{INT}}$; see Figure 8. The timers are running in sync with the seconds counter (see Table 19 on page 19).

The minute and half minute interrupts must only be used when the frequency offset is set to normal mode (MODE = 0), see Section 8.2.3. In normal mode, the interrupt pulses on pin $\overline{\text{INT}}$ are $\frac{1}{64}$ s wide.

When starting MI, the first interrupt will be generated after 1 second to 59 seconds. When starting HMI, the first interrupt will be generated after 1 second to 29 seconds. Subsequent periods do not have such a delay. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a half minute interrupt is not distinguishable.

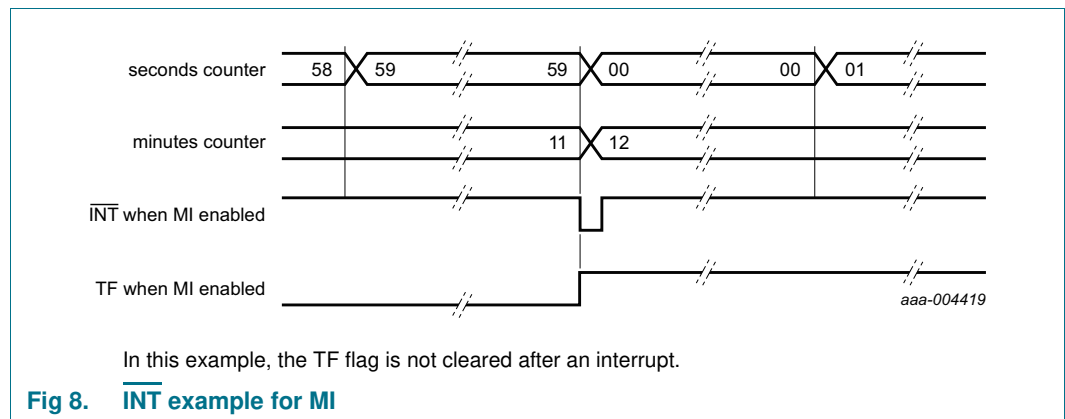


Table 10. Effect of bits MI and HMI on $\overline{\text{INT}}$ generation

| Minute interrupt (bit MI) | Half minute interrupt (bit HMI) | Result |
|---------------------------|---------------------------------|---------------------------|
| 0 | 0 | no interrupt generated |
| 1 | 0 | an interrupt every minute |
| 0 | 1 | an interrupt every 30 s |
| 1 | 1 | an interrupt every 30 s |

The duration of the timer is affected by the register Offset (see Section 8.2.3). Only when OFFSET[6:0] has the value 00h the periods are consistent.

8.2.2.3 TF: timer flag

The timer flag (bit TF) is set logic 1 on the first trigger of MI, HMI, or the countdown timer. The purpose of the flag is to allow the controlling system to interrogate what caused the interrupt: timer or alarm. The flag can be read and cleared by command.

The status of the timer flag TF can affect the $\overline{\text{INT}}$ pulse generation depending on the setting of TI_TP (see Section 8.6.2 “Register Timer mode” on page 28):

- When TI_TP is set logic 1
 - an $\overline{\text{INT}}$ pulse is generated independent of the status of the timer flag TF
 - TF stays set until it is cleared
 - TF does not affect $\overline{\text{INT}}$

- the countdown timer runs in a repetitive loop and keeps generating timed periods
- When TI_TP is set logic 0
 - the $\overline{\text{INT}}$ generation follows the TF flag
 - TF stays set until it is cleared
 - If TF is not cleared before the next coming interrupt, no $\overline{\text{INT}}$ is generated
 - the countdown timer stops after the first countdown

8.2.2.4 COF[2:0]: Clock output frequency

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Control_2. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is a push-pull output and enabled at power-on. CLKOUT can be disabled by setting COF[2:0] to 111. When disabled, the CLKOUT is LOW.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all clock frequencies except 32.768 kHz have a duty cycle of 50 : 50.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped. For more details of the STOP bit function, see [Section 8.2.1.2](#).

Table 11. CLKOUT frequency selection

| COF[2:0] | CLKOUT frequency (Hz) | Typical duty cycle ^[1] | Effect of STOP bit |
|--------------------|-----------------------|-----------------------------------|--------------------|
| 000 ^[2] | 32768 | 60 : 40 to 40 : 60 | no effect |
| 001 | 16384 | 50 : 50 | no effect |
| 010 | 8192 | 50 : 50 | no effect |
| 011 | 4096 | 50 : 50 | CLKOUT = LOW |
| 100 | 2048 | 50 : 50 | CLKOUT = LOW |
| 101 | 1024 | 50 : 50 | CLKOUT = LOW |
| 110 | 1 ^[3] | 50 : 50 | CLKOUT = LOW |
| 111 | CLKOUT = LOW | - | - |

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] 1 Hz clock pulses are affected by offset correction pulses.

8.2.3 Register Offset

The PCA85063A incorporates an offset register (address 02h) which can be used to implement several functions, such as:

- Accuracy tuning
- Aging adjustment
- Temperature compensation

Table 12. Offset - offset register (address 02h) bit description

| Bit | Symbol | Value | Description |
|--------|-------------|------------------------------|--|
| 7 | MODE | | offset mode |
| | | 0 ^[1] | normal mode: offset is made once every two hours |
| | | 1 | course mode: offset is made every 4 minutes |
| 6 to 0 | OFFSET[6:0] | see Table 13 | offset value |

[1] Default value.

For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB.

Table 13. Offset values

| OFFSET[6:0] | Offset value in decimal | Offset value in ppm | |
|------------------------|-------------------------|-------------------------|-----------------------|
| | | Normal mode MODE = 0 | Fast mode MODE = 1 |
| 0111111 | +63 | +273.420 | +256.347 |
| 0111110 | +62 | +269.080 | +252.278 |
| : | : | : | : |
| 0000010 | +2 | +8.680 | +8.138 |
| 0000001 | +1 | +4.340 | +4.069 |
| 0000000 ^[1] | 0 | 0 ^[1] | 0 ^[1] |
| 1111111 | -1 | -4.340 | -4.069 |
| 1111110 | -2 | -8.680 | -8.138 |
| : | : | : | : |
| 1000001 | -63 | -273.420 | -256.347 |
| 1000000 | -64 | -277.760 | -260.416 |

[1] Default value.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second but not by changing the oscillator frequency.

It is possible to monitor when correction pulses are applied. To enable correction interrupt generation, bit CIE (register Control_1) has to be set logic 1. At every correction cycle, a pulse is generated on pin INT. The pulse width depends on the correction mode. If multiple correction pulses are applied, an interrupt pulse is generated for each correction pulse applied.

8.2.3.1 Correction when MODE = 0

The correction is triggered once every two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 14. Correction pulses for MODE = 0

| Correction value | Update every n th hour | Minute | Correction pulses on $\overline{\text{INT}}$ per minute ^[1] |
|------------------|-----------------------------------|-------------------|--|
| +1 or -1 | 2 | 00 | 1 |
| +2 or -2 | 2 | 00 and 01 | 1 |
| +3 or -3 | 2 | 00, 01, and 02 | 1 |
| : | : | : | : |
| +59 or -59 | 2 | 00 to 58 | 1 |
| +60 or -60 | 2 | 00 to 59 | 1 |
| +61 or -61 | 2 | 00 to 59 | 1 |
| | | 2nd and next hour | 00 |
| +62 or -62 | 2 | 00 to 59 | 1 |
| | | 2nd and next hour | 00 and 01 |
| +63 or -63 | 02 | 00 to 59 | 1 |
| | | 2nd and next hour | 00, 01, and 02 |
| -64 | 02 | 00 to 59 | 1 |
| | | 2nd and next hour | 00, 01, 02, and 03 |

[1] The correction pulses on pin $\overline{\text{INT}}$ are $\frac{1}{64}$ s wide.

In MODE = 0, any timer or clock output using a frequency below 64 Hz is affected by the clock correction (see [Table 15](#)).

Table 15. Effect of correction pulses on frequencies for MODE = 0

| Frequency (Hz) | Effect of correction |
|---------------------------|----------------------|
| CLKOUT | |
| 32768 | no effect |
| 16384 | no effect |
| 8192 | no effect |
| 4096 | no effect |
| 2048 | no effect |
| 1024 | no effect |
| 1 | affected |
| Timer source clock | |
| 4096 | no effect |
| 64 | no effect |
| 1 | affected |
| $\frac{1}{60}$ | affected |

8.2.3.2 Correction when MODE = 1

The correction is triggered once every four minutes and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Table 16. Correction pulses for MODE = 1

| Correction value | Update every n th minute | Second | Correction pulses on INT per second ^[1] |
|------------------|-------------------------------------|----------------|--|
| +1 or -1 | 2 | 00 | 1 |
| +2 or -2 | 2 | 00 and 01 | 1 |
| +3 or -3 | 2 | 00, 01, and 02 | 1 |
| : | : | : | : |
| +59 or -59 | 2 | 00 to 58 | 1 |
| +60 or -60 | 2 | 00 to 59 | 1 |
| +61 or -61 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 2 |
| +62 or -62 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 3 |
| +63 or -63 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 4 |
| -64 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 5 |

[1] The correction pulses on pin INT are 1/1024 s wide. For multiple pulses, they are repeated at an interval of 1/512 s.

In MODE = 1, any timer source clock using a frequency below 1.024 kHz is also affected by the clock correction (see Table 17).

Table 17. Effect of correction pulses on frequencies for MODE = 1

| Frequency (Hz) | Effect of correction |
|---------------------------|----------------------|
| CLKOUT | |
| 32768 | no effect |
| 16384 | no effect |
| 8192 | no effect |
| 4096 | no effect |
| 2048 | no effect |
| 1024 | no effect |
| 1 | affected |
| Timer source clock | |
| 4096 | no effect |
| 64 | affected |
| 1 | affected |
| 1/60 | affected |

8.2.3.3 Offset calibration workflow

The calibration offset has to be calculated based on the time. [Figure 9](#) shows the workflow how the offset register values can be calculated:

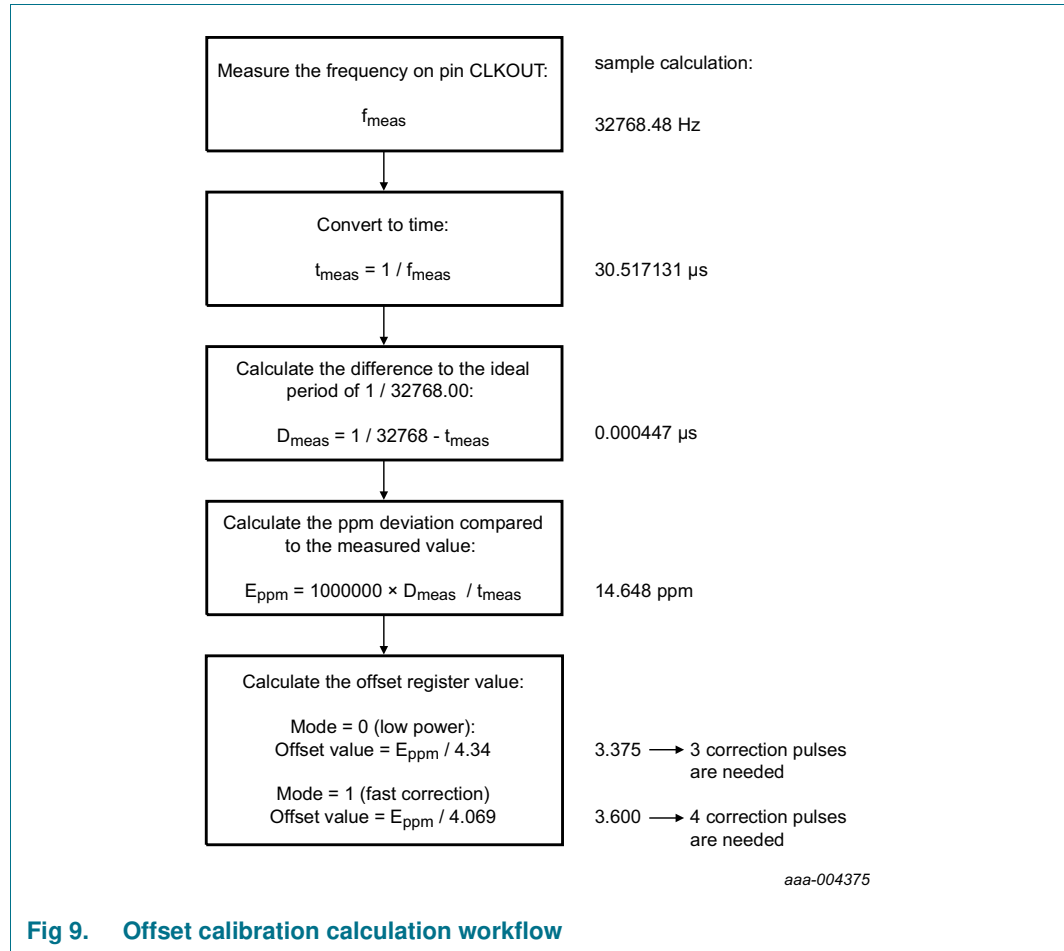
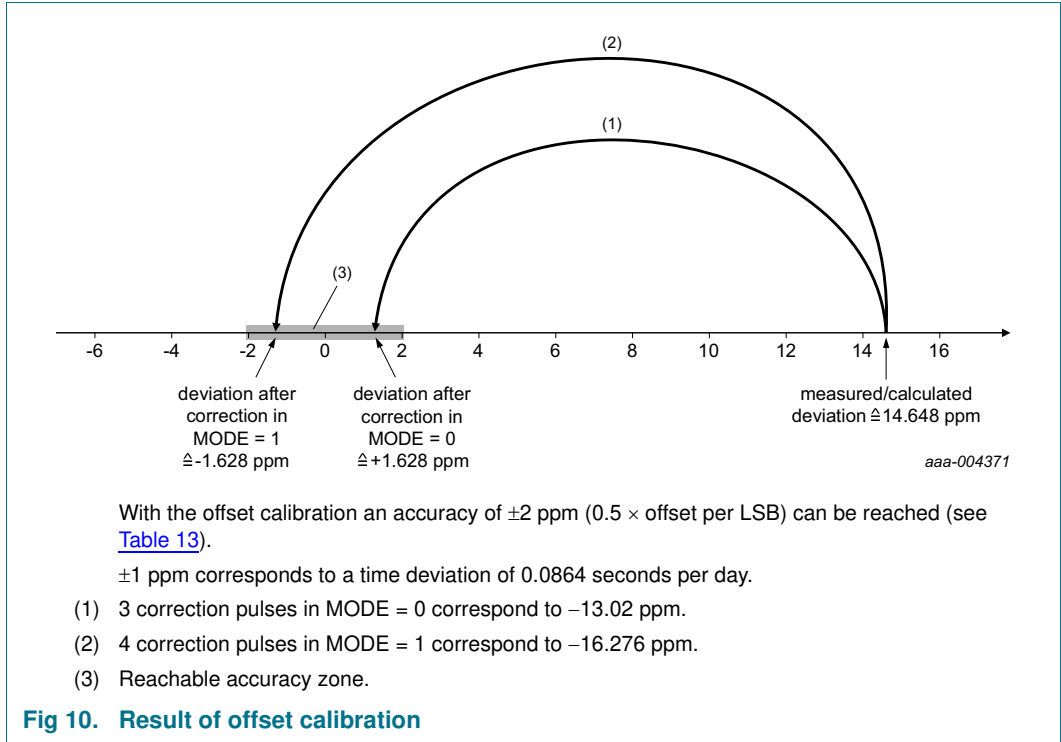


Fig 9. Offset calibration calculation workflow



8.2.4 Register RAM_byte

The PCA85063A provides a free RAM byte, which can be used for any purpose, for example, status byte of the system.

Table 18. RAM_byte - 8-bit RAM register (address 03h) bit description

| Bit | Symbol | Value | Description |
|--------|--------|-------------------------------------|-------------|
| 7 to 0 | B[7:0] | 00000000 ^[1] to 11111111 | RAM content |

[1] Default value.

8.3 Time and date registers

Most of the registers are coded in the BCD format to simplify application use.

8.3.1 Register Seconds

Table 19. Seconds - seconds register (address 04h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------|-----------------------|-------------|---|
| 7 | OS | | | oscillator stop |
| | | 0 | - | clock integrity is guaranteed |
| | | 1 ^[1] | - | clock integrity is not guaranteed; oscillator has stopped or has been interrupted |
| 6 to 4 | SECONDS | 0 ^[1] to 5 | ten's place | actual seconds coded in BCD format, see Table 20 |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

Table 20. Seconds coded in BCD format

| Seconds value in decimal | Upper-digit (ten's place) | | | Digit (unit place) | | | |
|--------------------------|---------------------------|-------|-------|--------------------|-------|-------|-------|
| | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 ^[1] | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 02 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| : | : | : | : | : | : | : | : |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| : | : | : | : | : | : | : | : |
| 58 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 59 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

[1] Default value.

8.3.1.1 OS: Oscillator stop

When the oscillator of the PCA85063A is stopped, the OS flag is set. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSC1 or OSC0 to ground. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature, and supply voltage.

The flag remains set until cleared by command (see Figure 11). If the flag cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

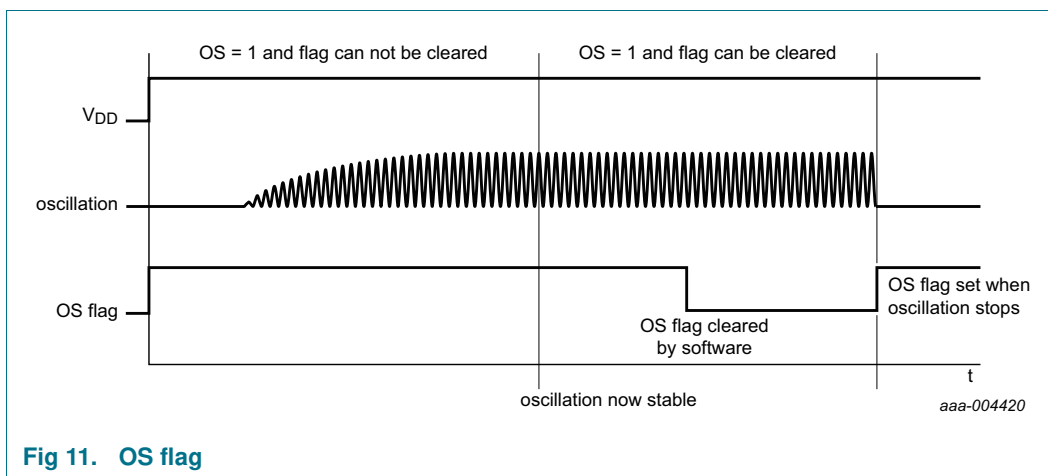


Fig 11. OS flag

8.3.2 Register Minutes

Table 21. Minutes - minutes register (address 05h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------|-----------------------|-------------|---|
| 7 | - | 0 | - | unused |
| 6 to 4 | MINUTES | 0 ^[1] to 5 | ten's place | actual minutes coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.3.3 Register Hours

Table 22. Hours - hours register (address 06h) bit description

| Bit | Symbol | Value | Place value | Description |
|-----------------------------------|--------|-----------------------|-------------|---|
| 7 to 6 | - | 00 | - | unused |
| 12-hour mode^[1] | | | | |
| 5 | AMPM | | | AM/PM indicator |
| | | 0 ^[2] | - | AM |
| | | 1 | - | PM |
| 4 | HOURS | 0 ^[2] to 1 | ten's place | actual hours in 12-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[2] to 9 | unit place | |
| 24-hour mode^[1] | | | | |
| 5 to 4 | HOURS | 0 ^[2] to 2 | ten's place | actual hours in 24-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[2] to 9 | unit place | |

[1] Hour mode is set by the 12_24 bit in register Control_1.

[2] Default value.

8.3.4 Register Days

Table 23. Days - days register (address 07h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------------------|-----------------------|-------------|---------------------------------------|
| 7 to 6 | - | 00 | - | unused |
| 5 to 4 | DAYS ^[1] | 0 ^[2] to 3 | ten's place | actual day coded in BCD format |
| 3 to 0 | | 0 ^[3] to 9 | unit place | |

[1] If the year counter contains a value, which is exactly divisible by 4 (including the year 00), the PCA85063A compensates for leap years by adding a 29th day to February.

[2] Default value.

[3] Default value is 1.

8.3.5 Register Weekdays

Table 24. Weekdays - weekdays register (address 08h) bit description

| Bit | Symbol | Value | Description |
|--------|----------|--------|--|
| 7 to 3 | - | 00000 | unused |
| 2 to 0 | WEEKDAYS | 0 to 6 | actual weekday values, see Table 25 |

Table 25. Weekday assignments

| Day ^[1] | Bit | | |
|-------------------------|-----|---|---|
| | 2 | 1 | 0 |
| Sunday | 0 | 0 | 0 |
| Monday | 0 | 0 | 1 |
| Tuesday | 0 | 1 | 0 |
| Wednesday | 0 | 1 | 1 |
| Thursday | 1 | 0 | 0 |
| Friday | 1 | 0 | 1 |
| Saturday ^[2] | 1 | 1 | 0 |

[1] Definition may be reassigned by the user.

[2] Default value.

8.3.6 Register Months

Table 26. Months - months register (address 09h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------|--------|-------------|---|
| 7 to 5 | - | 000 | - | unused |
| 4 | MONTHS | 0 to 1 | ten's place | actual month coded in BCD format, see Table 27 |
| 3 to 0 | | 0 to 9 | unit place | |

Table 27. Month assignments in BCD format

| Month | Upper-digit (ten's place) | Digit (unit place) | | | |
|------------------------|------------------------------|--------------------|-------|-------|-------|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| January ^[1] | 0 | 0 | 0 | 0 | 1 |
| February | 0 | 0 | 0 | 1 | 0 |
| March | 0 | 0 | 0 | 1 | 1 |
| April | 0 | 0 | 1 | 0 | 0 |
| May | 0 | 0 | 1 | 0 | 1 |
| June | 0 | 0 | 1 | 1 | 0 |
| July | 0 | 0 | 1 | 1 | 1 |
| August | 0 | 1 | 0 | 0 | 0 |
| September | 0 | 1 | 0 | 0 | 1 |
| October | 1 | 0 | 0 | 0 | 0 |
| November | 1 | 0 | 0 | 0 | 1 |
| December | 1 | 0 | 0 | 1 | 0 |

[1] Default value.

8.3.7 Register Years

Table 28. Years - years register (0Ah) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------|-----------|-------------|---------------------------------|
| 7 to 4 | YEARS | 0[1] to 9 | ten's place | actual year coded in BCD format |
| 3 to 0 | | 0[1] to 9 | unit place | |

[1] Default value.

8.4 Setting and reading the time

Figure 12 shows the data flow and data dependencies starting from the 1 Hz clock tick.

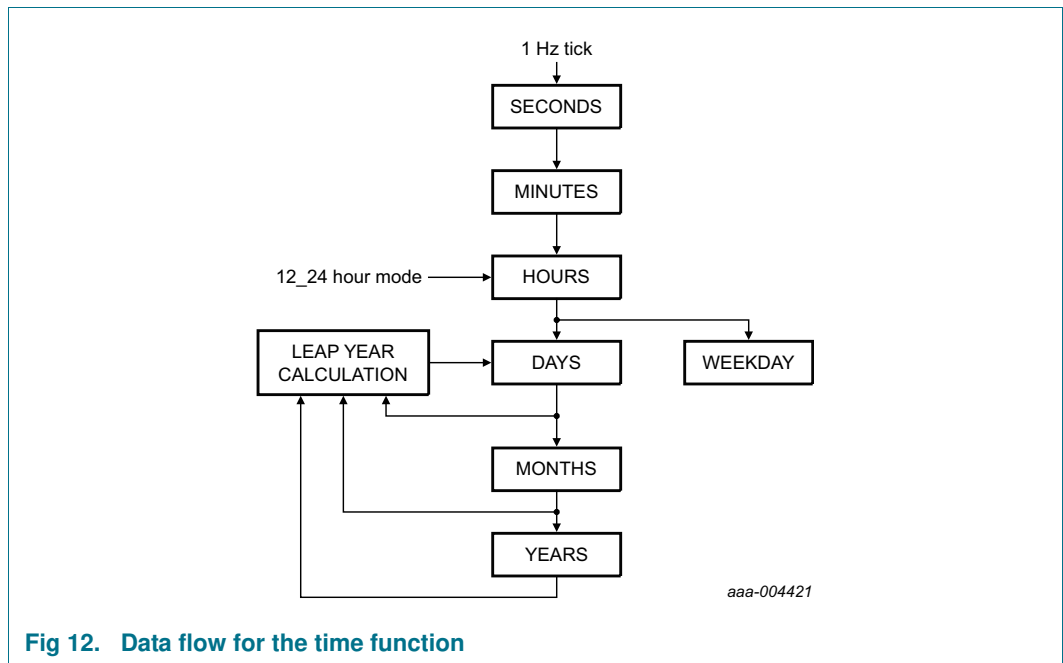


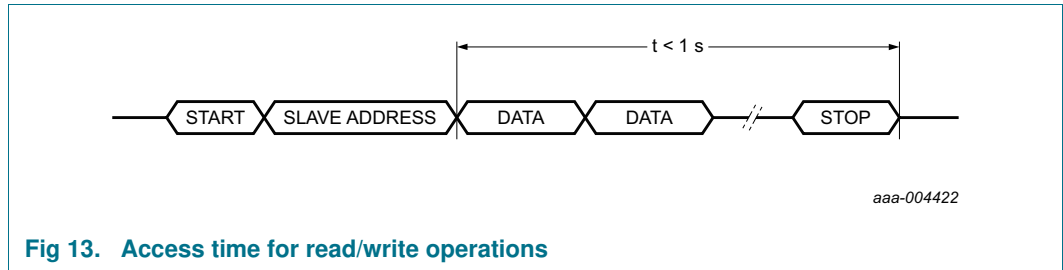
Fig 12. Data flow for the time function

During read/write operations, the time counting circuits (memory locations 04h through 0Ah) are blocked.

The blocking prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 13).



Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address (see [Table 39 on page 33](#)) for write (A2h)
2. Set the address pointer to 4 (Seconds) by sending 04h
3. Send a RESTART condition or STOP followed by START
4. Send the slave address for read (A3h)
5. Read Seconds
6. Read Minutes
7. Read Hours
8. Read Days
9. Read Weekdays
10. Read Months
11. Read Years
12. Send a STOP condition

8.5 Alarm registers

8.5.1 Register Second_alarm

Table 29. Second_alarm - second alarm register (address 0Bh) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------------|-----------------------|-------------|--|
| 7 | AEN_S | | | second alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 to 4 | SECOND_ALARM | 0 ^[1] to 5 | ten's place | second alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.2 Register Minute_alarm

Table 30. Minute_alarm - minute alarm register (address 0Ch) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------------|-----------------------|-------------|---|
| 7 | AEN_M | | | minute alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 to 4 | MINUTE_ALARM | 0 ^[1] to 5 | ten's place | minute alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.3 Register Hour_alarm

Table 31. Hour_alarm - hour alarm register (address 0Dh) bit description

| Bit | Symbol | Value | Place value | Description |
|-----------------------------------|------------|-----------------------|-------------|---|
| 7 | AEN_H | | | hour alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 | - | 0 | - | unused |
| 12-hour mode^[2] | | | | |
| 5 | AMPM | | | AM/PM indicator |
| | | 0 ^[1] | - | AM |
| | | 1 | - | PM |
| 4 | HOUR_ALARM | 0 ^[1] to 1 | ten's place | hour alarm information in 12-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |
| 24-hour mode^[2] | | | | |
| 5 to 4 | HOUR_ALARM | 0 ^[1] to 2 | ten's place | hour alarm information in 24-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

[2] Hour mode is set by the 12_24 bit in register Control_1.

8.5.4 Register Day_alarm

Table 32. Day_alarm - day alarm register (address 0Eh) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|-----------|-----------------------|-------------|--|
| 7 | AEN_D | | | day alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 | - | 0 | - | unused |
| 5 to 4 | DAY_ALARM | 0 ^[1] to 3 | ten's place | day alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.