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# PCA8530

Automotive 102 x 4 Chip-On-Glass LCD segment driver

Rev. 2 — 25 September 2014

Product data sheet

## 1. General description

The PCA8530 is a fully featured Chip-On-Glass (COG)<sup>1</sup> Liquid Crystal Display (LCD) driver, designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:4. It generates the drive signals for a static or multiplexed LCD containing up to 4 backplane, 102 segment outputs, and up to 408 segments/elements. The PCA8530 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCA8530 offers a programmable temperature compensation of the LCD supply voltage. The PCA8530 can be easily controlled by a microcontroller through either the two-line I<sup>2</sup>C-bus or a four-line bidirectional SPI-bus.

For a selection of NXP LCD segment drivers, see [Table 58 on page 93](#).

## 2. Features and benefits

- AEC Q100 grade 2 compliant for automotive applications
- Low power consumption
- Extended operating temperature range from –40 °C to +105 °C
- 102 segments and 4 backplanes allowing to drive:
  - ◆ up to 51 7-segment numeric characters
  - ◆ up to 25 14-segment alphanumeric characters
  - ◆ any graphics of up to 408 segments/elements
- 408-bit RAM for display data storage
- Two sets of backplane outputs providing higher flexibility for optimal COG layout configurations
- Up to 4 chips can be cascaded to drive larger displays with an internally generated or externally supplied  $V_{LCD}$
- Selectable backplane drive configuration: static, 2, or 4 backplane multiplexing
- LCD supply voltage
  - ◆ Programmable internal charge pump for on-chip LCD voltage generation up to  $5 \times V_{DD2}$
  - ◆ External LCD voltage supply possible as well
- Selectable 400 kHz I<sup>2</sup>C-bus or 3 MHz SPI-bus interface
- Selectable linear temperature compensation of  $V_{LCD}$
- Selectable display bias configuration
- Wide range for digital and analog power supply: from 2.5 V to 5.5 V

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 21 on page 95](#).



- Wide LCD voltage range from 4.0 V for low threshold LCDs up to 12.0 V for high threshold twisted nematic and Vertical Alignment (VA) displays
- Display memory bank switching in static and 1:2 multiplex drive modes
- Programmable frame frequency in the range of 45 Hz to 300 Hz; factory calibrated with a tolerance of  $\pm 3$  Hz (at 80 Hz)
- Selectable inversion scheme for LCD driving waveforms: frame or n-line inversion
- Diagnostic features for status monitoring
- Integrated temperature sensor with temperature readout
- On chip calibration of internal oscillator frequency and  $V_{LCD}$
- Laser marking at the back-side of the die for traceability of the lot number, wafer number, and die position on the wafer

### 3. Applications

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- Automotive
  - ◆ Instrument clusters
  - ◆ Climate control
  - ◆ Car entertainment
  - ◆ Car radio
- Industrial
  - ◆ Consumer
  - ◆ Medical and health care
  - ◆ Measuring equipment
  - ◆ Machine control systems
  - ◆ Information boards
  - ◆ White goods
  - ◆ General-purpose display modules

## 4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8530DUG	bare die	247 bumps	PCA8530DUG

### 4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCA8530DUG/DA	PCA8530DUG/DAZ	935304675033	chips with bumps <sup>[1]</sup> in tray	1

[1] Bump hardness, see [Table 56 on page 90](#).

## 5. Marking

Table 3. Marking codes

Product type number	Marking code
PCA8530DUG/DA	on the active side of the die PC8530-1 on the rear side of the die <sup>[1]</sup> LLLLLL WW XXXXXX

[1] The rear side marking has the following meaning:

**LLLLLL** — wafer lot number

**WW** — wafer number

**XXXXXX** — die identification number



6. Block diagram

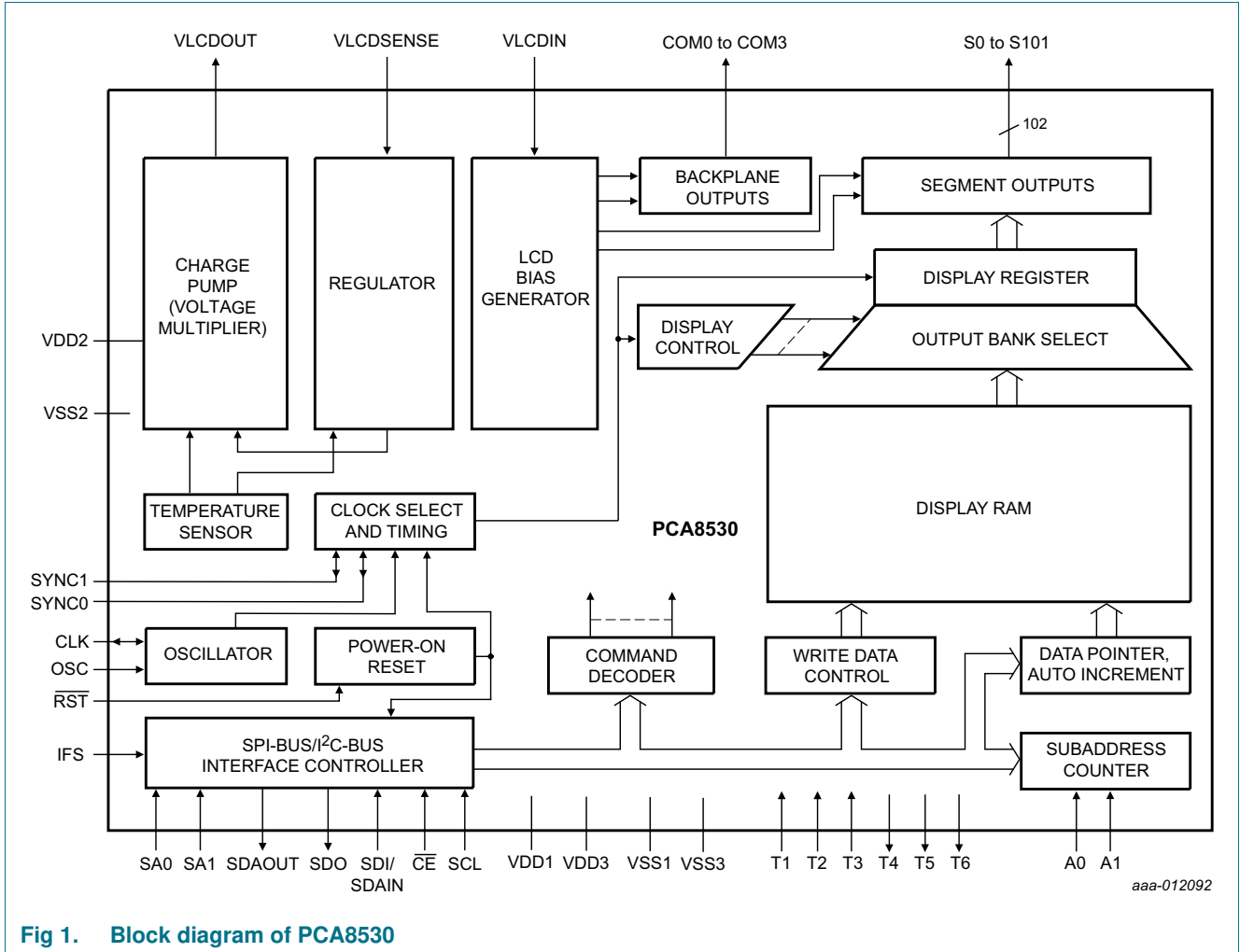
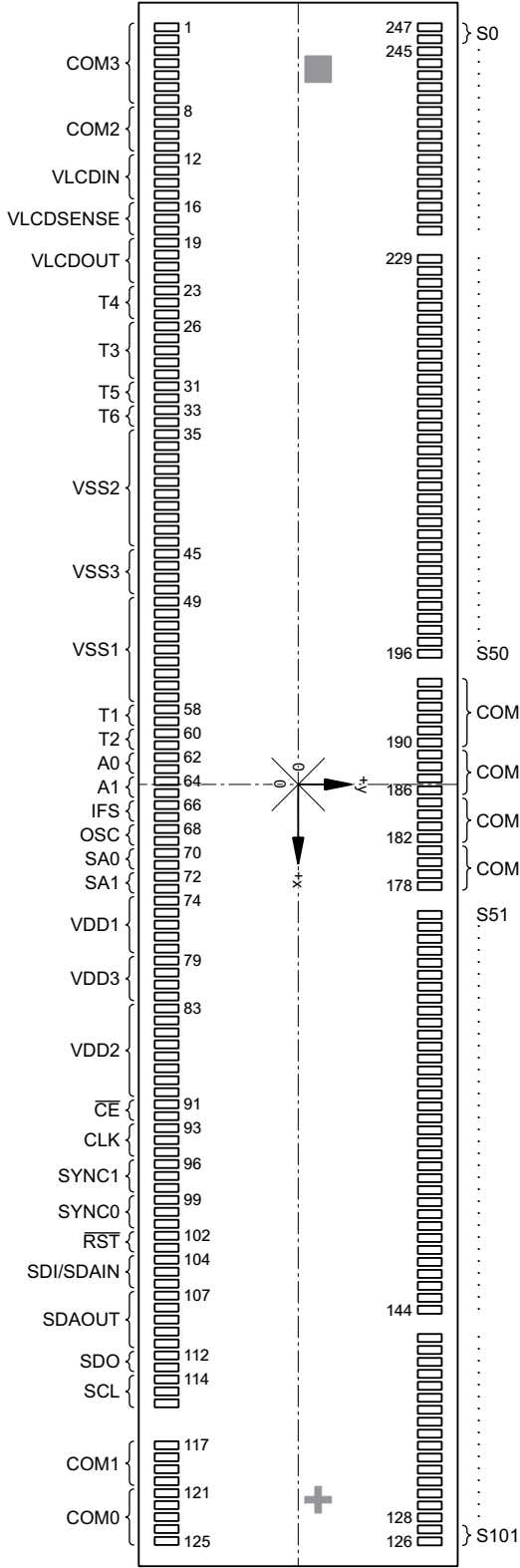


Fig 1. Block diagram of PCA8530

## 7. Pinning information

### 7.1 Pinning



aaa-012091

Viewed from active side. For mechanical details, see [Figure 59 on page 85](#).

Fig 2. Pinning diagram of PCA8530DUG

## 7.2 Pin description

**Table 4. Pin description**

Input or input/output pins must always be at a defined level ( $V_{SS}$  or  $V_{DD}$ ) unless otherwise specified.

Symbol	Pin	Type	Description
<b>Backplane output pins</b>			
COM3	1 to 7, 190 to 195	output	LCD backplane
COM2	8 to 11, 186 to 189		
COM1	117 to 120, 182 to 185		
COM0	121 to 125, 178 to 181		
<b>Segment output pins</b>			
S101	126, 127	output	LCD segment
S100 to S51	128 to 177		
S50 to S1	196 to 245		
S0	246, 247		
<b><math>V_{LCD}</math> pins</b>			
VLCDIN	12 to 15	supply	$V_{LCD}$ input
VLCDSENSE	16 to 18	input	$V_{LCD}$ regulation input
VLCDOUT	19 to 22	output	$V_{LCD}$ output
<b>Test pins</b>			
T4	23 to 25	output	not accessible; must be left open
T3	26 to 30	input	not accessible; must be connected to T5
T5	31, 32	output	not accessible; must be connected to T3
T6	33, 34	output	not accessible; must be left open
T1	58, 59	input	not accessible; must be connected to $V_{SS1}$
T2	60, 61		
<b>Supply pins</b>			
VSS2 <sup>[1]</sup>	35 to 44	supply	ground supply
VSS3 <sup>[1]</sup>	45 to 48		
VSS1 <sup>[1]</sup>	49 to 57		
VDD1	74 to 78	supply	supply voltage 1 (analog and digital)
VDD3	79 to 82	supply	supply voltage 3 (analog)
VDD2	83 to 90	supply	supply voltage 2 (charge pump)
<b>Oscillator, synchronization, addressing, and reset pins</b>			
CLK <sup>[2]</sup>	93 to 95	input/output	internal oscillator output, external oscillator input
OSC <sup>[2]</sup>	68, 69	input	clock (internal/external) selector
SYNC1 <sup>[3]</sup>	96 to 98	input/output	charge pump synchronization for cascaded devices; must not be connected if $V_{LCD}$ is externally supplied
SYNC0 <sup>[3]</sup>	99 to 101	input/output	display synchronization for cascaded devices
$\overline{RST}$	102, 103	input	active LOW reset input
A0	62, 63	input	hardware device address selection for cascading; <ul style="list-style-type: none"> <li>connect to <math>V_{SS1}</math> for logic 0</li> <li>connect to <math>V_{DD1}</math> for logic 1</li> </ul>
A1	64, 65	input	

**Table 4. Pin description ...continued**

Input or input/output pins must always be at a defined level ( $V_{SS}$  or  $V_{DD}$ ) unless otherwise specified.

Symbol	Pin	Type	Description	
<b>Bus-related pins</b>				
			SPI-bus	I <sup>2</sup> C-bus
IFS	66, 67	input	interface selector input	
			<ul style="list-style-type: none"> <li>connect to <math>V_{SS1}</math></li> </ul>	<ul style="list-style-type: none"> <li>connect to <math>V_{DD1}</math></li> </ul>
SA0	70, 71	input	unused;	slave address selector;
SA1	72, 73	input	<ul style="list-style-type: none"> <li>connect to <math>V_{SS1}</math></li> </ul>	<ul style="list-style-type: none"> <li>connect to <math>V_{SS1}</math> for logic 0</li> <li>connect to <math>V_{DD1}</math> for logic 1</li> </ul>
$\overline{CE}$	91, 92	input	chip enable input (active LOW)	unused;
				<ul style="list-style-type: none"> <li>connect to <math>V_{DD1}</math></li> </ul>
SDI/SDAIN	104 to 106	input	SPI-bus data input	I <sup>2</sup> C-bus serial data input
SDAOUT	107 to 111	output	unused;	serial data output
			<ul style="list-style-type: none"> <li>must be connected to <math>V_{SS1}</math></li> </ul>	
SDO	112, 113	output	SPI serial data output	unused;
				<ul style="list-style-type: none"> <li>must be left open</li> </ul>
SCL	114 to 116	input	serial clock input	serial clock input

[1] The substrate (rear side of the die) is connected to  $V_{SS1}$  and should be electrically isolated.

[2] If pin OSC is tied to  $V_{SS1}$ , CLK is the output pin of the internal oscillator. If pin OSC is tied to  $V_{DD1}$ , CLK is the input pin for the external oscillator.

[3] If cascading is not used, pin must be left floating; for cascading see [Section 15.2 on page 80](#).



## 8. Functional description

### 8.1 Commands of PCA8530

The PCA8530 is controlled by the commands defined in [Table 5](#).

**Remark:** Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCA8530.

**Table 5. Commands of PCA8530**

Command name	R/W <sup>[1]</sup>	Register selection RS[1:0] <sup>[2]</sup>		Command bits								Reference
				7	6	5	4	3	2	1	0	
<b>General control commands</b>												
Initialize	0	0	0	0	0	1	1	1	0	1	0	<a href="#">Section 8.2.1</a>
OTP-refresh	0	0	0	1	1	0	1	1	0	0	0	<a href="#">Section 8.2.2</a>
Device-address	0	0	0	0	0	0	1	1	0	A[1:0]		<a href="#">Section 8.2.3</a>
SYNC1_pin	0	0	0	1	0	1	1	1	0	0	OE	<a href="#">Section 8.2.4</a>
Clock-out-ctrl	0	0	0	1	1	0	1	0	1	0	COE	<a href="#">Section 8.2.5</a>
Read-select	0	0	0	0	0	0	1	1	1	0	SO	<a href="#">Section 8.2.6</a>
Status-readout	temperature	1	0	0	TD[7:0]							<a href="#">Section 8.2.7</a>
	device status				SR7	SR6	SR5	SR4	SR[3:0]			
Clear-reset-flag	0	0	0	0	0	0	1	1	1	1	1	<a href="#">Section 8.2.8</a>
<b>Charge pump and LCD bias control commands</b>												
Charge-pump-ctrl	0	0	0	1	1	0	0	CPE	CPC[2:0]		<a href="#">Section 8.3.1</a>	
Set-V <sub>LCD</sub>	MSB	0	0	0	0	1	0	V[8:4]			<a href="#">Section 8.3.2</a>	
	LSB	0	0	0	0	1	1	0	V[3:0]			
Set-bias-mode	0	0	0	1	1	0	1	0	0	B[1:0]		<a href="#">Section 8.3.3</a>

Table 5. Commands of PCA8530 ...continued

Command name		R/W <sup>[1]</sup>	Register selection RS[1:0] <sup>[2]</sup>		Command bits						Reference		
					7	6	5	4	3	2			1
<b>Temperature compensation control commands</b>													
Temperature-ctrl		0	1	0	0	0	0	0	0	TCE	TMF	TME	<a href="#">Section 8.4.1</a>
TC-slope	A	0	1	0	0	0	0	0	1	TSA[2:0]		<a href="#">Section 8.4.3</a>	
	B	0	1	0	0	0	0	1	0	TSB[2:0]			
	C	0	1	0	0	0	0	1	1	TSC[2:0]			
	D	0	1	0	0	0	1	0	0	TSD[2:0]			
	E	0	1	0	0	0	1	0	1	TSE[2:0]			
	F	0	1	0	0	0	1	1	0	TSF[2:0]			
TC-set	1	0	1	0	0	0	1	1	1	T1T[2:0]		<a href="#">Section 8.4.2</a>	
	2	0	1	0	0	1	0	0	0	T2T[2:0]			
	3	0	1	0	0	1	0	0	1	T3T[2:0]			
	4	0	1	0	0	1	0	1	0	T4T[2:0]			
<b>Display control commands</b>													
Set-MUX-mode		0	0	0	0	0	0	0	0	M[2:0]		<a href="#">Section 8.5.1</a>	
Inversion-mode		0	0	0	1	0	1	1	0	INV[2:0]		<a href="#">Section 8.5.2</a>	
Display-ctrl		0	0	0	0	0	1	1	1	0	0	DE	<a href="#">Section 8.5.3</a>
<b>Clock and frame frequency command</b>													
Frame-frequency		0	0	0	1	1	1	FF[4:0]			<a href="#">Section 8.6.4</a>		
<b>Display RAM commands</b>													
Write-display-data		0	0	1	DB[7:0]					<a href="#">Section 8.7.1</a>			
Input-bank-select		0	0	0	0	0	0	0	1	0	IB[1:0]		<a href="#">Section 8.7.2</a>
Output-bank-select		0	0	0	0	0	0	1	0	OB[1:0]			
Data-pointer-init		0	0	0	1	0	1	0	0	0	0	0	<a href="#">Section 8.7.3</a>
Data-pointer	MSB	0	0	0	1	0	0	0	0	PX[6:4]			<a href="#">Section 8.7.3</a>
	LSB	0	0	0	1	0	0	1	PX[3:0]				

[1] For further information about the R/ $\bar{W}$ -bit, see [Table 42 on page 56](#).[2] For further information about the register selection bits, see [Table 42 on page 56](#).

## 8.2 General control commands

### 8.2.1 Initialization

#### 8.2.1.1 Command: Initialize

This command generates a chip-wide reset of the device without changing the content of the display RAM. For further information about start-up and shut-down, see [Section 8.8 on page 26](#).

**Table 6. Initialize command bit description**

Bit	Symbol	Value	Description
-	R/ $\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00111010	fixed value

#### 8.2.1.2 $\overline{RST}$ pin

The  $\overline{RST}$  pin generates a chip-wide reset of the device without changing the content of the display RAM. For further information about start-up and shut-down, see [Section 8.8 on page 26](#).

### 8.2.2 Command: OTP-refresh

Each IC is calibrated during production and testing of the device in order to achieve the specified accuracy of the  $V_{LCD}$ , the frame frequency, and the temperature measurement. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. These cells are read by the device after a reset and every time when the Initialize command or the OTP-refresh command is sent. The OTP-refresh command takes approximately 10 ms to finish.

**Table 7. OTP-refresh - OTP-refresh command bit description**

Bit	Symbol	Value	Description
-	R/ $\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	11011000	fixed value

### 8.2.3 Command: Device-address

The Device-address command allows setting the address of the device in a cascaded configuration and corresponds with pins A0 and A1 (see [Section 15.2 on page 80](#)).

**Table 8. Device-address - device address command bit description**

Bit	Symbol	Value	Description
-	R/ $\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	000110	fixed value
1 to 0	A[1:0]		<b>set address</b>
		00	master
		01	slave 1
		10	slave 2
		11	slave 3

### 8.2.4 Command: SYNC1\_pin

With the SYNC1\_pin command, the SYNC1 pin can be configured for using the PCA8530 as a single chip or a master in a cascade. If the PCA8530 is a slave in a cascade, the command has no effect.

**Table 9. SYNC1\_pin - SYNC1 pin configuration command bit description**

*This command has no effect if the PCA8530 is a slave in a cascade.*

Bit	Symbol	Value	Description
-	R/ $\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1011100	fixed value
0	OE		<b>SYNC1 pin configuration</b>
		0	pin SYNC1 is an output; gated to 0 V; to be used when PCA8530 is a single chip
		1	pin SYNC1 is an output; providing the synchronization signal; to be used when PCA8530 is a master in a cascade

### 8.2.5 Command: Clock-out-ctrl

When pin CLK is configured as an output pin, the Clock-out-ctrl command enables or disables the clock output on pin CLK ([Section 8.6.1 on page 22](#)).

**Table 10. Clock-out-ctrl - CLK pin input/output switch command bit description**

Bit	Symbol	Value	Description
-	$\overline{R/W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1101010	fixed value
0	COE		<b>control pin CLK</b>
		0	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

### 8.2.6 Command: Read-select

The Read-select command allows choosing to readout the temperature or the device status.

**Table 11. Read-select - status read select command bit description**

Bit	Symbol	Value	Description
-	$\overline{R/W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0001110	fixed value
0	SO		<b>readout</b>
		0	temperature; the Status-readout command allows to readout the temperature TD[7:0], see <a href="#">Table 12</a>
		1	device status: the Status-readout command allows to readout some information about the status of the device, see <a href="#">Table 12</a>

## 8.2.7 Command: Status-readout

The Status-readout command offers to readout some status bits of the PCA8530. These bits indicate the status of the device at the moment of reading.

**Table 12. Status-readout - status and temperature read command bit description**

For this command, bit R/W has to be set logic 1.

Bit	Symbol	Value	Description
-	R/W	1	fixed value
-	RS[1:0]	00	fixed value
<b>Temperature readout if SO = 0 (see Table 11)</b>			
7 to 0	TD[7:0]	00000000 to 11111111	<b>temperature readout</b> (see Section 8.10.4.1 on page 40)
<b>Device status readout if SO = 1 (see Table 11)</b>			
7	SR7		<b>display status</b> (see Table 22 on page 21)
		0	display is disabled
		1	display is enabled
6	SR6		<b>charge pump switching status</b> (status of bit CPE, see Table 14 on page 15)
		0	charge pump disabled
		1	charge pump enabled
5	SR5		<b>charge pump charge status</b>
		0	charge pump has not reached programmed value
		1	charge pump has reached programmed value
4	SR4		<b>reset status flag</b>
		0	<b>no reset</b> has occurred since the reset status flag was cleared last time
		1	<b>reset</b> has occurred since the reset status flag was cleared last time <sup>[1]</sup>
3 to 0	SR[3:0]		<b>EMC detection</b>
		01 SA1 SA0	pre-defined code for EMC detection when I <sup>2</sup> C interface is used
		0101	pre-defined code for EMC detection when SPI interface is used

[1] The flag is set whenever a reset occurs, induced by  $\overline{\text{RST}}$  pin, Power-On Reset (POR), or Initialize command. After power-on, the flag is set and should be cleared for reset monitoring.

Some bits of the Status-readout command have a certain probability of being changed by an EMC/ESD event. For example, an EMC/ESD event can cause a change of the hard-wired settings of SA1 or SA0. Therefore SR[3:0] can help to detect if an EMC/ESD event has occurred which has caused the change of a bit. In environments where EMC/ESD events may occur, it could be helpful to compare the result of the Status-readout command with the initial bit settings periodically.



### 8.2.8 Command: Clear-reset-flag

The Clear-reset-flag command clears the reset flag SR4, see [Table 12](#).

**Table 13. Clear-reset-flag - Clear-reset-flag command bit description**

Bit	Symbol	Value	Description
-	$\overline{R/W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00011111	fixed value

## 8.3 Charge pump and LCD bias control commands

### 8.3.1 Command: Charge-pump-ctrl

The Charge-pump-ctrl command enables or disables the internal  $V_{LCD}$  generation and controls the charge pump voltage multiplier settings.

**Table 14. Charge-pump-ctrl - charge pump control command bit description**

Bit	Symbol	Value	Description
-	$\overline{R/W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	1100	fixed value
3	CPE		<b>charge pump status</b>
		0	charge pump disabled; no internal $V_{LCD}$ generation; external supply of $V_{LCD}$
		1	charge pump enabled; internal $V_{LCD}$ generation; no external supply of $V_{LCD}$
2 to 0	CPC[2:0]		<b>charge pump voltage multiplier setting</b>
		000	$V_{LCD} = 2 \times V_{DD2}$
		001	$V_{LCD} = 3 \times V_{DD2}$
		010	$V_{LCD} = 4 \times V_{DD2}$
		011	$V_{LCD} = 5 \times V_{DD2}$
		100 to 111	$V_{LCD} = V_{DD2}$ (direct mode)

### 8.3.2 Command: Set- $V_{LCD}$

The Set- $V_{LCD}$  command allows setting the LCD voltage.

**Table 15. Set- $V_{LCD}$  - Set- $V_{LCD}$  command bit description**

Bit	Symbol	Value	Description
<b>Set-<math>V_{LCD}</math>-MSB</b>			
-	$\overline{R/W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 5	-	010	fixed value
4 to 0	V[8:4]		<b>set <math>V_{LCD}</math> MSB</b>
		00000 to 11111	the 5 most significant bits of V[8:0]
<b>Set-<math>V_{LCD}</math>-LSB</b>			
-	$\overline{R/W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	0110	fixed value
3 to 0	V[3:0]		<b>set <math>V_{LCD}</math> LSB</b>
		0000 to 1111	the 4 least significant bits of V[8:0]

A value of 0h corresponds to  $V_{LCD} = 4$  V and values equal or higher than 10Ch correspond to  $V_{LCD} = 12$  V without temperature compensation. Every LSB change corresponds to a  $V_{LCD}$  programming step of 0.03 V. For further information, see

[Section 8.10.3 on page 34](#) and [Equation 2 on page 35](#).

### 8.3.3 Command: Set-bias-mode

**Table 16. Set-bias-mode - set bias mode command bit description**

*This command is not applicable for the static drive mode.*

Bit	Symbol	Value	Description
-	$\overline{R/W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	110100	fixed value
1 to 0	B[1:0]		<b>set bias mode</b>
		00, 01	unused
		11	$\frac{1}{3}$ bias
		10	$\frac{1}{2}$ bias

## 8.4 Temperature compensation control commands

### 8.4.1 Command: Temperature-ctrl

The Temperature-ctrl command enables or disables the temperature measurement block and the temperature compensation of  $V_{LCD}$  (see [Section 8.10.4 on page 40](#)).

**Table 17. Temperature-ctrl - temperature measurement control command bit description**

For this command, the register selection bits have to be set  $RS[1:0] = 10$ .

Bit	Symbol	Value	Description
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00000	fixed value
2	TCE		<b>temperature compensation control</b>
		0	temperature compensation of $V_{LCD}$ disabled
		1	temperature compensation of $V_{LCD}$ enabled
1	TMF		<b>temperature measurement filter</b>
		0	digital temperature filter disabled <sup>[1]</sup>
		1	digital temperature filter enabled
0	TME		<b>temperature measurement control</b>
		0	temperature measurement disabled; no temperature readout possible
		1	temperature measurement enabled; temperature readout possible

[1] The unfiltered digital value of TD[7:0] is immediately available for the readout and  $V_{LCD}$  compensation.

### 8.4.2 Command: TC-set

The TC-set command allows defining six temperature intervals in the operating temperature range from  $-40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ . For each of the temperature intervals, the TC-slope command (see [Section 8.4.3](#)) allows setting the temperature coefficient of  $V_{\text{LCD}}$ .

**Table 18. TC-set -  $V_{\text{LCD}}$  temperature compensation set command bit description**

For this command, the register selection bits have to be set  $RS[1:0] = 10$ .

Bit	Symbol	Value	Description
<b>TC-set-1</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00111	fixed value
2 to 0	T1T[2:0]	000 to 111	see <a href="#">Table 32 on page 42</a>
<b>TC-set-2</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01000	fixed value
2 to 0	T2T[2:0]	000 to 111	see <a href="#">Table 32 on page 42</a>
<b>TC-set-3</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01001	fixed value
2 to 0	T3T[2:0]	000 to 111	see <a href="#">Table 32 on page 42</a>
<b>TC-set-4</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01010	fixed value
2 to 0	T4T[2:0]	000 to 111	see <a href="#">Table 32 on page 42</a>

### 8.4.3 Command: TC-slope

The TC-slope command allows setting the temperature coefficients of  $V_{LCD}$  corresponding to six temperature intervals defined by the TC-set command.

**Table 19. TC-slope -  $V_{LCD}$  temperature compensation slope command bit description**

For this command, the register selection bits have to be set  $RS[1:0] = 10$ .

Bit	Symbol	Value	Description
<b>TC-slope-A</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00001	fixed value
2 to 0	TSA[2:0]	000 to 111	see <a href="#">Table 33 on page 43</a>
<b>TC-slope-B</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00010	fixed value
2 to 0	TSB[2:0]	000 to 111	see <a href="#">Table 33 on page 43</a>
<b>TC-slope-C</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00011	fixed value
2 to 0	TSC[2:0]	000 to 111	see <a href="#">Table 33 on page 43</a>
<b>TC-slope-D</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00100	fixed value
2 to 0	TSD[2:0]	000 to 111	see <a href="#">Table 33 on page 43</a>
<b>TC-slope-E</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00101	fixed value
2 to 0	TSE[2:0]	000 to 111	see <a href="#">Table 33 on page 43</a>
<b>TC-slope-F</b>			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00110	fixed value
2 to 0	TSF[2:0]	000 to 111	see <a href="#">Table 33 on page 43</a>



## 8.5 Display control commands

### 8.5.1 Command: Set-MUX-mode

The Set-MUX-mode command allows setting the multiplex drive mode.

**Table 20. Set-MUX-mode - set multiplex drive mode command bit description**

Bit	Symbol	Value	Description
-	R/W	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	00000	fixed value
2 to 0	M[2:0]		<b>set multiplex drive mode</b>
		000 to 100	unused
		101	1:4 multiplex drive mode
		110	1:2 multiplex drive mode
		111	static

### 8.5.2 Command: Inversion-mode

The Inversion-mode command allows changing the drive scheme inversion mode.

The waveforms used to drive LCD displays (see [Figure 25 on page 46](#) to [Figure 28 on page 49](#)) inherently produce a DC voltage across the display cell. The PCA8530 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of the compensation method is determined with INV[2:0] in [Table 21](#).

**Table 21. Inversion-mode - inversion mode command bit description**

Bit	Symbol	Value	Description
-	R/W	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	10110	fixed value
2 to 0	INV[2:0]		<b>set inversion mode</b>
		000	frame inversion mode
		001	1-line inversion mode
		010	2-line inversion mode
		011	3-line inversion mode
		100 to 111	unused

#### 8.5.2.1 Line inversion mode (driving scheme A)

In line inversion mode, the DC value is compensated every  $n^{\text{th}}$  line. Changing the inversion mode to line inversion mode reduces the possibility for flickering but increases the power consumption (see example waveforms in [Figure 25 on page 46](#) to [Figure 28 on page 49](#))

### 8.5.2.2 Frame inversion mode (driving scheme B)

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is possibility for flicker to occur.

### 8.5.3 Command: Display-ctrl

The Display-ctrl command enables or disables the display.

**Table 22. Display-ctrl - display on and off switch command bit description**

Bit	Symbol	Value	Description
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0011100	fixed value
0	DE		<b>display control</b>
		0	display disabled
		1	display enabled

## 8.6 Clock and frame frequency command

### 8.6.1 Oscillator

The internal logic and LCD drive signals of the PCA8530 are timed by the clock frequency  $f_{clk}$ , which is either internally generated by an on-chip oscillator circuit or externally supplied.

The clock frequency  $f_{clk}$  determines the internal data flow of the device that includes the transfer of display data from the display RAM to the display segment outputs and the generation of the LCD frame frequency.

### 8.6.2 External clock

When an external clock is used, the input pin OSC must be connected to  $V_{DD1}$ . The clock must be supplied to the CLK pin and must have an amplitude equal to the  $V_{DD1}$  voltage supplied to the chip and be referenced to  $V_{SS1}$ .

**Remark:** If an external clock is used, then this clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. Removal of the clock is possible when following the correct procedures as described in [Section 8.8.3 on page 29](#).

### 8.6.3 Internal clock

In applications where the internal clock is used, the input pin OSC must be connected to  $V_{SS1}$ . It is possible to make the clock frequency available on pin CLK by setting bit COE logic 1 (see [Table 10 on page 12](#)). If pin CLK is not used, it should be left open. At power-on the signal at pin CLK is disabled and pin CLK is in 3-state.

### 8.6.4 Command: Frame-frequency

With this command, the clock and frame frequency can be programmed when using the internal clock.

**Table 23. Frame-frequency - frame frequency select command bit description**

Bit	Symbol	Value	Description
-	R/W	0	fixed value
-	RS[1:0]	00	fixed value
7 to 5	-	111	fixed value
4 to 0	FF[4:0]	see <a href="#">Table 24</a>	clock and frame frequency (Hz)

The duty ratio of the clock output may change when choosing different values for the frame frequency (see [Table 24](#)).

The LCD frame frequency is derived from the clock frequency by a fixed division (see [Equation 1](#)).

$$f_{fr} = \frac{f_{clk}}{144} \tag{1}$$

The Frame-frequency command allows configuring the frame frequency in the range of 45 Hz to 300 Hz with steps of

- 5 Hz from 45 Hz to 100 Hz
- 10 Hz from 100 Hz to 300 Hz

The frame frequency of 80 Hz is factory calibrated with a tolerance of  $\pm 3$  Hz at 25 °C.

**Table 24. Clock and frame frequency values**

*Duty cycle definition: % HIGH-level time : % LOW-level time.*

FF[4:0]	Frame frequency (Hz)	Clock frequency (Hz)	Typical duty cycle (%)
00000	45	6472	29 : 71
00001	50	7200	20 : 80
00010	55	7945	12 : 88
00011	60	8662	4 : 96
00100	65	9366	48 : 52
00101	70	10105	44 : 56
00110	75	10766	41 : 59
00111	80	11520	36 : 64
01000	85	12255	32 : 68
01001	90	12944	29 : 71
01010	95	13714	24 : 76
01011	100	14400	20 : 80
01100	110	15781	13 : 87
01101	120	17194	5 : 95
01110	130	18581	49 : 51
01111	140	20211	44 : 56
10000	150	21736	40 : 60
10001	160	23040	36 : 64
10010	170	24511	32 : 68
10011	180	26182	28 : 72
10100	190	27429	24 : 76
10101	200	28800	20 : 80
10110	210	30316	16 : 84
10111	220	32000	12 : 88
11000	230	32914	9 : 91
11001	240	34909	4 : 96
11010	250	36000	50 : 50
11011	260	37161	49 : 51
11100	270	38400	47 : 53
11101	280	39724	45 : 55
11110	290	41143	43 : 57
11111	300	42667	41 : 59

## 8.7 Display RAM commands

### 8.7.1 Command: Write-display-data

The Write-display-data command writes data byte-wise to the RAM. After Power-On Reset (POR), the RAM content is random and should be brought to a defined status by clearing it (setting it logic 0).

**Table 25. Write-display-data - write display data command bit description**

For this command, the register selection bits have to be set  $RS[1:0] = 01$ .

Bit	Symbol	Value	Description
-	R/W	0	fixed value
-	RS[1:0]	01	fixed value
7 to 0	DB[7:0]	00000000 to 11111111	<b>writing data byte-wise to RAM</b>

More information about the display RAM can be found in [Section 8.14 on page 51](#).

### 8.7.2 Bank select commands

For multiplex drive modes 1:2, and static drive mode, it is possible to write data to one area of the RAM while displaying from another. These areas are named as RAM banks. Input and output banks can be set independently from one another with the Input-bank-select and the Output-bank-select command. More information about RAM bank switching can be found in [Section 8.14.3 on page 53](#).

#### 8.7.2.1 Command: Input-bank-select

**Table 26. Input-bank-select - input bank select command bit description**

This command is not applicable for multiplex drive mode 1:4.

Bit	Symbol	Value	Description	
-	R/W	0	fixed value	
-	RS[1:0]	00	fixed value	
7 to 2	-	000010	fixed value	
1 to 0	IB[1:0]	<b>selects RAM bank to write to</b>		
		<b>static drive mode</b>		
		<b>1:2 drive mode</b>		
		00	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1
		01	bank 1: RAM-row 1	
		10	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3
		11	bank 3: RAM-row 3	

### 8.7.2.2 Command: Output-bank-select

**Table 27. Output-bank-select - output bank select command bit description**

*This command is not applicable for multiplex drive mode 1:4.*

Bit	Symbol	Value	Description
-	R/W	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	000100	fixed value
1 to 0	OB[1:0]		<b>selects RAM bank to read from to the LCD</b>
			<b>static drive mode</b>
			<b>1:2 drive mode</b>
		00	bank 0: RAM-row 0
		01	bank 1: RAM-row 1
			bank 0: RAM-rows 0 and 1
		10	bank 2: RAM-row 2
		11	bank 3: RAM-row 3
			bank 2: RAM-rows 2 and 3

### 8.7.3 Command: Data-pointer

The Data-pointer command defines the display RAM address where the following display data are sent to. For setting the data pointer always the three commands Data-pointer-init, Data-pointer-MSB and Data-pointer-LSB have to be sent.

**Table 28. Data-pointer - set data pointer command bit description**

*For further information about the RAM, see [Section 8.14 on page 51](#).*

Bit	Symbol	Value	Description
<b>Data-pointer-init</b>			
-	R/W	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	10100000	fixed value
<b>Data-pointer-MSB: PX[6:4]</b>			
-	R/W	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	10000	fixed value
2 to 0	PX[6:4]	000 to 111	3-bit binary value
<b>Data-pointer-LSB: PX[3:0]</b>			
-	R/W	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	1001	fixed value
3 to 0	PX[3:0]	0000 to 1111	4-bit binary value