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PCA8537

Automotive LCD driver for multiplex rates up to 1:8

Rev. 2 — 7 April 2015　　　　　　　　　　　　　　　　　　**Product data sheet**

1. General description

The PCA8537 is a fully featured Liquid Crystal Display (LCD)[1] driver, specifically designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:8. It generates the drive signals for any static or multiplexed LCD containing up to eight backplanes, 46 segments, and up to 352 elements. The PCA8537 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCA8537 offers a programmable temperature compensation of the LCD supply voltage. The PCA8537 can be easily connected to a microcontroller by either the two-line I²C-bus (PCA8537AH) or a three-line bidirectional SPI-bus (PCA8537BH).

For a selection of NXP LCD segment drivers, see Table 43 on page 72.

2. Features and benefits

- AEC Q100 compliant for automotive applications.
- Low-power single-chip LCD controller and driver
- 352 elements allowing to drive:
  - ◆ up to 44 7-segment alphanumeric characters
  - ◆ up to 22 14-segment alphanumeric characters
- Selectable backplane drive configuration: static, 2, 4, 6, or 8 backplane multiplexing
- Software programmable internal charge pump for on-chip LCD voltage generation up to 9 V with internal capacitors
- 400 kHz I²C-bus interface (PCA8537AH)
- 5 MHz SPI-bus interface (PCA8537BH)
- Programmable temperature compensation of V_{LCD} in four regions
- Selectable display bias configuration
- Wide range for digital power supply: from 1.8 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 9.0 V for high threshold twisted nematic LCDs
- Display memory bank switching in static, duplex, and quadruplex drive modes
- 352-bit RAM for display data storage
- Programmable frame frequency in the range of 60 Hz to 300 Hz in steps of 10 Hz; factory calibrated
- Integrated temperature sensor with temperature readout
- On chip calibration of internal oscillator frequency and V_{LCD}
- Manufactured in silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

3. Applications

- Instrument cluster
- Car radio
- Climate control units

4. Ordering information

Table 1.   Ordering information

Type number	Interface type	Package		
		Name	**Description**	**Version**
PCA8537AH	I^{2}C-bus	TQFP64	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.0 mm	SOT357-1
PCA8537BH	SPI-bus	TQFP64	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.0 mm	SOT357-1

4.1 Ordering options

Table 2.   Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCA8537AH/Q900/1	PCA8537AH/Q900/1,5	935297895518	tape and reel, 13 inch, dry pack	1
PCA8537BH/Q900/1	PCA8537BH/Q900/1,5	935297896518	tape and reel, 13 inch, dry pack	1

5. Marking

Table 3.   Marking codes

Type number	Marking code
PCA8537AH/Q900/1	PCA8537AH
PCA8537BH/Q900/1	PCA8537BH

6. Block diagram
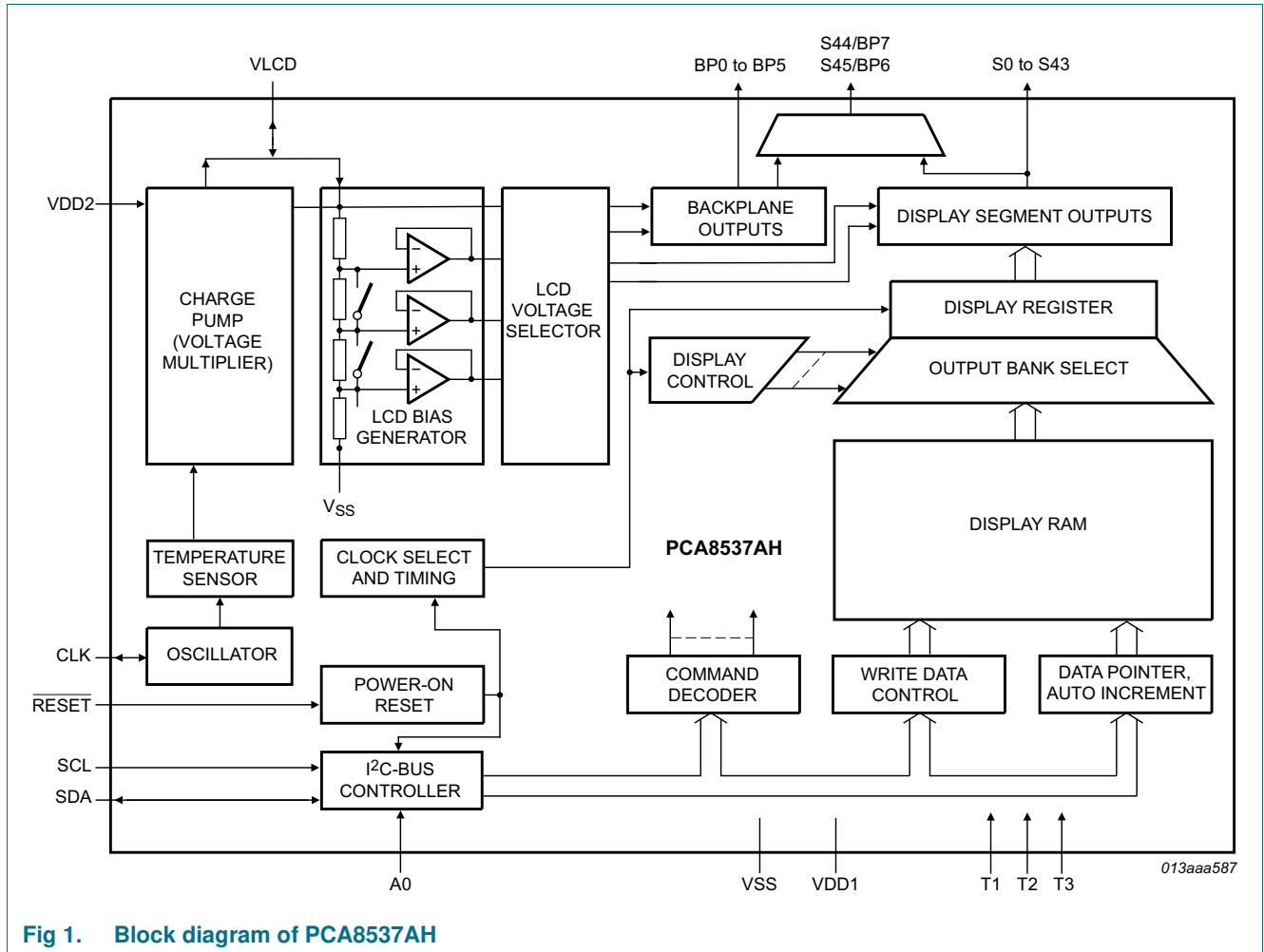
Fig 1.   Block diagram of PCA8537AH

PCA8537

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VLCD

BP0 to BP5

S44/BP7
S45/BP6

S0 to S43

VDD2

CHARGE PUMP (VOLTAGE MULTIPLIER)

LCD BIAS GENERATOR

V$_{SS}$

LCD VOLTAGE SELECTOR

BACKPLANE OUTPUTS

DISPLAY SEGMENT OUTPUTS

DISPLAY REGISTER

DISPLAY CONTROL

OUTPUT BANK SELECT

PCA8537BH

DISPLAY RAM

TEMPERATURE SENSOR

CLOCK SELECT AND TIMING

OSCILLATOR

CLK

$\overline{\text{RESET}}$

POWER-ON RESET

SCL

SDIO

SPI-BUS CONTROLLER

COMMAND DECODER

WRITE DATA CONTROL

DATA POINTER, AUTO INCREMENT

$\overline{\text{CE}}$

VSS

VDD1

T1 T2 T3

013aaa588

Fig 2.   Block diagram of PCA8537BH

7. Pinning information

7.1 Pinning

Top view. For mechanical details, see Figure 62.

Fig 3. Pin configuration for TQFP64 (PCA8537AH)

Top view. For mechanical details, see Figure 62.

Fig 4. Pin configuration for TQFP64 (PCA8537BH)
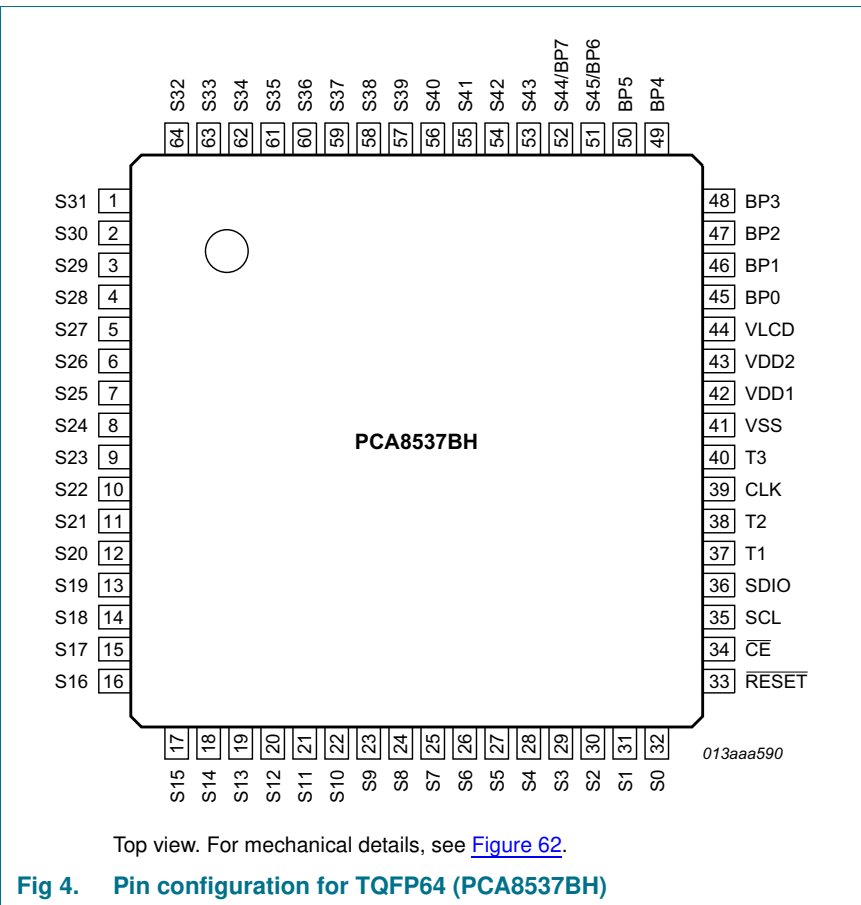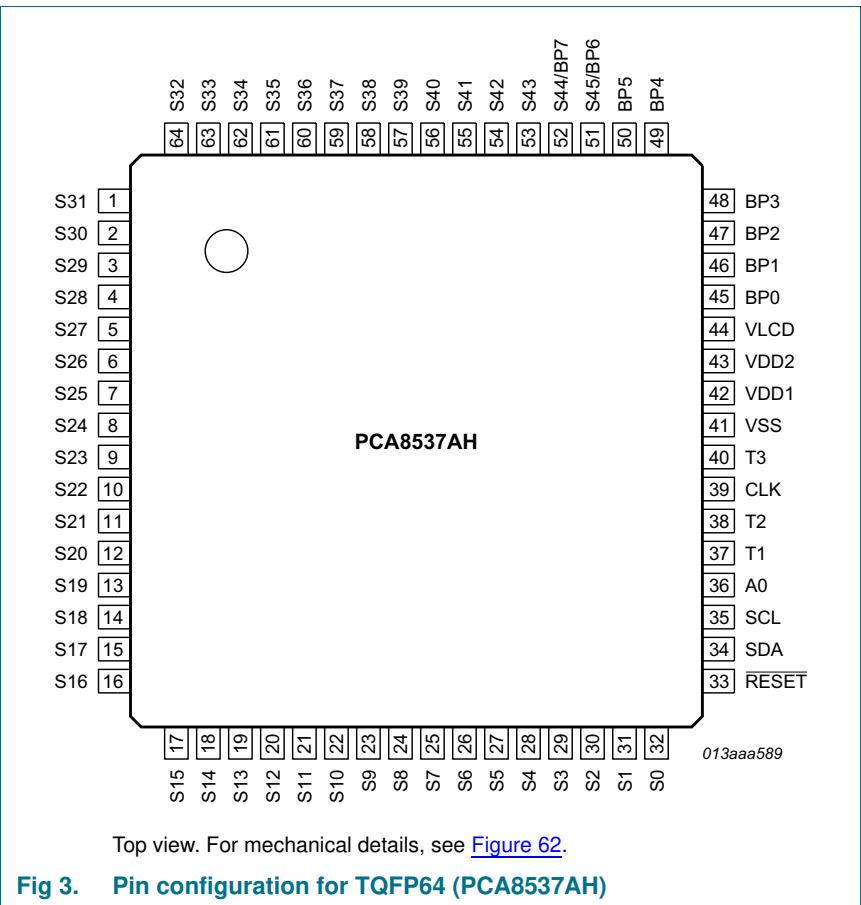
7.2 Pin description

Table 4.   Pin description of PCA8537AH and PCA8537BH
Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Pin	Symbol		Type	Description
	PCA8537AH	**PCA8537BH**		
1 to 32	S31 to S0		output	LCD segments
33	$\overline{\text{RESET}}$		input	active low reset input
34	SDA		input/output	I2C-bus serial data
		$\overline{\text{CE}}$	input	SPI-bus chip enable - active LOW
35	SCL		input	I2C-bus serial clock
		SCL	input	SPI-bus serial clock
36	A0		input	I2C-bus slave address selection
		SDIO	input/output	SPI-bus serial data
37, 38, 40	T1 to T3		input	test pins; must be tied to V_{SS} in applications
39	CLK		input/output	internal oscillator output, external oscillator input
41	VSS		supply	ground supply
42	VDD1		supply	supply voltage 1
43	VDD2		supply	supply voltage 2
44	VLCD[1]		supply	LCD supply[2]
45 to 50	BP0 to BP5		output	LCD backplanes
51	S45/BP6		output	LCD segments for 1:6 multiplex drive mode;
52	S44/BP7		output	LCD backplanes for 1:8 multiplex drive mode
53 to 64	S43 to S32		output	LCD segments

[1] V_{LCD} must be equal to or greater than V_{DD2}.

[2]   When the internal V_{LCD} generation is used, this pin drives the V_{LCD} voltage. In this case pin VLCD is an output. When the external supply is requested, then pin VLCD is an input and V_{LCD} can be supplied on it. In this case, the internal charge pump must be disabled (see Table 9).

8. Functional description

The PCA8537 is a versatile peripheral device designed to interface any microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 352 elements.

8.1 Commands of PCA8537

The commands to control the PCA8537 are defined in Table 5. Any other combinations of operation code bits that are not mentioned in this document can lead to undesired operation modes of PCA8537.

Table 5.　　Commands of PCA8537
The bit labeled with - is not implemented.

Command name	RS[1]	Bits								Reference
		7	6	5	4	3	2	1	0	
Initialize	0	0	0	1	1	1	0	1	0	Section 8.1.1
OTP-refresh	0	1	1	0	1	0	0	0	0	Section 8.1.2
Oscillator-ctrl	0	1	1	0	0	1	1	COE	OSC	Section 8.1.3
Charge-pump-ctrl	0	1	1	0	0	0	0	CPE	CPC	Section 8.1.4
Temp-msr-ctrl	0	1	1	0	0	1	0	TCE	TME	Section 8.1.5
Temp-comp	0	0	0	0	1	1	SLA[2:0]			Section 8.1.6
	0	0	0	1	0	0	SLB[2:0]			
	0	0	0	1	0	1	SLC[2:0]			
	0	0	0	1	1	0	SLD[2:0]			
Set-VPR	0	0	1	0	0	VPR[7:4]				Section 8.1.7
	0	0	1	0	1	VPR[3:0]				
Display-enable	0	0	0	1	1	1	0	0	E	Section 8.1.8
Set-MUX-mode	0	0	0	0	0	0	M[2:0]			Section 8.1.9
Set-bias-mode	0	1	1	0	0	0	1	B[1:0]		Section 8.1.10
Load-data-pointer	0	1	0	P[5:0]						Section 8.1.11
Frame-frequency	0	0	1	1	F[4:0]					Section 8.1.12
Bank-select	0	0	0	0	0	1	0	IBS	OBS	Section 8.1.13
Write-RAM-data	1	B[7:0]								Section 8.1.14
Temp-read	-	TD[7:0]								Section 8.1.15
Invmode_ctrl	0	1	1	0	1	0	1	LF	0	Section 8.1.16
Temp-filter	0	1	1	0	1	0	0	1	TFE	Section 8.1.17

[1]　For further information about the register selection bit, see Table 31 on page 50.

8.1.1 Command: Initialize

This command generates a chip-wide reset which resets all command values to their default values. After this command is sent, it is possible to send additional commands without the need to re-initialize the interface. The reset takes 100 ns to complete.

Table 6.   Initialize - initialize command bit description
For further information, see Section 8.2 on page 16.

Bit	Symbol	Binary value	Description
7 to 0	-	00111010	fixed value

8.1.2 Command: OTP-refresh

During production and testing of the device, each IC is calibrated to achieve the specified accuracy of V_{LCD}, the frame frequency, and the temperature measurement. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells.

The device reads these cells every time at power-on, after a reset, and every time when the initialize command or the OTP-refresh command is sent.

Remark: It is recommended not to enter power-down mode during the OTP refresh cycle.

Table 7.   OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Binary value	Description
7 to 0	-	1101 0000	fixed value

8.1.3 Command: Oscillator-ctrl

The Oscillator-ctrl command switches between internal and external oscillator and enables or disables the pin CLK.

Table 8.   Oscillator-ctrl - oscillator control command bit description
For further information, see Section 8.1.3.1.

Bit	Symbol	Binary value	Description
7 to 2	-	110011	fixed value
1	COE		**control pin CLK**
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state and may be left floating
		1	clock signal available on pin CLK
0	OSC		**oscillator source**
		0[1]	internal oscillator used
		1	external oscillator used; pin CLK becomes an input

[1]   Default value.

8.1.3.1 Oscillator

The internal logic and LCD drive signals of the PCA8537 are timed either by the built-in oscillator or from an external clock.

8.1.3.2 Internal oscillator

When the internal oscillator is used, it is possible to make the clock signal available on pin CLK by using the Oscillator-ctrl command (see Table 8). If this is not intended, the pin CLK should be left open. At power-on the signal at pin CLK is disabled and pin CLK is in 3-state.

If the internal charge pump is enabled, then the internal oscillator starts and is used to run the charge pump. An external oscillator can still be applied for driving the display waveforms.

The duty cycle of the output clock provided on the CLK pin is not always 50 : 50. Table 18 on page 13 shows the expected duty cycle for each of the chosen frame frequencies.

8.1.3.3 External clock

In applications where an external clock must be applied to the PCA8537, bit OSC (see Table 8) must be set logic 1. In this case, pin CLK becomes an input.

The CLK signal is a signal that is fed into the V_{DD1} domain. Therefore it must have an amplitude equal to the V_{DD1} voltage supplied to the chip and be referenced to V_{SS}.

The clock frequency (f_{clk}) determines the LCD frame frequency.

Remark: If an external clock is used then this clock signal must always be supplied to the device. Removing the clock can freeze the LCD in a DC state. Removal of the clock is possible when following the correct procedures (see Figure 11 on page 21 and Figure 12 on page 22).

8.1.4 Command: Charge-pump-ctrl

The Charge-pump-ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier setting.

Table 9.   Charge-pump-ctrl - charge pump control command bit description
For further information, see Table 12 on page 11 and Section 8.4.3 on page 26.

Bit	Symbol	Binary value	Description
7 to 2	-	110000	fixed value
1	CPE		**charge pump switch**
		0[1]	charge pump disabled; no internal V_{LCD} generation; external supply of V_{LCD}
		1	charge pump enabled
0	CPC		**charge pump voltage multiplier setting**
		0[1]	$V_{LCD} = 2 \times V_{DD2}$
		1	$V_{LCD} = 3 \times V_{DD2}$

[1]   Default value.

8.1.5 Command: Temp-msr-ctrl

The Temp-msr-ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD}.

Table 10. Temp-msr-ctrl - temperature measurement control command bit description
For further information, see Section 8.4.4 on page 28.

Bit	Symbol	Binary value	Description
7 to 2	-	110010	fixed value
1	TCE		**temperature compensation switch**
		0	no temperature compensation of V_{LCD} possible
		1[1]	temperature compensation of V_{LCD} possible
0	TME		**temperature measurement switch**
		0	temperature measurement disabled: no temperature readout possible
		1[1]	temperature measurement enabled: temperature readout possible

[1] Default value.

8.1.6 Command: Temp-comp

The Temp-comp command allows setting the temperature compensation coefficients for each of the temperature regions SFA to SFD. For further information, see Section 8.4.4.2.

Table 11. Temp-comp - temperature compensation coefficients command
For further information, see Section 8.4.4 on page 28.

Bit	Symbol	Binary value	Description
SLA			
7 to 3	-	00011	fixed value
2 to 0	SLA[2:0]	000[1] to 111	**temperature compensation coefficient SLA**, see Table 27 on page 30
SLB			
7 to 3	-	00100	fixed value
2 to 0	SLB[2:0]	000[1] to 111	**temperature compensation coefficient SLB**, see Table 27 on page 30
SLC			
7 to 3	-	00101	fixed value
2 to 0	SLC[2:0]	000[1] to 111	**temperature compensation coefficient SLC**, see Table 27 on page 30
SLD			
7 to 3	-	00110	fixed value
2 to 0	SLD[2:0]	000[1] to 111	**temperature compensation coefficient SLD**, see Table 27 on page 30

[1] Default value.

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8.1.7 Command: Set-VPR

With these two instructions, it is possible to set the target V_{LCD} voltage for the internal charge pump.

Table 12.   Set-VPR - set VPR command bit description
For further information, see Section 8.4.2 on page 24.

Bit	Symbol	Binary value	Description
Set-VPR MSB			
7 to 4	-	0100	fixed value
3 to 0	VPR[7:4]	0000[1] to 1111[2]	**the four most significant bits of VPR[7:0]**
Set-VPR LSB			
7 to 4	-	0101	fixed value
3 to 0	VPR[3:0]	0000[1] to 1111[2]	**the four least significant bits of VPR[7:0]**

[1]   Default value.

[2]   VPR[7:0] = 0h results in $V_{prog(LCD)}$ = 3 V;
        VPR[7:0] = C8h results in $V_{prog(LCD)}$ = 9 V.

8.1.8 Command: Display-enable

This command allows switching the display on and off. The possibility to disable and enable the display allows implementation of blinking the entire display under external control.

Table 13.   Display-enable - display enable command bit description

Bit	Symbol	Binary value	Description
7 to 1	-	0011100	fixed value
0	E	0[1]	**display disabled** backplane and segment outputs are internally connected to V_{SS}
		1	**display enabled**

[1]   Default value.

8.1.9 Command: Set-MUX-mode

The multiplex drive mode is configured with the bits described in Table 14.

Table 14.   Set-MUX-mode - set multiplex drive mode command bit description
For further information, see Section 8.4.5 on page 31.

Bit	Symbol	Binary value	Description
7 to 3	-	00000	fixed value
2 to 0	M[2:0]	000[1] 011 101 111	**1:8 multiplex drive mode** 8 backplanes and 44 segments
		110	**1:6 multiplex drive mode** 6 backplanes and 46 segments
		100	**1:4 multiplex drive mode** 4 backplanes and 44 segments
		010	**1:2 multiplex drive mode** 2 backplanes and 44 segments
		001	**static drive mode** 1 backplane and 44 segments

[1]   Default value.

8.1.10 Command: Set-bias-mode

The Set-bias-mode command allows setting the bias level.

Table 15.   Set-bias-mode - set bias mode command bit description
For further information, see Section 8.4.5 on page 31.

Bit	Symbol	Binary value	Description
7 to 2	-	110001	fixed value
1 to 0	B[1:0]		LCD bias configuration[1]
		00[2] 01	$\frac{1}{4}$ bias
		11	$\frac{1}{3}$ bias
		10	$\frac{1}{2}$ bias

[1]   Not applicable for static drive mode.

[2]   Default value.

8.1.11 Command: Load-data-pointer

The Load-data-pointer command defines the display RAM address where the following display data will be sent to.

Table 16.   Load-data-pointer - load data pointer command bit description
For further information, see Section 8.8 on page 43.

Bit	Symbol	Binary value	Description
7 to 6	-	10	fixed value
5 to 0	P[5:0]	000000 to 101101	**RAM address** 6-bit binary value of 0 to 45

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8.1.12 Command: Frame-frequency

With the Frame-frequency command, the frame frequency and the output clock frequency can be configured.

Table 17.   Frame frequency - frame frequency and output clock frequency command bit description

Bit	Symbol	Binary value	Description
7 to 5	-	011	fixed value
4 to 0	F[4:0]	see Table 18	**frame frequency values**, see Table 18

Table 18.   Frame frequency values

F[4:0]	Nominal frame frequency f_{fr} (Hz)[1]	Resultant output clock frequency, $f_{clk(o)}$ (Hz)	Duty cycle (%)[2]
00000	60	2880	20 : 80
00001	70	3360	7 : 93
00010	80	3840	47 : 53
00011	91	4368	40 : 60
00100	100	4800	33 : 67
00101	109	5232	27 : 73
00110	120	5760	20 : 80
00111	129.7	6226	13 : 87
01000	141.2	6778	5 : 95
01001	150	7200	50 : 50
01010	160	7680	47 : 53
01011	171.4	8227	43 : 57
01100	177.8	8534	41 : 59
01101	192	9216	36 : 64
01110[3]	200	9600	33 : 67
01111	208.7	10018	30 : 70
10000	218.2	10474	27 : 73
10001	228.6	10973	23 : 77
10010	240	11520	20 : 80
10011	252.6	12125	16 : 84
10100, 10101	266.7	12802	10 : 90
10110, 10111	282.4	13555	5 : 95
11000 to 11111	300	14400	50 : 50

[1]   Nominal frame frequency calculated for the default clock frequency of 9600 Hz.

[2]   Duty cycle definition: % HIGH-level time : % LOW-level time.

[3]   Default value.

8.1.12.1 Timing and frame frequency

The timing of the PCA8537 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency. The frame frequency is a fixed division of the internal clock or of the frequency applied to pin CLK when an external clock is used.

When the internal clock is used, the clock frequency can be programmed by software such that the nominal frame frequency can be chosen in steps of 10 Hz in the range of 60 Hz to 300 Hz (see Table 18). Furthermore the nominal frame frequency is factory-calibrated with an accuracy of ±15 %.

When the internal clock is enabled at pin CLK by using bit COE, the duty ratio of the clock may change when choosing different values for the frame frequency prescaler. Table 18 shows the different output duty ratios for each frame frequency prescaler setting.

8.1.13 Command: Bank-select

For the multiplex drive modes 1:4, 1:2, and the static drive mode, it is possible to write data to one area of the RAM while displaying from another. These areas are named RAM banks. There are two banks, 0 and 1. Figure 39 on page 49 and Figure 40 on page 49 show the concept. The Bank-select command controls where data is written to and where it is displayed from.

Table 19.   Bank-select - bank select command bit description
For further information, see Section 8.9 on page 49.

Bit	Symbol	Binary value	Description
7 to 2	-	000010	fixed value
1	IBS		**selects RAM bank to write to**
		0[1]	Bank 0
		1	Bank 1
0	OBS		**selects RAM bank to read from to the LCD**
		0[1]	Bank 0
		1	Bank 1

[1]   Default value.

8.1.14 Command: Write-RAM-data

By setting the RS bit of the control byte to logic 1, all data transferred is interpreted as RAM data and placed in the RAM in accordance with the current setting of the RAM address pointer (see Section 8.1.11 on page 12). Definition of the RS can be found in Table 31 on page 50.

Remark: After Power-On Reset (POR) the RAM content is random and should be brought to a defined status by clearing it (setting it to logic 0).

Table 20.   Write-RAM-data - write RAM data command bit description
For further information, see Section 8.8 on page 43.

Bit	Symbol	Binary value	Description
7 to 0	B[7:0]	00000000 to 11111111	**writing data byte-wise to the RAM**

8.1.15 Command: Temp-read

The Temp-read command allows reading out the temperature values measured by the internal temperature sensor.

Table 21. Temp-read - temperature readout command bit description
For further information, see Section 8.4.4 on page 28.

Bit	Symbol	Binary value	Description
7 to 0	TD[7:0]	00000000 to 11111111	**digital temperature values**[1]

[1] For this command, bit R/$\overline{\text{W}}$ of the I²C-bus slave address byte has to be set logic 1 (see Table 32).

8.1.16 Command: Invmode_ctrl

The Invmode_ctrl command allows changing the drive scheme inversion mode.

The waveforms used to drive LCD displays inherently produce a DC voltage across the display cell. The PCA8537 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of compensation method is determined with the LF bit.

Table 22. Invmode_ctrl - drive scheme inversion command bit description
For further information, see Section 8.4.6 on page 34.

Bit	Symbol	Binary value	Description
7 to 2	-	110101	fixed value
1	LF		**set inversion mode**
		0[1]	driving scheme A: line inversion mode
		1	driving scheme B: frame inversion mode
0	-	0	fixed value

[1] Default value.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is possibility for flicker to occur.

Figure 24 on page 34 to Figure 30 on page 40 are showing the waveforms in line inversion mode. Figure 31 on page 41 shows an example of frame inversion.

8.1.17 Command: Temp-filter

Table 23. Temp-filter - digital temperature filter command bit description
For further information, see Section 8.4.4 on page 28.

Bit	Symbol	Binary value	Description
7 to 1	-	1101 001	fixed value
0	TFE		**digital temperature filter switch**
		0[1]	digital temperature filter disabled; the unfiltered digital value of TD[7:0] is immediately available for the readout and V_{LCD} compensation, see Section 8.4.4.1
		1	digital temperature filter enabled

[1] Default value.

8.2 Start-up and shut-down

8.2.1 Power-On Reset (POR)

At power-on, the PCA8537 resets to starting conditions as follows:

1. All backplane and segment outputs are set to V_{SS}.
2. Selected drive mode is: 1:8 with $\frac{1}{4}$ bias.
3. Input and output bank selectors are reset.
4. The I^{2}C-bus and SPI-bus interface are initialized.
5. The data pointer is cleared (set logic 0).
6. The internal oscillator is running; no clock signal is available on pin CLK; pin CLK is in 3-state.
7. Temperature measurement is enabled.
8. Temperature filter is disabled.
9. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
10. The V_{LCD} temperature compensation is enabled.
11. The display is disabled.

The reset state is as shown in Table 24.

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Table 24.   Reset state

Reset state of configuration bits shown in the command table format for clarity. The bit labeled with - has an undefined reset state.

Command name	Bits							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Oscillator-ctrl	1	1	0	0	1	1	COE = 0	OSC = 0
Charge-pump-ctrl	1	1	0	0	0	0	CPE = 0	CPC = 0
Temp-msr-ctrl	1	1	0	0	1	0	TCE = 1	TME = 1
Temp-comp	0	0	0	1	1	SLA[2:0] = 000		
	0	0	1	0	0	SLB[2:0] = 000		
	0	0	1	0	1	SLC[2:0] = 000		
	0	0	1	1	0	SLD[2:0] = 000		
Set-VPR	0	1	0	0	VPR[7:4] = 0000			
	0	1	0	1	VPR[3:0] = 0000			
Display-enable	0	0	1	1	1	0	0	E = 0
Set-MUX-mode	0	0	0	0	0	M[2:0] = 000		
Set-bias-mode	1	1	0	0	0	1	B[1:0] = 00	
Load-data-pointer	1	0	P[5:0] is undefined					
Frame-frequency	0	1	1	F[4:0] = 01110				
Bank-select	0	0	0	0	1	0	IBS = 0	OBS = 0
Invmode_ctrl	1	1	0	1	0	1	LF = 0	-
Temp-filter	1	1	0	1	0	0	1	TFE = 0

Remark: Do not transfer data on the I²C-bus or SPI-bus for at least 1 ms after a power-on reset to allow the reset action to complete.

The first command sent to the device after the power-on event must be the Initialize command (see Section 8.1.1).

After POR and before enabling the display, the RAM content should be brought to a defined status

- by clearing it (setting it all to logic 0) or
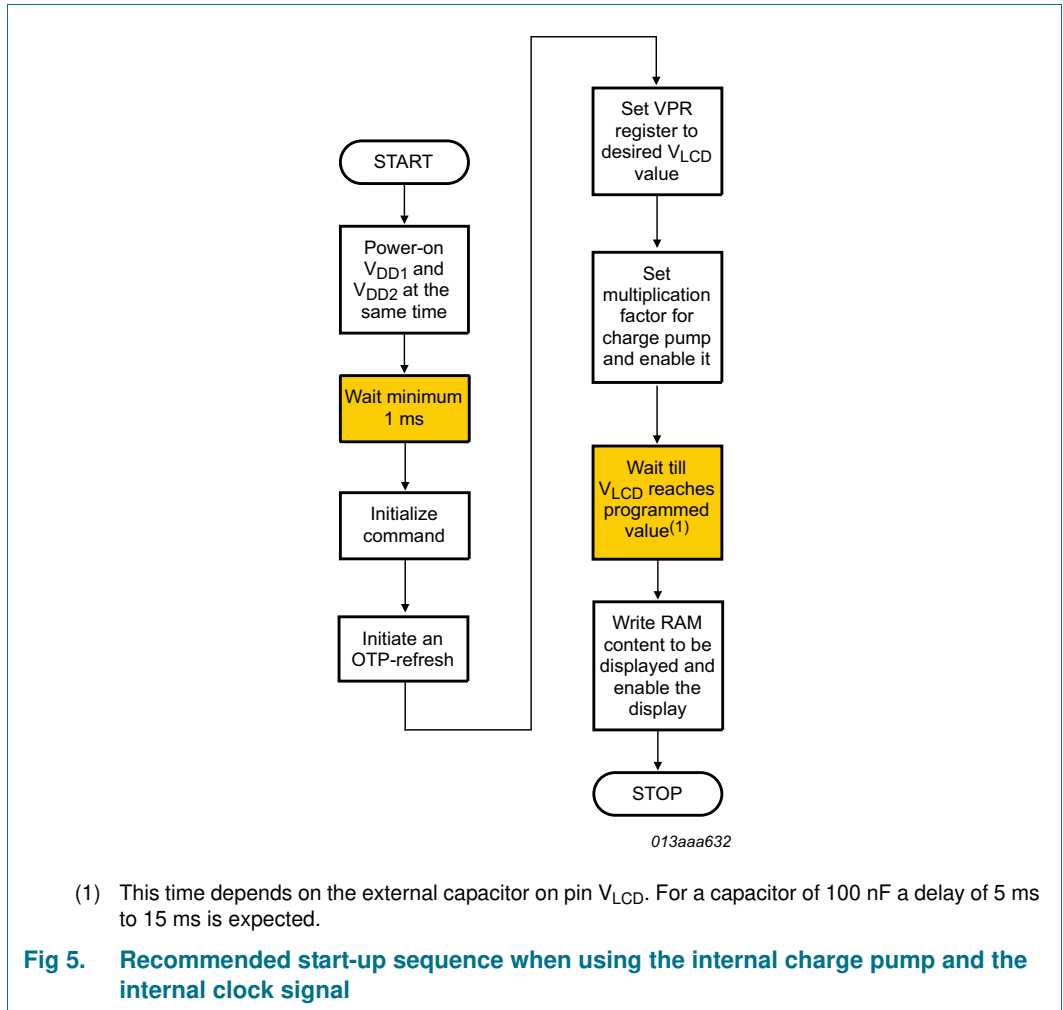- by writing meaningful content (for example, a graphic)

otherwise unwanted display artifacts may appear on the display.

8.2.2 $\overline{\text{RESET}}$ pin function

The $\overline{\text{RESET}}$ pin of the PCA8537 resets all the registers to their default state. The reset state is given in Table 24. The RAM contents remain unchanged. After the reset signal is removed, the PCA8537 will behave in the same manner as after POR. See Section 8.2.1 for details.

8.2.3   Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.

(1) This time depends on the external capacitor on pin V_{LCD}. For a capacitor of 100 nF a delay of 5 ms to 15 ms is expected.

Fig 5. Recommended start-up sequence when using the internal charge pump and the internal clock signal

If the display is enabled too soon after the charge pump is enabled, then the V_{LCD} voltage may not have yet stabilized leading to an uneven display effect.
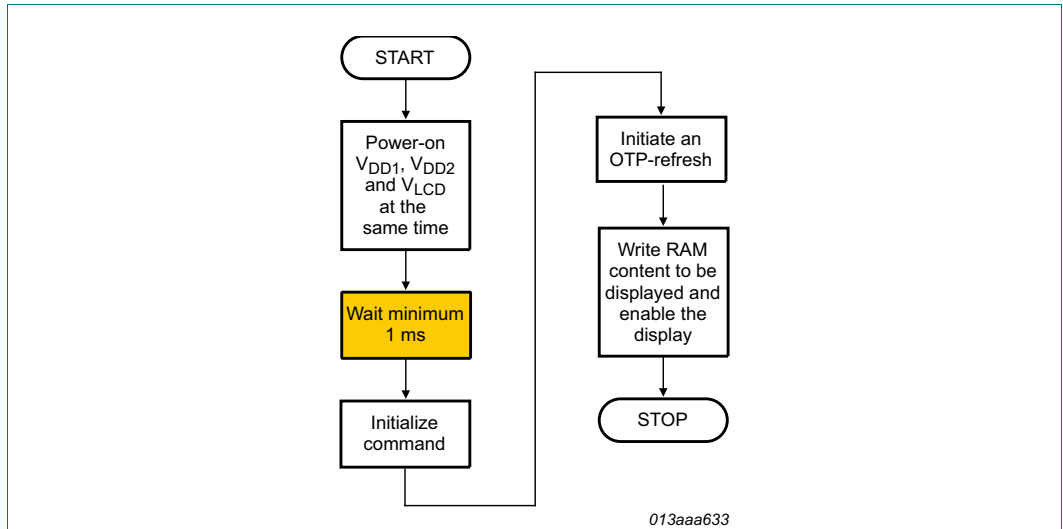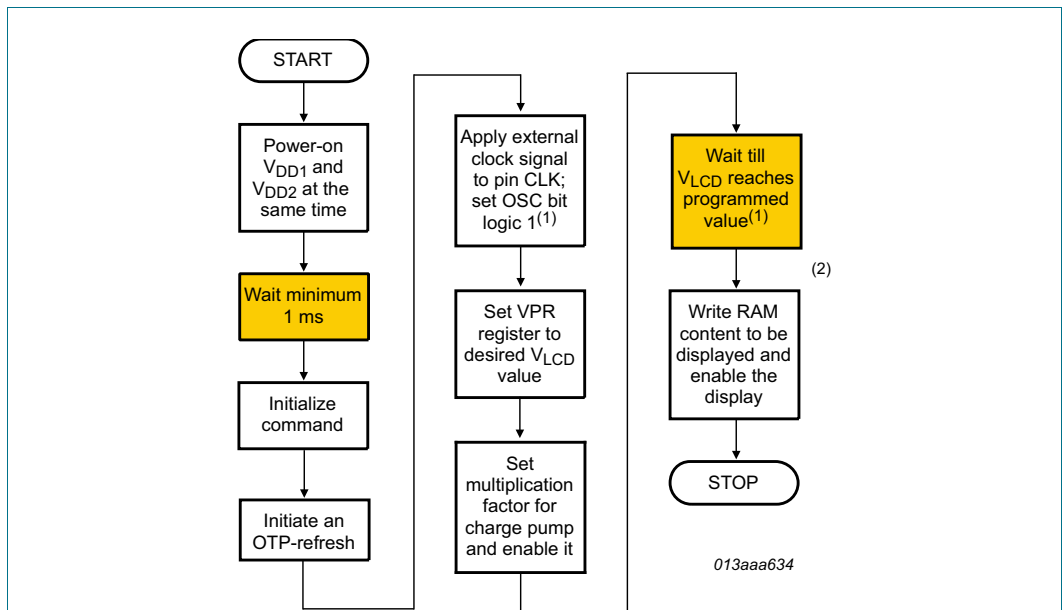
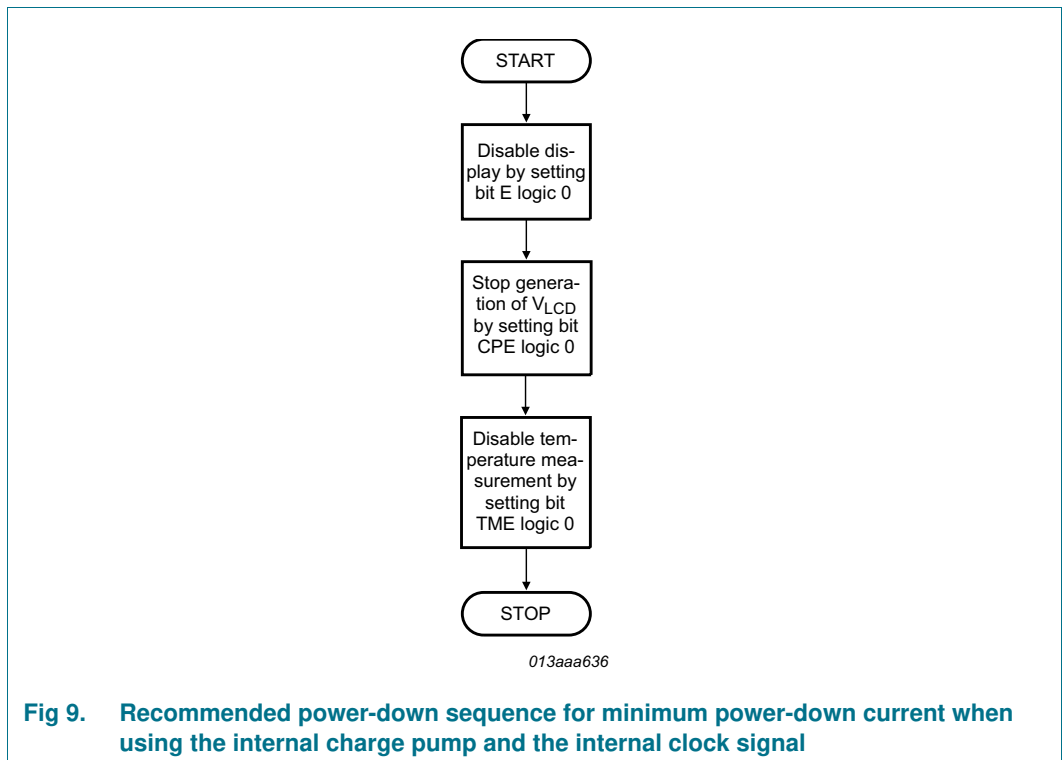**Fig 6.** Recommended start-up sequence when using an external supplied V_{LCD} and the internal clock signal

(1) The external clock signal can be applied after the generation of the V_{LCD} voltage as well.

(2) This time depends on the external capacitor on pin V_{LCD}. For a capacitor of 100 nF a delay of 5 ms to 15 ms is expected.
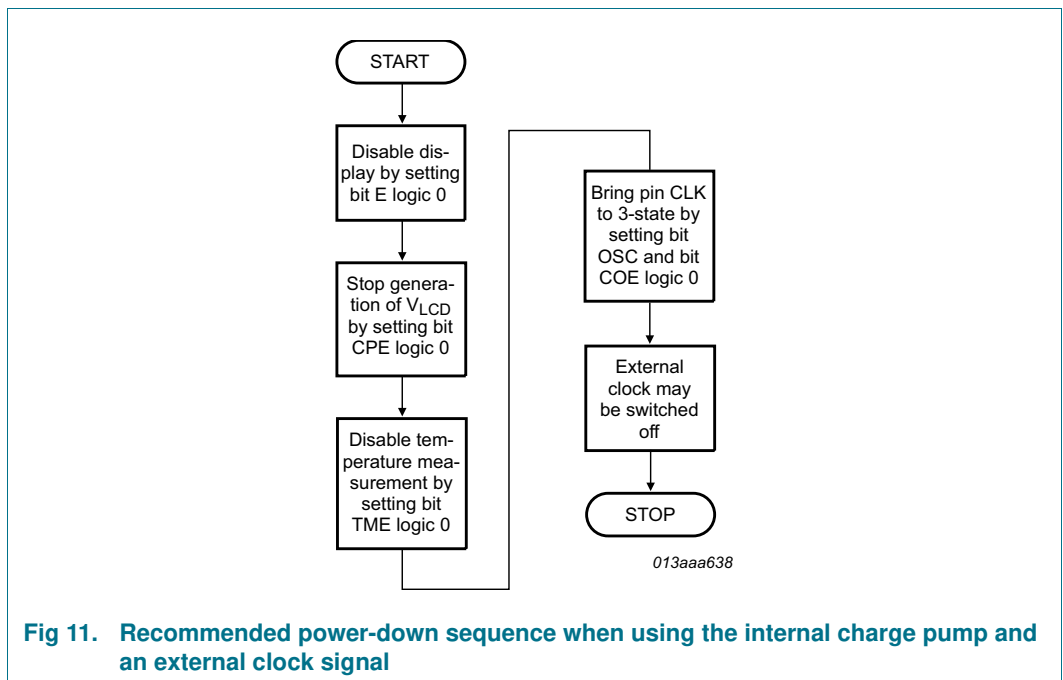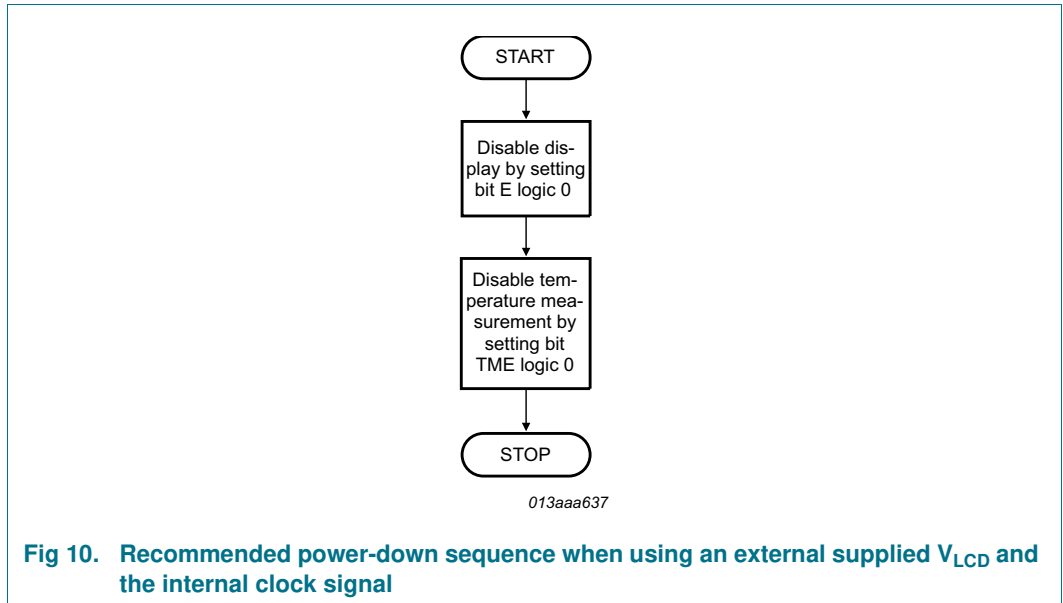
Fig 7. Recommended start-up sequence when using the internal charge pump and an external clock signal

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Fig 8. **Recommended start-up sequence when using an external supplied V_{LCD} and an external clock signal**
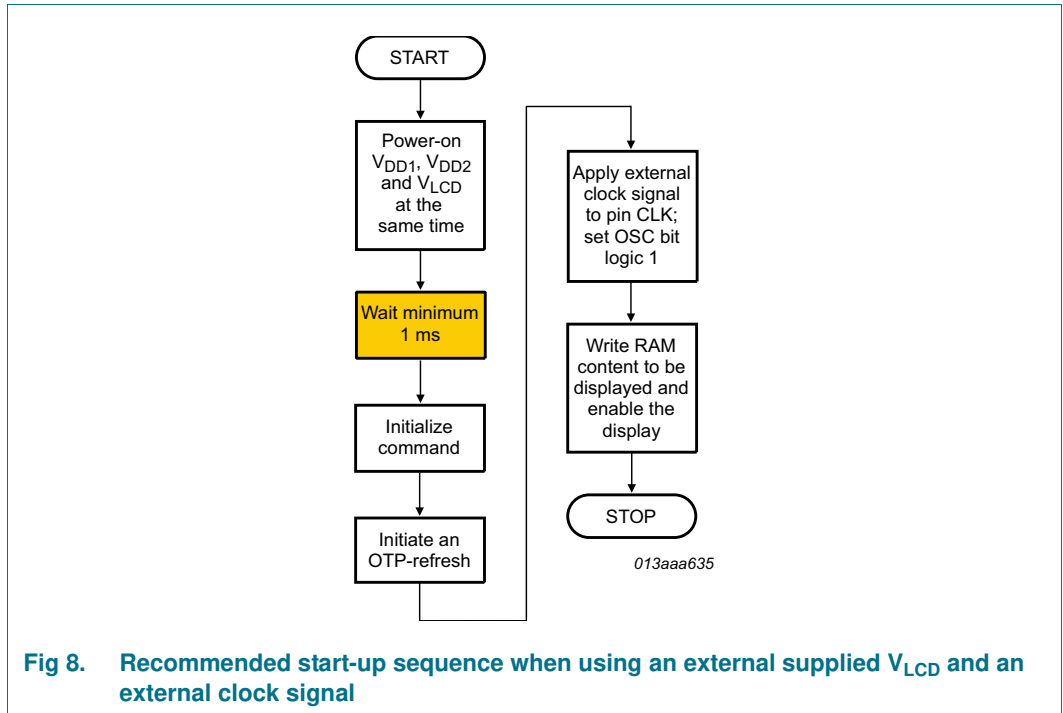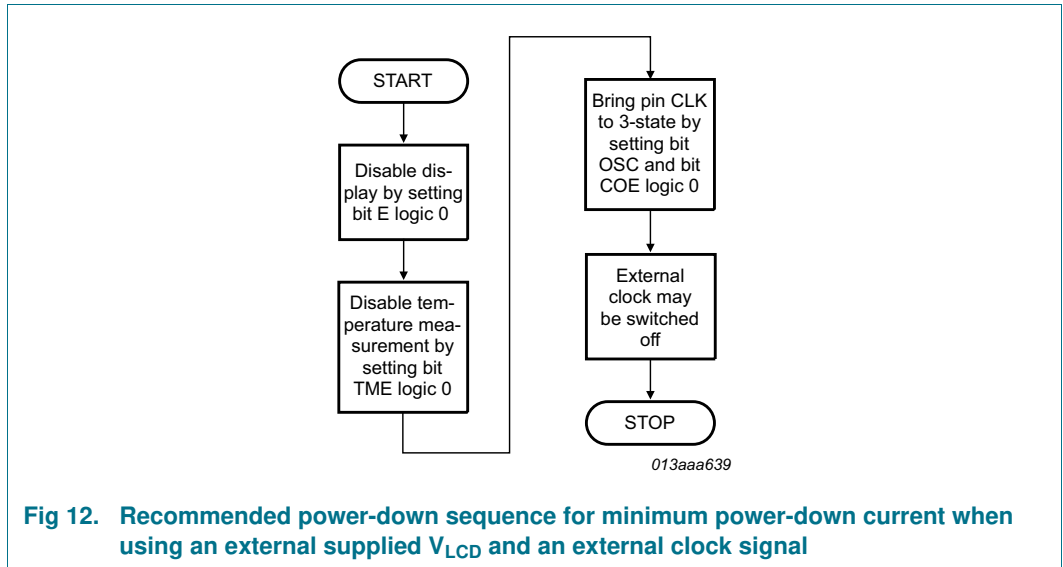
8.2.4 Recommended sequences to enter power-down mode

With the following sequences, the PCA8537 can be set to a state of minimum power consumption, called power-down mode.

Fig 9. **Recommended power-down sequence for minimum power-down current when using the internal charge pump and the internal clock signal**

013aaa637

Fig 10.　Recommended power-down sequence when using an external supplied V_{LCD} and the internal clock signal

013aaa638

Fig 11.　Recommended power-down sequence when using the internal charge pump and an external clock signal

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013aaa639

Fig 12. **Recommended power-down sequence for minimum power-down current when using an external supplied V$_{LCD}$ and an external clock signal**

Remark: It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (see Section 10). Otherwise this may cause unwanted display artifacts. In the case of uncontrolled removal of supply voltages the PCA8537 will not be damaged.

Remark: Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V$_{LCD}$) is on while the IC supply voltage (V$_{DD1}$ or V$_{DD2}$) is off, or the other way around. This may cause unwanted display artifacts. To avoid such artifacts, V$_{LCD}$, V$_{DD1}$, and V$_{DD2}$ must be applied or removed together.

Remark: A clock signal must always be supplied to the device when the display is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. It is recommended to first disable the display and afterwards to remove the clock signal.

8.3 Possible display configurations

The PCA8537 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 13). It can directly drive any static or multiplexed LCD containing up to eight backplanes with 44 segments.

The display configurations possible with the PCA8537 depend on the number of active backplane outputs required. A selection of possible display configurations is given in Table 25.
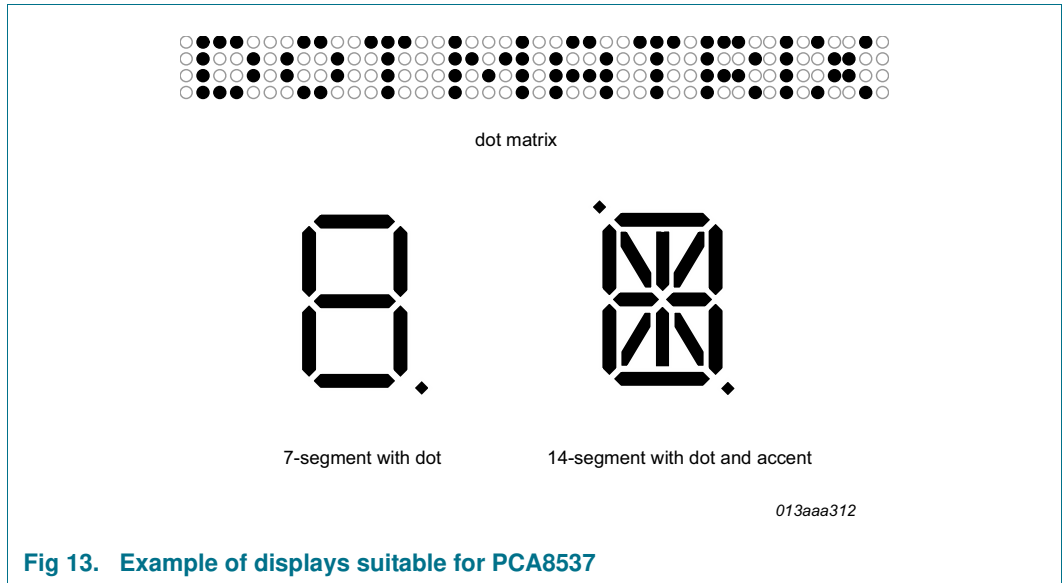
dot matrix

7-segment with dot   14-segment with dot and accent

013aaa312

Fig 13.   Example of displays suitable for PCA8537

Table 25.   Selection of display configurations

Number of			Digits/Characters		Dot matrix/ Elements
Backplanes	**Segments**	**Icons**	**7 segment**[1]	**14 segment**[2]	
8	44	352	44	22	352 dots (8 × 44)
6	46	276	34	17	276 dots (6 × 46)
4	44	176	22	11	176 dots (4 × 44)
2	44	88	11	5	88 dots (2 × 44)
1	44	44	5	2	44 dots (1 × 44)

[1]   7 segment display has 8 elements including the decimal point.

[2]   14 segment display has 16 elements including decimal point and accent dot.

All of the display configurations in Table 25 can be implemented in the typical systems shown in Figure 14 (internal V_{LCD}) and in Figure 15 (external V_{LCD}).
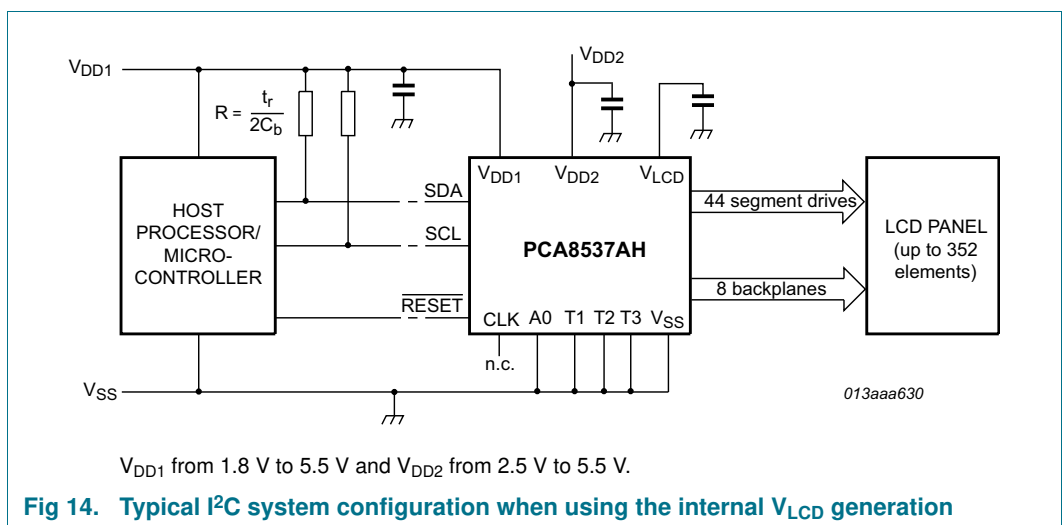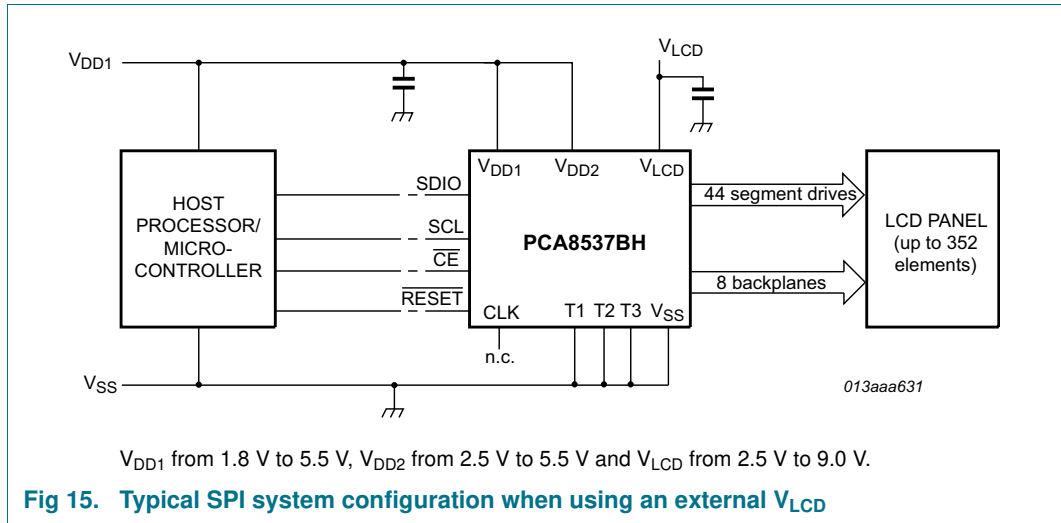

V_{DD1} from 1.8 V to 5.5 V and V_{DD2} from 2.5 V to 5.5 V.

Fig 14.   Typical I²C system configuration when using the internal V_{LCD} generation

V_{DD1} from 1.8 V to 5.5 V, V_{DD2} from 2.5 V to 5.5 V and V_{LCD} from 2.5 V to 9.0 V.

Fig 15. **Typical SPI system configuration when using an external V_{LCD}**

The host microcontroller maintains the two-line I^{2}C-bus communication channel with the PCA8537AH or the three-line SPI-bus with the PCA8537BH. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD1}, V_{DD2}, V_{SS}, V_{LCD}), the external capacitors, and the LCD panel selected for the application.

The recommended values for external capacitors on V_{DD1}, V_{DD2}, and V_{LCD} are of nominal 100 nF value. When using bigger capacitors, especially on the V_{LCD}, the generated ripple will be consequently smaller. However it will take longer for the internal charge pump to first reach the target V_{LCD} voltage.

If V_{DD1} and V_{DD2} are connected externally, the capacitors on V_{DD1} and V_{DD2} can be replaced by a single capacitor with a nominal value of 220 nF.

Remark: In case of insufficient decoupling, ripple on V_{DD1} and V_{DD2} will create additional V_{LCD} ripple. The ripple on the V_{LCD} can be reduced by making the V_{SS} connection as low-ohmic as possible. Excessive ripple on V_{LCD} may cause flicker on the display.

8.4 LCD supply voltage

8.4.1 External V_{LCD} supply

V_{LCD} can be directly supplied to the VLCD pin. In this case, the internal charge pump must not be enabled otherwise a high current may occur on pin VDD2 and pin VLCD. When V_{LCD} is supplied externally, no internal temperature compensation occurs on this voltage even if bit TCE is set logic 1 (see Section 8.4.4.2). The V_{LCD} voltage which is supplied externally will be available at the segments and backplanes of the device through the chosen bias system. Also programming VPR[7:0] will have no effect on the V_{LCD} which is externally supplied.
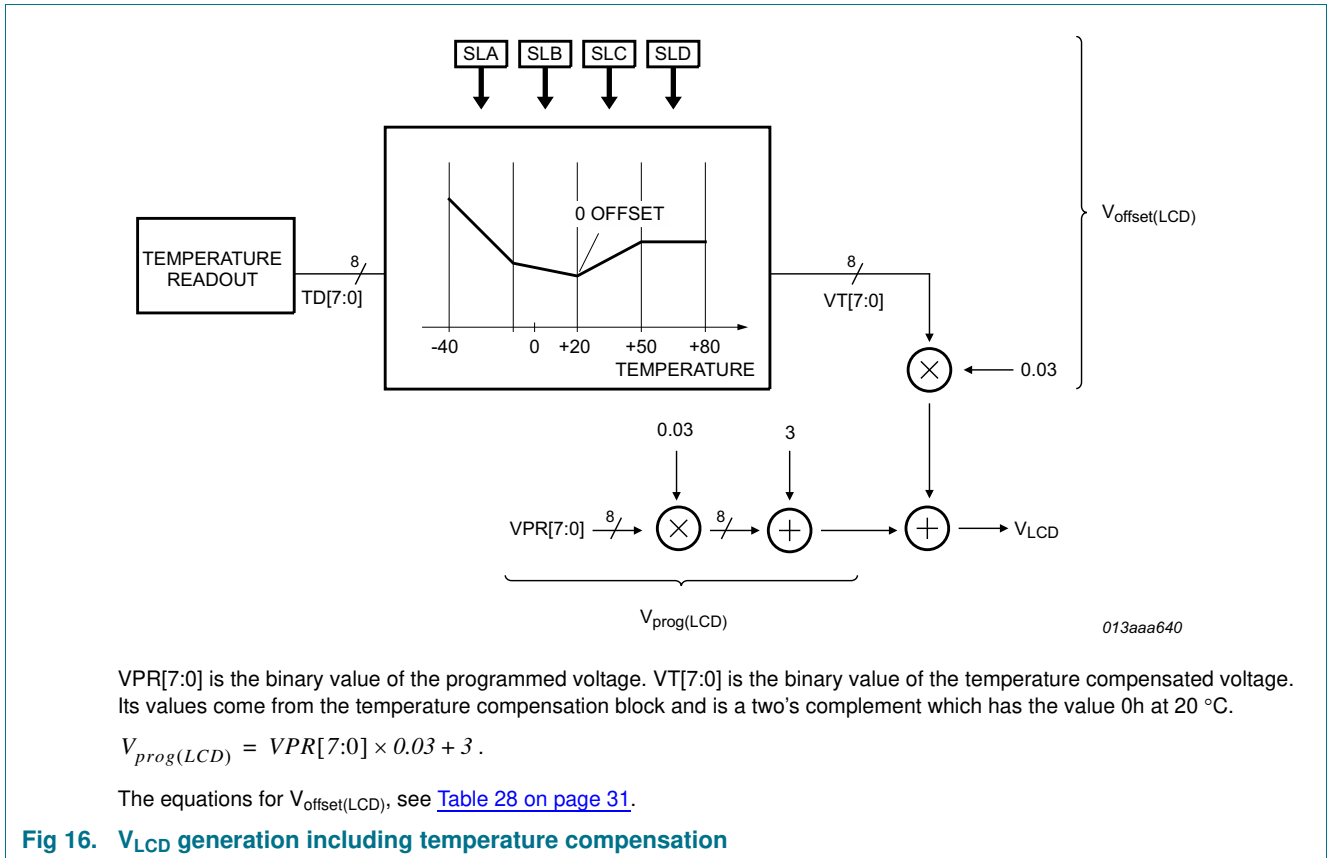
8.4.2 Internal V_{LCD} generation

V_{LCD} can be generated and controlled on the chip by using software commands. When the internal charge pump is used, the programmed V_{LCD} is available on pin VLCD. The charge pump generates a V_{LCD} of up to $3 \times V_{DD2}$. The charge pump can be enabled or disabled with the CPE bit (see Table 9 on page 9). With bit CPC, the charge pump multiplier setting can be configured.

The final value of V_{LCD} is a combination of the programmed $V_{prog(LCD)}$ value and the output of the temperature compensation block, $V_{offset(LCD)}$.

$$V_{LCD} = V_{prog(LCD)} + V_{offset(LCD)} \tag{1}$$

The system is shown in Figure 16.

VPR[7:0] is the binary value of the programmed voltage. VT[7:0] is the binary value of the temperature compensated voltage. Its values come from the temperature compensation block and is a two's complement which has the value 0h at 20 °C.

$$V_{prog(LCD)} = VPR[7:0] \times 0.03 + 3 \, .$$

The equations for $V_{offset(LCD)}$, see Table 28 on page 31.

Fig 16. V_{LCD} generation including temperature compensation

Figure 17 illustrates how V_{LCD} changes with the programmed value of VPR[7:0].