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PCA8538

Automotive 102 x 9 Chip-On-Glass LCD segment driver

Rev. 4 — 26 September 2014 Product data sheet

1. General description

The PCA8538 is a fully featured Chip-On-Glass (COG)[1] Liquid Crystal Display (LCD) driver, designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:9. It generates the drive signals for a static or multiplexed LCD containing up to 9 backplanes, 102 segments, and up to 918 segments/elements. The PCA8538 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCA8538 offers a programmable temperature compensation of the LCD supply voltage. The PCA8538 can be easily controlled by a microcontroller through either the two-line I^2C-bus or a four-line bidirectional SPI-bus.

For a selection of NXP LCD segment drivers, see Table 62 on page 97.

2. Features and benefits

- AEC Q100 grade 2 compliant for automotive applications
- Low power consumption
- Extended operating temperature range from −40 °C to +105 °C
- 102 segments and 9 backplanes allowing to drive:
  - up to 114 7-segment numeric characters
  - up to 57 14-segment alphanumeric characters
  - any graphics of up to 918 segments/elements
- 918-bit RAM for display data storage
- Two sets of backplane outputs providing higher flexibility for optimal COG layout configurations
- Up to 4 chips can be cascaded to drive larger displays with an internally generated or externally supplied V_{LCD}
- Selectable backplane drive configuration: static, 2, 4, 6, 8, or 9 backplane multiplexing
- LCD supply voltage
  - Programmable internal charge pump for on-chip LCD voltage generation up to $5 \times V_{DD2}$
  - External LCD voltage supply possible as well
- Selectable 400 kHz I^2C-bus or 3 MHz SPI-bus interface
- Selectable linear temperature compensation of V_{LCD}
- Selectable display bias configuration
- Wide range for digital and analog power supply: from 2.5 V to 5.5 V

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21 on page 99.

- Wide LCD voltage range from 4.0 V for low threshold LCDs up to 12.0 V for high threshold twisted nematic and Vertical Alignment (VA) displays
- Display memory bank switching in static, duplex, and quadruplex drive modes
- Programmable frame frequency in the range of 45 Hz to 300 Hz; factory calibrated with a tolerance of ±3 Hz (at 80 Hz)
- Selectable inversion scheme for LCD driving waveforms: frame or n-line inversion
- Diagnostic features for status monitoring
- Integrated temperature sensor with temperature readout
- On chip calibration of internal oscillator frequency and V_{LCD}
- Laser marking at the back-side of the die for traceability of the lot number, wafer number, and die position on the wafer

3. Applications

- Automotive
  - Instrument clusters
  - Climate control
  - Car entertainment
  - Car radio
- Industrial
  - Consumer
  - Medical and health care
  - Measuring equipment
  - Machine control systems
  - Information boards
  - White goods
  - General-purpose display modules

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8538UG	bare die	247 bumps	PCA8538UG

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA8538UG/2DA/Q1	935301433033	PCA8538UG/2DA/Q1Z	1	chips with bumps[1] in tray

[1] Bump hardness, see Table 60 on page 94.

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCA8538UG/2DA/Q1	on the active side of the die PC8538-1 on the rear side of the die[1] LLLLLLL WW XXXXXX

[1] The rear side marking has the following meaning:
LLLLLLL — wafer lot number
WW — wafer number
XXXXXX — die identification number

6. Block diagram

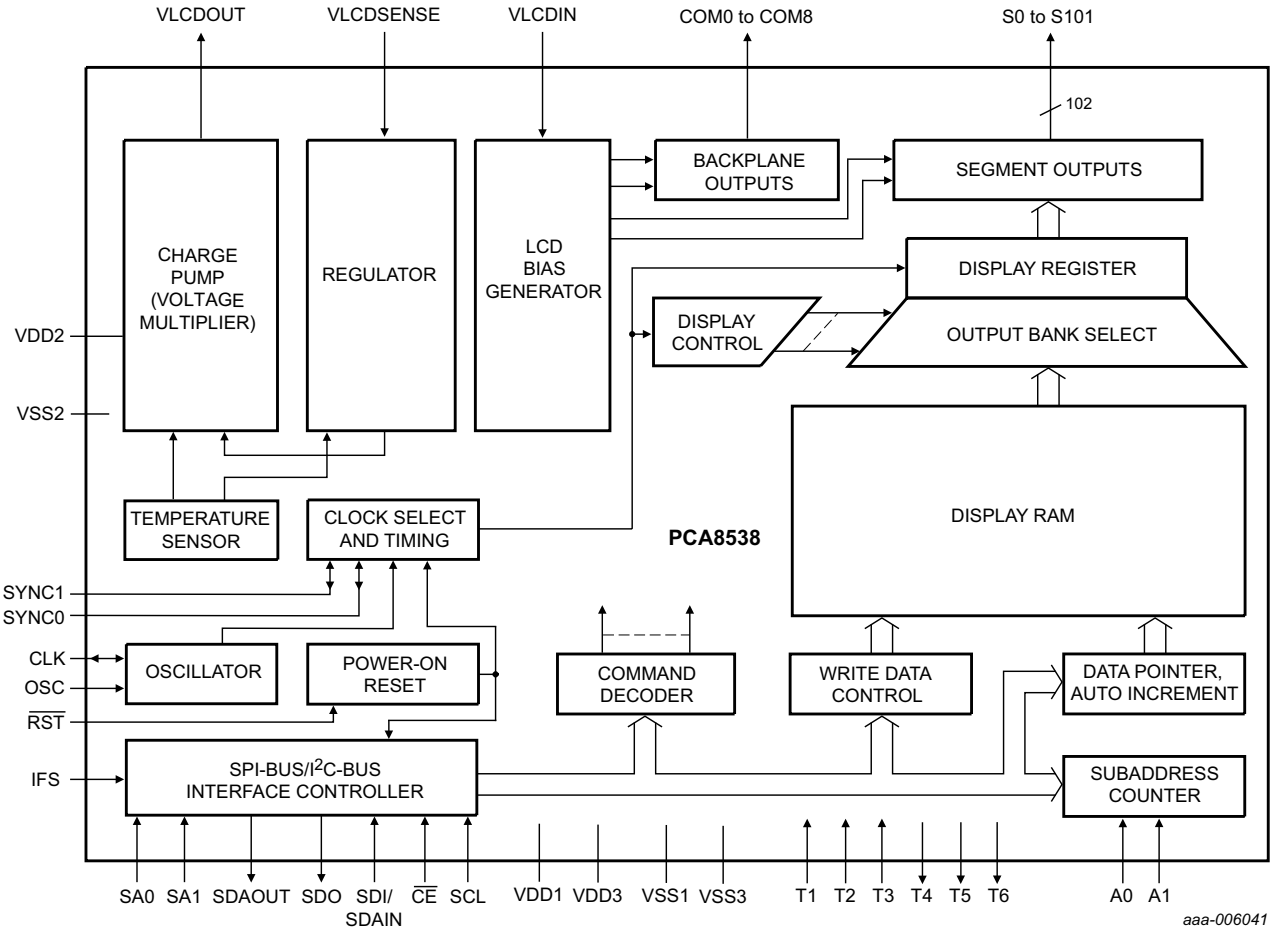
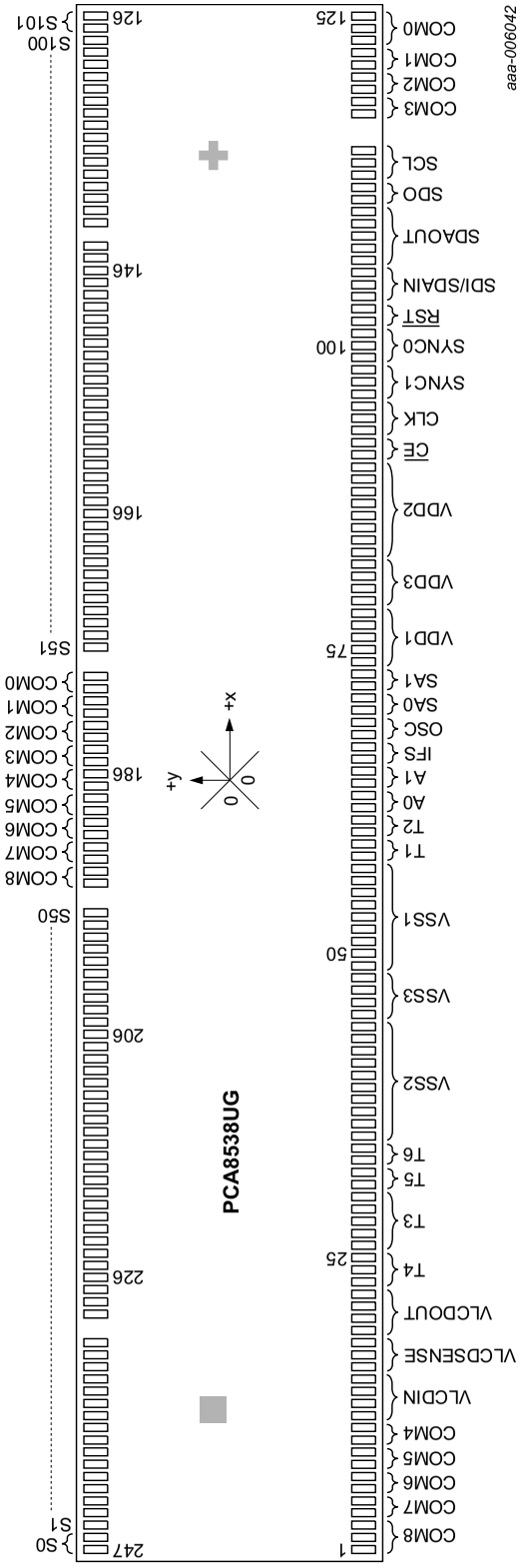


Fig 1. Block diagram of PCA8538

7. Pinning information

7.1 Pinning



Viewed from active side. For mechanical details, see Figure 64 on page 89.

Fig 2. Pinning diagram of PCA8538UG

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
Backplane output pins			
COM8	1 to 3, 194, 195	output	LCD backplane
COM7	4, 5, 192, 193		
COM6	6, 7, 190, 191		
COM5	8, 9, 188, 189		
COM4	10, 11, 186, 187		
COM3	117, 118, 184, 185		
COM2	119, 120, 182, 183		
COM1	121, 122, 180, 181		
COM0	123 to 125, 178, 179		
Segment output pins			
S101	126, 127	output	LCD segment
S100 to S51	128 to 177		
S50 to S1	196 to 245		
S0	246, 247		
V_{LCD} pins			
VLCDIN	12 to 15	supply	V_{LCD} input
VLCDSENSE	16 to 18	input	V_{LCD} regulation input
VLCDOUT	19 to 22	output	V_{LCD} output
Test pins			
T4	23 to 25	output	not accessible; must be left open
T3	26 to 30	input	not accessible; must be connected to T5
T5	31, 32	output	not accessible; must be connected to T3
T6	33, 34	output	not accessible; must be left open
T1	58, 59	input	not accessible; must be connected to V_{SS1}
T2	60, 61		
Supply pins			
VSS2[1]	35 to 44	supply	ground supply
VSS3[1]	45 to 48		
VSS1[1]	49 to 57		
VDD1	74 to 78	supply	supply voltage 1 (analog and digital)
VDD3	79 to 82	supply	supply voltage 3 (analog)
VDD2	83 to 90	supply	supply voltage 2 (charge pump)

Table 4. Pin description *...continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description	
Oscillator, synchronization, addressing, and reset pins				
CLK[2]	93 to 95	input/output	internal oscillator output, external oscillator input	
OSC[2]	68, 69	input	clock (internal/external) selector	
SYNC1[3]	96 to 98	input/output	charge pump synchronization for cascaded devices; must not be connected if V_{LCD} is externally supplied	
SYNC0[3]	99 to 101	input/output	display synchronization for cascaded devices	
$\overline{RST}$	102, 103	input	active LOW reset input	
A0	62, 63	input	hardware device address selection for cascading; • connect to V_{SS1} for logic 0 • connect to V_{DD1} for logic 1	
A1	64, 65			
Bus-related pins				
			SPI-bus	**I²C-bus**
IFS	66, 67	input	interface selector input	
			• connect to V_{SS1}	• connect to V_{DD1}
SA0	70, 71	input	unused; • connect to V_{SS1}	slave address selector; • connect to V_{SS1} for logic 0 • connect to V_{DD1} for logic 1
SA1	72, 73	input		
$\overline{CE}$	91, 92	input	chip enable input (active LOW)	unused; • connect to V_{DD1}
SDI/SDAIN	104 to 106	input	SPI-bus data input	I²C-bus serial data input
SDAOUT	107 to 111	output	unused; • must be connected to V_{SS1}	serial data output
SDO	112, 113	output	SPI serial data output	unused; • must be left open
SCL	114 to 116	input	serial clock input	serial clock input

[1] The substrate (rear side of the die) is connected to V_{SS1} and should be electrically isolated.

[2] If pin OSC is tied to V_{SS1}, CLK is the output pin of the internal oscillator. If pin OSC is tied to V_{DD1}, CLK is the input pin for the external oscillator.

[3] If cascading is not used, pin must be left floating; for cascading see Section 15.2 on page 85.

8. Functional description

8.1 Commands of PCA8538

The PCA8538 is controlled by the commands defined in Table 5.

Remark: Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCA8538.

Table 5. Commands of PCA8538

Command name		R/$\overline{W}$[1]	Register selection RS[1:0][2]		Command bits								Reference
					7	6	5	4	3	2	1	0	
General control commands													
Initialize		0	0	0	0	0	1	1	1	0	1	0	Section 8.2.1
OTP-refresh		0	0	0	1	1	0	1	1	0	0	0	Section 8.2.2
Device-address		0	0	0	0	0	0	1	1	0	A[1:0]		Section 8.2.3
SYNC1_pin		0	0	0	1	0	1	1	1	0	0	OE	Section 8.2.4
Clock-out-ctrl		0	0	0	1	1	0	1	0	1	0	COE	Section 8.2.5
Read-select		0	0	0	0	0	0	1	1	1	0	SO	Section 8.2.6
Status-readout	temperature	1	0	0	TD[7:0]								Section 8.2.7
	device status				SR7	SR6	SR5	SR4	SR[3:0]				
Clear-reset-flag		0	0	0	0	0	0	1	1	1	1	1	Section 8.2.8
Charge pump and LCD bias control commands													
Charge-pump-ctrl		0	0	0	1	1	0	0	CPE	CPC[2:0]			Section 8.3.1
Set-V_{LCD}	MSB	0	0	0	0	1	0	V[8:4]					Section 8.3.2
	LSB	0	0	0	0	1	1	0	V[3:0]				
Set-bias-mode		0	0	0	1	1	0	1	0	0	B[1:0]		Section 8.3.3

Table 5. Commands of PCA8538 *…continued*

Command name		R/$\overline{W}$[1]	Register selection RS[1:0][2]		Command bits								Reference
					7	6	5	4	3	2	1	0	
Temperature compensation control commands													
Temperature-ctrl		0	1	0	0	0	0	0	0	TCE	TMF	TME	Section 8.4.1
TC-slope	A	0	1	0	0	0	0	0	1	TSA[2:0]			Section 8.4.3
	B	0	1	0	0	0	0	1	0	TSB[2:0]			
	C	0	1	0	0	0	0	1	1	TSC[2:0]			
	D	0	1	0	0	0	1	0	0	TSD[2:0]			
	E	0	1	0	0	0	1	0	1	TSE[2:0]			
	F	0	1	0	0	0	1	1	0	TSF[2:0]			
TC-set	1	0	1	0	0	0	1	1	1	T1T[2:0]			Section 8.4.2
	2	0	1	0	0	1	0	0	0	T2T[2:0]			
	3	0	1	0	0	1	0	0	1	T3T[2:0]			
	4	0	1	0	0	1	0	1	0	T4T[2:0]			
Display control commands													
Set-MUX-mode		0	0	0	0	0	0	0	0	M[2:0]			Section 8.5.1
Inversion-mode		0	0	0	1	0	1	1	0	INV[2:0]			Section 8.5.2
Display-ctrl		0	0	0	0	0	1	1	1	0	0	DE	Section 8.5.3
Clock and frame frequency command													
Frame-frequency		0	0	0	1	1	1	FF[4:0]					Section 8.6.4
Display RAM commands													
Write-display-data		0	0	1	DB[7:0]								Section 8.7.1
Input-bank-select		0	0	0	0	0	0	0	1	IB[2:0]			Section 8.7.2
Output-bank-select		0	0	0	0	0	0	1	0	OB[2:0]			
Data-pointer-X	MSB	0	0	0	1	0	0	0	0	PX[6:4]			Section 8.7.3
	LSB	0	0	0	1	0	0	1	PX[3:0]				
Data-pointer-Y		0	0	0	1	0	1	0	0	0	0	PY0	

[1] For further information about the R/$\overline{W}$-bit, see Table 46 on page 63.

[2] For further information about the register selection bits, see Table 46 on page 63.

8.2 General control commands

8.2.1 Command: Initialize

This command generates a chip-wide reset by setting all commands to their default values. For further information, see Section 8.8 on page 23.

Table 6. Initialize command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00111010	fixed value

8.2.2 Command: OTP-refresh

Each IC is calibrated during production and testing of the device in order to achieve the specified accuracy of the V_{LCD}, the frame frequency, and the temperature measurement. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. These cells are read by the device after a reset and every time when the Initialize command or the OTP-refresh command is sent. This command takes approximately 10 ms to finish.

Table 7. OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	11011000	fixed value

8.2.3 Command: Device-address

The Device-address command allows setting the address of the device in a cascaded configuration and corresponds with pins A0 and A1 (see Section 15.2 on page 85).

Table 8. Device-address - device address command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	000110	fixed value
1 to 0	A[1:0]		**set address**
		00[1]	master
		01	slave 1
		10	slave 2
		11	slave 3

[1] Default value.

8.2.4 Command: SYNC1_pin

With the SYNC1_pin command, the SYNC1 pin can be configured for using the PCA8538 as a single chip or a master in a cascade. If the PCA8538 is a slave in a cascade, the command has no effect.

Table 9. SYNC1_pin - SYNC1 pin configuration command bit description

This command has no effect if the PCA8538 is a slave in a cascade.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1011100	fixed value
0	OE		**SYNC1 pin configuration**
		0[1]	pin SYNC1 is an output; gated to 0 V; to be used when PCA8538 is a single chip
		1	pin SYNC1 is an output; providing the synchronization signal; to be used when PCA8538 is a master in a cascade

[1] Default value.

8.2.5 Command: Clock-out-ctrl

When pin CLK is configured as an output pin, the Clock-out-ctrl command enables or disables the clock output on pin CLK (Section 8.6.1 on page 19).

Table 10. Clock-out-ctrl - CLK pin input/output switch command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1101010	fixed value
0	COE		**control pin CLK**
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

[1] Default value.

8.2.6 Command: Read-select

The Read-select command allows choosing to readout the temperature or the device status.

Table 11. Read-select - status read select command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0001110	fixed value
0	SO		**readout**
		0[1]	temperature; the Status-readout command allows to readout the temperature TD[7:0], see Table 12
		1	device status: the Status-readout command allows to readout some information about the status of the device, see Table 12

[1] Default value.

8.2.7 Command: Status-readout

The Status-readout command offers to readout some status bits of the PCA8538. These bits indicate the status of the device at the moment of reading.

Table 12. Status-readout - status and temperature read command bit description

For this command, bit R/$\overline{W}$ has to be set logic 1.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	1	fixed value
-	RS[1:0]	00	fixed value
Temperature readout if SO = 0 (see Table 11)			
7 to 0	TD[7:0]	00000000 to 11111111[1]	**temperature readout** (see Section 8.10.4.1 on page 38)
Device status readout if SO = 1 (see Table 11)			
7	SR7		**display status** (see Table 22 on page 19)
		0[1]	display is disabled
		1	display is enabled
6	SR6		**charge pump switching status** (status of bit CPE, see Table 14 on page 14)
		0[1]	charge pump disabled
		1	charge pump enabled
5	SR5		**charge pump charge status**
		0[1]	charge pump has not reached programmed value
		1	charge pump has reached programmed value

Table 12. Status-readout - status and temperature read command bit description *...continued*

For this command, bit R/$\overline{W}$ has to be set logic 1.

Bit	Symbol	Value	Description
4	SR4		**reset status flag**
		0	no reset has occurred since the reset status flag was cleared last time
		1[1]	reset has occurred since the reset status flag was cleared last time[2]
3 to 0	SR[3:0]		**EMC detection**
		01 SA1 SA0	pre-defined code for EMC detection when I^2C interface is used
		0101	pre-defined code for EMC detection when SPI interface is used

[1] Default value.

[2] The flag is set whenever a reset occurs, induced by $\overline{RST}$ pin, Power-On Reset (POR), or Initialize command. After power-on, the flag is set and should be cleared for reset monitoring.

Some bits of the Status-readout command have a certain probability of being changed by an EMC/ESD event. For example, an EMC/ESD event can cause a change of the hard-wired settings of SA1 or SA0. Therefore SR[3:0] can help to detect if an EMC/ESD event has occurred which has caused the change of a bit. In environments where EMC/ESD events may occur, it could be helpful to compare the result of the Status-readout command with the initial bit settings periodically.

8.2.8 Command: Clear-reset-flag

The Clear-reset-flag command clears the reset flag SR4, see Table 12.

Table 13. Clear-reset-flag - Clear-reset-flag command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00011111	fixed value

8.3 Charge pump and LCD bias control commands

8.3.1 Command: Charge-pump-ctrl

The Charge-pump-ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier settings.

Table 14. Charge-pump-ctrl - charge pump control command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	1100	fixed value
3	CPE		**charge pump status**
		0[1]	charge pump disabled; no internal V_{LCD} generation; external supply of V_{LCD}
		1	charge pump enabled; internal V_{LCD} generation; no external supply of V_{LCD}
2 to 0	CPC[2:0]		**charge pump voltage multiplier setting**
		000[1]	$V_{LCD} = 2 \times V_{DD2}$
		001	$V_{LCD} = 3 \times V_{DD2}$
		010	$V_{LCD} = 4 \times V_{DD2}$
		011	$V_{LCD} = 5 \times V_{DD2}$
		100 to 111	$V_{LCD} = V_{DD2}$ (direct mode)

[1] Default value.

8.3.2 Command: Set-V_{LCD}

The Set-V_{LCD} command allows setting the LCD voltage.

Table 15. Set-V_{LCD} - Set-V_{LCD} command bit description

Bit	Symbol	Value	Description
Set-V_{LCD}-MSB			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 5	-	010	fixed value
4 to 0	V[8:4]		**set V_{LCD} MSB**
		00000[1] to 11111	the 5 most significant bits of V[8:0]
Set-V_{LCD}-LSB			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	0110	fixed value
3 to 0	V[3:0]		**set V_{LCD} LSB**
		0000[1] to 1111	the 4 least significant bits of V[8:0]

[1] Default value.

A value of 0h corresponds to V_{LCD} = 4 V and values equal or higher than 10Ch correspond to V_{LCD} = 12 V without temperature compensation. Every LSB change corresponds to a V_{LCD} programming step of 0.03 V. For further information, see Equation 2 on page 33 and Section 8.10.3 on page 32.

8.3.3 Command: Set-bias-mode

Table 16. Set-bias-mode - set bias mode command bit description

This command is not applicable for the static drive mode.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	110100	fixed value
1 to 0	B[1:0]		**set bias mode**
		00[1], 01	$^1/_4$ bias
		11	$^1/_3$ bias
		10	$^1/_2$ bias

[1] Default value.

8.4 Temperature compensation control commands

8.4.1 Command: Temperature-ctrl

The Temperature-ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD} (see Section 8.10.4 on page 38).

Table 17. Temperature-ctrl - temperature measurement control command bit description

For this command, the register selection bits have to be set RS[1:0] = 10.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00000	fixed value
2	TCE		**temperature compensation control**
		0[1]	temperature compensation of V_{LCD} disabled
		1	temperature compensation of V_{LCD} enabled
1	TMF		**temperature measurement filter**
		0[1]	digital temperature filter disabled[2]
		1	digital temperature filter enabled
0	TME		**temperature measurement control**
		0[1]	temperature measurement disabled; no temperature readout possible
		1	temperature measurement enabled; temperature readout possible

[1] Default value.

[2] The unfiltered digital value of TD[7:0] is immediately available for the readout and V_{LCD} compensation.

8.4.2 Command: TC-set

The TC-set command allows defining six temperature intervals in the operating temperature range from −40 °C to +105 °C. For each of the temperature intervals, the TC-slope command (see Section 8.4.3) allows setting the temperature coefficient of V_{LCD}.

Table 18. TC-set - V_{LCD} temperature compensation set command bit description

For this command, the register selection bits have to be set RS[1:0] = 10.

Bit	Symbol	Value	Description
TC-set-1			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00111	fixed value
2 to 0	T1T[2:0]	000[1] to 111	see Table 33 on page 40
TC-set-2			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01000	fixed value
2 to 0	T2T[2:0]	000[1] to 111	see Table 33 on page 40
TC-set-3			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01001	fixed value
2 to 0	T3T[2:0]	000[1] to 111	see Table 33 on page 40
TC-set-4			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01010	fixed value
2 to 0	T4T[2:0]	000[1] to 111	see Table 33 on page 40

[1] Default value.

8.4.3 Command: TC-slope

The TC-slope command allows setting the temperature coefficients of V_{LCD} corresponding to six temperature intervals defined by the TC-set command.

Table 19. TC-slope - V_{LCD} temperature compensation slope command bit description

For this command, the register selection bits have to be set RS[1:0] = 10.

Bit	Symbol	Value	Description
TC-slope-A			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00001	fixed value
2 to 0	TSA[2:0]	000[1] to 111	see Table 34 on page 41
TC-slope-B			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00010	fixed value
2 to 0	TSB[2:0]	000[1] to 111	see Table 34 on page 41
TC-slope-C			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00011	fixed value
2 to 0	TSC[2:0]	000[1] to 111	see Table 34 on page 41
TC-slope-D			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00100	fixed value
2 to 0	TSD[2:0]	000[1] to 111	see Table 34 on page 41
TC-slope-E			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00101	fixed value
2 to 0	TSE[2:0]	000[1] to 111	see Table 34 on page 41
TC-slope-F			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00110	fixed value
2 to 0	TSF[2:0]	000[1] to 111	see Table 34 on page 41

[1] Default value.

8.5 Display control commands

8.5.1 Command: Set-MUX-mode

The Set-MUX-mode command allows setting the multiplex drive mode.

Table 20. Set-MUX-mode - set multiplex drive mode command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	00000	fixed value
2 to 0	M[2:0]		**set multiplex drive mode**
		000[1]	1:9 multiplex drive mode
		001	
		010	
		011	1:8 multiplex drive mode
		100	1:6 multiplex drive mode
		101	1:4 multiplex drive mode
		110	1:2 multiplex drive mode
		111	static

[1] Default value.

8.5.2 Command: Inversion-mode

The Inversion-mode command allows changing the drive scheme inversion mode.

The waveforms used to drive LCD displays (see Figure 25 on page 45 to Figure 33 on page 53) inherently produce a DC voltage across the display cell. The PCA8538 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of the compensation method is determined with INV[2:0] in Table 21.

Table 21. Inversion-mode - inversion mode command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	10110	fixed value
2 to 0	INV[2:0]		**set inversion mode**
		000[1]	frame inversion mode
		001	1-line inversion mode
		010	2-line inversion mode
		011	3-line inversion mode
		100	4-line inversion mode
		101	5-line inversion mode
		110	6-line inversion mode
		111	7-line inversion mode

[1] Default value.

8.5.2.1 Line inversion mode (driving scheme A)

In line inversion mode, the DC value is compensated every n^{th} line. Changing the inversion mode to line inversion mode reduces the possibility for flickering but increases the power consumption (see example waveforms in Figure 25 on page 45 to Figure 32 on page 52)

8.5.2.2 Frame inversion mode (driving scheme B)

In frame inversion mode, the DC value is compensated across two frames and not within one frame (see example waveform in Figure 33 on page 53). Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is possibility for flicker to occur.

8.5.3 Command: Display-ctrl

The Display-ctrl command enables or disables the display.

Table 22. Display-ctrl - display on and off switch command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0011100	fixed value
0	DE		**display control**
		0[1]	display disabled
		1	display enabled

[1] Default value.

8.6 Clock and frame frequency command

8.6.1 Oscillator

The internal logic and LCD drive signals of the PCA8538 are timed by the clock frequency f_{clk}, which is either internally generated by an on-chip oscillator circuit or externally supplied.

The clock frequency f_{clk} determines the internal data flow of the device that includes the transfer of display data from the display RAM to the display segment outputs and the generation of the LCD frame frequency.

8.6.2 External clock

When an external clock is used, the input pin OSC must be connected to V_{DD1}. The clock must be supplied to the CLK pin and must have an amplitude equal to the V_{DD1} voltage supplied to the chip and be referenced to V_{SS1}.

Remark: If an external clock is used, then this clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. Removal of the clock is possible when following the correct procedures as described in Section 8.8.4 on page 27.

8.6.3 Internal clock

In applications where the internal clock is used, the input pin OSC must be connected to V_{SS1}. It is possible to make the clock frequency available on pin CLK by setting bit COE logic 1 (see Table 10 on page 11). If pin CLK is not used, it should be left open. At power-on the signal at pin CLK is disabled and pin CLK is in 3-state.

8.6.4 Command: Frame-frequency

With this command the clock and frame frequency can be programmed when using the internal clock.

Table 23. Frame-frequency - frame frequency select command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 5	-	111	fixed value
4 to 0	FF[4:0]	see Table 24	**clock and frame frequency (Hz)**

The duty ratio of the clock output may change when choosing different values for the frame frequency (see Table 24).

The LCD frame frequency is derived from the clock frequency by a fixed division (see Equation 1).

$$f_{fr} = \frac{f_{clk}}{144} \quad (1)$$

The Frame-frequency command allows configuring the frame frequency in the range of 45 Hz to 300 Hz with steps of

- 5 Hz from 45 Hz to 100 Hz
- 10 Hz from 100 Hz to 300 Hz

The default frame frequency of 80 Hz is factory calibrated with a tolerance of ±3 Hz at 25 °C.

Table 24. Clock and frame frequency values

Duty cycle definition: % HIGH-level time : % LOW-level time.

FF[4:0]	Frame frequency (Hz)	Clock frequency (Hz)	Typical duty cycle (%)[1]
00000	45	6472	29 : 71
00001	50	7200	20 : 80
00010	55	7945	12 : 88
00011	60	8662	4 : 96
00100	65	9366	48 : 52
00101	70	10105	44 : 56
00110	75	10766	41 : 59
00111[1]	80	11520	36 : 64
01000	85	12255	32 : 68
01001	90	12944	29 : 71
01010	95	13714	24 : 76

Table 24. Clock and frame frequency values *...continued*

Duty cycle definition: % HIGH-level time : % LOW-level time.

FF[4:0]	Frame frequency (Hz)	Clock frequency (Hz)	Typical duty cycle (%)[1]
01011	100	14400	20 : 80
01100	110	15781	13 : 87
01101	120	17194	5 : 95
01110	130	18581	49 : 51
01111	140	20211	44 : 56
10000	150	21736	40 : 60
10001	160	23040	36 : 64
10010	170	24511	32 : 68
10011	180	26182	28 : 72
10100	190	27429	24 : 76
10101	200	28800	20 : 80
10110	210	30316	16 : 84
10111	220	32000	12 : 88
11000	230	32914	9 : 91
11001	240	34909	4 : 96
11010	250	36000	50 : 50
11011	260	37161	49 : 51
11100	270	38400	47 : 53
11101	280	39724	45 : 55
11110	290	41143	43 : 57
11111	300	42667	41 : 59

[1] Default value.

8.7 Display RAM commands

8.7.1 Command: Write-display-data

The Write-display-data command writes data byte-wise to the RAM. After Power-On Reset (POR) the RAM content is random and should be brought to a defined status by clearing it (setting it logic 0).

Table 25. Write-display-data - write display data command bit description

For this command, the register selection bits have to be set RS[1:0] = 01.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	01	fixed value
7 to 0	DB[7:0]	00000000 to 11111111	**writing data byte-wise to RAM**

More information about the display RAM can be found in Section 8.14 on page 55.

8.7.2 Bank select commands

For multiplex drive modes 1:4, 1:2, and static drive mode, it is possible to write data to one area of the RAM while displaying from another. These areas are named as RAM banks. Input and output banks can be set independently from one another with the Input-bank-select and the Output-bank-select command. More information about RAM bank switching can be found in Section 8.14.3 on page 59.

8.7.2.1 Command: Input-bank-select

Table 26. Input-bank-select - input bank select command bit description

This command is not applicable for multiplex drive mode 1:6, 1:8, and 1:9.

Bit	Symbol	Value	Description		
-	R/$\overline{W}$	0	fixed value		
-	RS[1:0]	00	fixed value		
7 to 3	-	00001	fixed value		
2 to 0	IB[2:0]		**selects RAM bank to write to**		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[1]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[1] Default value.

8.7.2.2 Command: Output-bank-select

Table 27. Output-bank-select - output bank select command bit description

This command is not applicable for multiplex drive mode 1:6, 1:8, and 1:9.

Bit	Symbol	Value	Description		
-	R/$\overline{W}$	0	fixed value		
-	RS[1:0]	00	fixed value		
7 to 3	-	00010	fixed value		
2 to 0	OB[2:0]		**selects RAM bank to read from to the LCD**		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[1]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[1] Default value.

8.7.3 Commands: Data-pointer-X and Data-pointer-Y

The Data-pointer-X and Data-pointer-Y commands define the display RAM address where the following display data will be sent to.

Table 28. Data-pointer-X and Data-pointer-Y - set data pointer command bit description

For further information about the RAM, see Section 8.14 on page 55.

Bit	Symbol	Value	Description
Data-pointer-X-MSB: PX[6:4]			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	10000	fixed value
2 to 0	PX[6:4]	000[1] to 111	3-bit binary value
Data-pointer-X-LSB: PX[3:0]			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	1001	fixed value
3 to 0	PX[3:0]	0000[1] to 1111	4-bit binary value
Data-pointer-Y: PY0			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1010000	fixed value
0	PY0	0[1] to 1	1-bit binary value

[1] Default value.

8.8 Start-up and shut-down

8.8.1 Power-On Reset (POR)

At power-on, the PCA8538 resets to the following starting conditions:

1. All backplane and segment outputs are set to V_{SS1}.
2. Selected drive mode is: 1:9 with ¼ bias.
3. Input and output bank selectors are reset.
4. The interface is initialized.
5. The data pointer is cleared (set logic 0).
6. The internal oscillator is disabled.
7. Temperature measurement is disabled.
8. Temperature filter is disabled.
9. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
10. The V_{LCD} temperature compensation is disabled.
11. The display is disabled.

The reset state is as shown in Table 29.

Table 29. Reset state of PCA8538

Command name	Command bits							
	7	6	5	4	3	2	1	0
General control commands								
Device-address	0	0	0	1	1	0	0	0
SYNC1_pin	1	0	1	1	1	0	0	0
Clock-out-ctrl	1	1	0	1	0	1	0	0
Read-select	0	0	0	1	1	1	0	0
Status-readout	1	1	1	1	1	1	1	1
	0	0	0	1	0	1	0/SA1	1/SA0
Charge pump and LCD bias control commands								
Charge-pump-ctrl	1	1	0	0	0	0	0	0
Set-V_{LCD}	0	1	0	0	0	0	0	0
	0	1	1	0	0	0	0	0
Set-bias-mode	1	1	0	1	0	0	0	0
Temperature compensation control commands								
Temperature-ctrl	0	0	0	0	0	0	0	0
TC-slope-A	0	0	0	0	1	0	0	0
TC-slope-B	0	0	0	1	0	0	0	0
TC-slope-C	0	0	0	1	1	0	0	0
TC-slope-D	0	0	1	0	0	0	0	0
TC-slope-E	0	0	1	0	1	0	0	0
TC-slope-F	0	0	1	1	0	0	0	0
TC-set-1	0	0	1	1	1	0	0	0
TC-set-2	0	1	0	0	0	0	0	0
TC-set-3	0	1	0	0	1	0	0	0
TC-set-4	0	1	0	1	0	0	0	0
Display control commands								
Set-MUX-mode	0	0	0	0	0	0	0	0
Inversion-mode	1	0	1	1	0	0	0	0
Display-ctrl	0	0	1	1	1	0	0	0
Clock and frame frequency command								
Frame-frequency	1	1	1	0	0	1	1	1
Display RAM commands								
Input-bank-select	0	0	0	0	1	0	0	0
Output-bank-select	0	0	0	1	0	0	0	0
Data-pointer-X-MSB	1	0	0	0	0	0	0	0
Data-pointer-X-LSB	1	0	0	1	0	0	0	0
Data-pointer-Y	1	0	1	0	0	0	0	0

Remarks:

1. Do not transfer data for at least 1 ms after a power-on to allow the reset action to complete.

2. The first command sent to the device after the power-on event must be the Initialize command (see Section 8.2.1 on page 10).
3. After Power-On Reset (POR) and before enabling the display, the RAM content should be brought to a defined status
   - by clearing it (setting it all logic 0) or
   - by writing meaningful content (for example, a graphic)

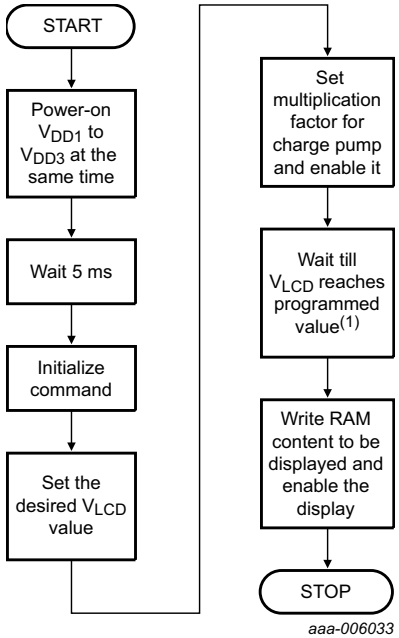
   otherwise unwanted display artifacts may appear on the display.

8.8.2 Reset pin function

The reset pin of the PCA8538 resets all the registers to their default state (see Table 29). The RAM contents remain unchanged. After the reset signal is removed, the PCA8538 will behave in the same manner as at POR. See Section 8.8.1 for details.

8.8.3 Recommended start-up sequences

This section describes how to proceed with the initialization of the chip in different application modes.



(1) This time depends on the external capacitor on the V_{LCD} pins. For a capacitor of 100 nF a delay of about 55 ms to 65 ms is expected.

Fig 3. Recommended start-up sequence when using the internal charge pump and the internal clock signal

When using the internal V_{LCD} generation, the display must not be enabled before the generation of V_{LCD} with the internal charge pump is completed. Otherwise unwanted display artifacts may appear on the display.