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# PCA8539

## 100 x 18 Chip-On-Glass automotive LCD dot matrix driver

Rev. 2 — 12 September 2014 Product data sheet

## 1. General description

The PCA8539 is a fully featured Liquid Crystal Display (LCD)[1] driver, specifically designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:18. It generates the drive signals for multiplexed LCD containing up to 18 backplanes, 100 segments, and up to 1800 elements/segments. The PCA8539 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCA8539 offers a programmable temperature compensation of the LCD supply voltage. The PCA8539 can be easily connected to a microcontroller by either the two-line $I^2C$-bus or a four-line bidirectional SPI-bus.

For a selection of NXP LCD graphic drivers, see Table 50 on page 86.

## 2. Features and benefits

- AEC Q100 grade 2 compliant for automotive applications
- Single-chip LCD controller and driver
- Extended operating temperature range from −40 °C to +105 °C
- 100 segments and 18 backplanes allowing to drive any graphic with up to 1800 elements
- On-chip:
  - Configurable 4, 3, or 2 times voltage multiplier generating LCD supply voltage, independent of $V_{DD}$, programmable by instruction (external supply also possible)
  - Integrated temperature sensor with temperature readout
  - Temperature compensation of on-chip generated VLCDOUT. Selectable linear temperature compensation of $V_{LCD}$
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Readout of RAM and registers possible
- Diagnostic features:
  - Checksum on $I^2C$ and SPI bus
- Frame frequency: programmable from 45 Hz to 360 Hz
- 2960-bit RAM for storage (1800 bit for display data)
- Two-line $I^2C$-bus interface or four-line SPI bus
- Multiplex drive mode 1:18 and 1:12
- Inversion modes
  - n-line (n = 1 to 7) inversion

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

- Frame inversion
- Large supply voltage range: $V_{DD1}$: 2.5 V to 5.5 V (chip can be driven with battery cells)
- Analog supply voltage $V_{DD2}$: 2.5 V to 5.5 V
- LCD supply voltage $V_{LCD}$: 4 V to 16 V
- Very low current consumption (20 μA to 200 μA):
  - Power-down mode: < 2 μA

## 3. Applications

- Automotive
  - Instrument clusters
  - Climate control display
  - Car entertainment
  - Car radio
- Industrial
  - Medical and health care
  - Measuring equipment
  - Machine control systems
  - Information boards
  - General-purpose display modules
- Consumer
  - White goods
  - Home entertainment

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PCA8539DUG | bare die | 244 bumps | PCA8539DUG |

## 4.1 Ordering options

**Table 2. Ordering options**

| Product type number | Sales item (12NC) | Orderable part number | IC revision | Delivery form |
|---|---|---|---|---|
| PCA8539DUG/DA | 935301519033 | PCA8539DUG/DAZ | 1 | chips with gold bumps in tray |

# 5. Marking

Each die has a laser marking on the rear side. The format is LLLLLLLWWXXXXXX having the following meaning:

LLLLLLL - wafer lot number

WW - wafer number

XXXXXX - die identification number

# 6. Block diagram

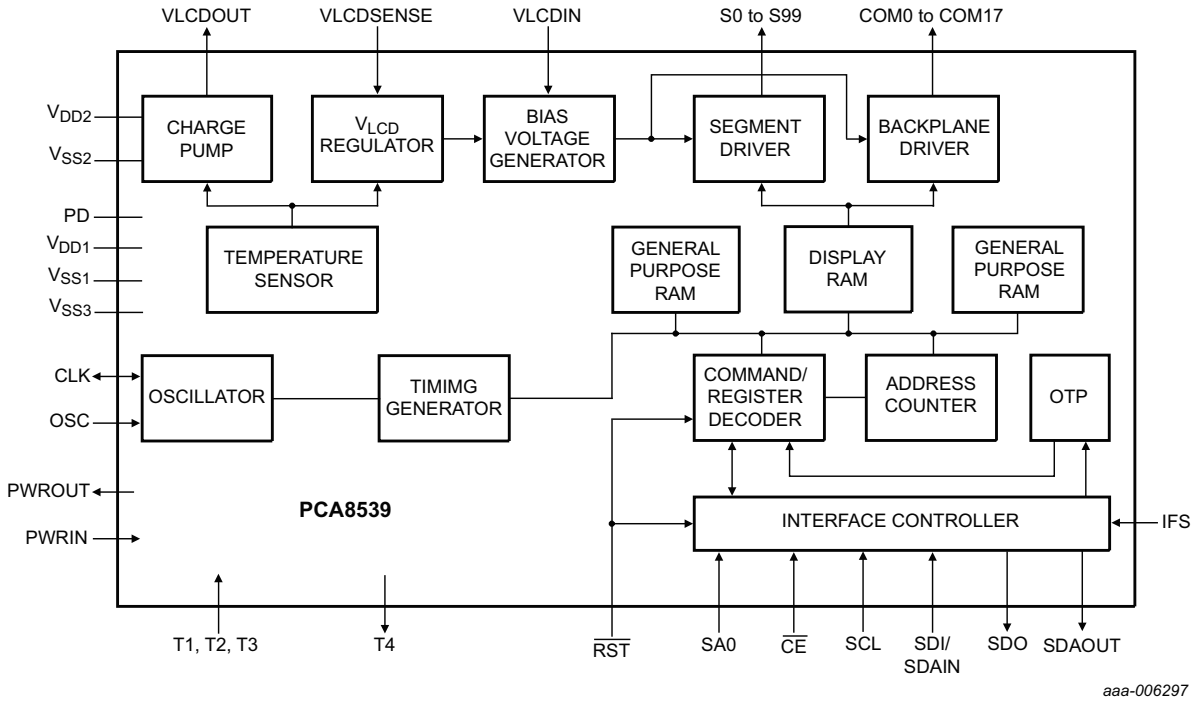



**Fig 1. Block diagram of PCA8539**

# 7. Pinning information

## 7.1 Pinning

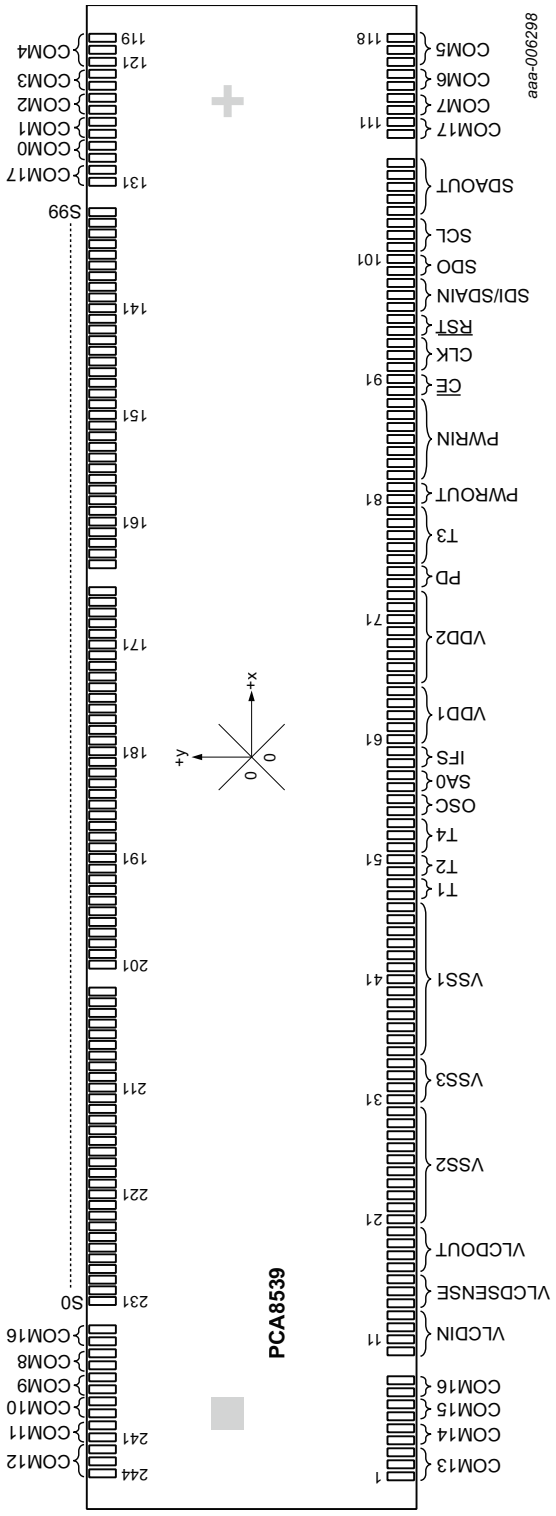



Fig 2. Pin configuration for PCA8539DUG

## 7.2 Pin description

**Table 3. Pin description of PCA8539DUG**

*Input or input/output pins must always be at a defined level ($V_{SS}$ or $V_{DD}$) unless otherwise specified.*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| **Backplane output pins** | | | |
| COM13 | 1 to 3 | output | LCD backplane |
| COM14 | 4, 5 | | |
| COM15 | 6, 7 | | |
| COM16 | 8, 9, 232, 233 | | |
| COM17 | 110, 111, 130, 131 | | |
| COM7 | 112, 113 | | |
| COM6 | 114, 115 | | |
| COM5 | 116 to 118 | | |
| COM4 | 119 to 121 | | |
| COM3 | 122, 123 | | |
| COM2 | 124, 125 | | |
| COM1 | 126, 127 | | |
| COM0 | 128, 129 | | |
| COM8 | 234, 235 | | |
| COM9 | 236, 237 | | |
| COM10 | 238, 239 | | |
| COM11 | 240, 241 | | |
| COM12 | 242 to 244 | | |
| **Segment output pins** | | | |
| S99 to S0 | 132 to 231 | output | LCD segment driver output |
| **$V_{LCD}$ pins** | | | |
| VLCDIN | 10 to 13 | supply | $V_{LCD}$ input |
| VLCDSENSE | 14 to 16 | input | $V_{LCD}$ regulation input |
| VLCDOUT | 17 to 20 | output | $V_{LCD}$ output |
| **Supply pins** | | | |
| VSS2[1] | 21 to 30 | supply | ground supply |
| VSS3[1] | 31 to 34 | | |
| VSS1[1] | 35 to 47 | | |
| VDD1 | 61 to 65 | supply | supply voltage 1 |
| VDD2 | 66 to 73 | supply | supply voltage 2 |
| PWROUT | 81, 82 | output | regulated voltage output; must be connected to PWRIN |
| PWRIN | 83 to 89 | input | regulated voltage input; must be connected to PWROUT |
| **Test pins** | | | |
| T1 | 48, 49 | input | not accessible; must be connected to $V_{SS1}$ |
| T2 | 50, 51 | | |
| T4 | 52 to 54 | output | not accessible; must be left open |

**Table 3. Pin description of PCA8539DUG** *…continued*

*Input or input/output pins must always be at a defined level ($V_{SS}$ or $V_{DD}$) unless otherwise specified.*

| Symbol | Pin | Type | Description | |
|---|---|---|---|---|
| T3 | 76 to 80 | input | not accessible; must be connected to PWROUT | |
| **Oscillator, synchronization, and reset pins** | | | | |
| OSC[2] | 55, 56 | input | clock (internal/external) selector | |
| PD | 74, 75 | input | power-down mode select<br>• for normal operation, pin PD must be LOW<br>• for power-down mode, pin PD must be HIGH | |
| CLK | 92 to 94 | input/output | internal oscillator output, external oscillator input | |
| $\overline{RST}$ | 95, 96 | input | active LOW reset input | |
| **Bus-related pins** | | | | |
| | | | **SPI-bus** | **I²C-bus** |
| SA0 | 57, 58 | input | unused;<br>• connect to $V_{SS1}$ | slave address selector;<br>• connect to $V_{SS1}$ for logic 0<br>• connect to $V_{DD1}$ for logic 1 |
| IFS | 59, 60 | input | interface selector input<br>• connect to $V_{SS1}$ | interface selector input<br>• connect to $V_{DD1}$ |
| $\overline{CE}$ | 90, 91 | input | chip enable input (active LOW) | unused<br>• connect to $V_{DD1}$ |
| SDI/SDAIN | 97 to 99 | input | SPI-bus data input | I²C-bus serial data input |
| SDO | 100, 101 | output | SPI serial data output | unused<br>• must be left open |
| SCL | 102 to 104 | input | serial clock input | serial clock input |
| SDAOUT | 105 to 109 | output | unused<br>• must be connected to $V_{SS1}$ | serial data output |

[1] The substrate (rear side of the die) is at $V_{SS1}$ potential and must not be connected.

[2] If pin OSC is tied to $V_{SS1}$, CLK is the output pin of the internal oscillator. If pin OSC is tied to $V_{DD1}$, CLK is the input pin for the external oscillator.

# 8. Functional description

## 8.1 Commands of PCA8539

The commands defined in Table 5 control the PCA8539.

The sequence to execute a command is like shown in Table 4:

**Table 4. Command execution sequence**

| Bus | Byte 1 | Byte 2 | Byte 3 |
|---|---|---|---|
| $I^2C$ | slave address[1] + R/$\overline{W}$[2] | CO + RS[1:0][3] | command |
| SPI | R/$\overline{W}$[2] + subaddress[4] | CO + RS[1:0][3] | command |

[1] More about the slave address, see Section 9.2.7.

[2] See Section 9.2.7 and Section 9.3.1.

[3] See Section 9.1.

[4] More about the subaddress, see Section 9.3.1.

**Remark:** Any other combinations of operation code bits that are not mentioned in this document can lead to undesired operation modes of PCA8539.

**Table 5. Commands of PCA8539**

*Bit positions labeled as - are not implemented have to be always written with 0.*

| Command name | R/$\overline{W}$ | Command select | | Bits | | | | | | | | Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RS[1:0] | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| **General control commands** | | | | | | | | | | | | |
| Initialize | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Section 8.1.1.1 |
| Clear_reset_flag | | | | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | Section 8.1.1.2 |
| OTP_refresh | | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Section 8.1.1.3 |
| Clock_out_ctrl | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | COE | Section 8.1.1.4 |
| Read_reg_select | | | | 0 | 0 | 0 | 0 | 0 | 1 | XC | SO | Section 8.1.1.5 |
| Read_status_reg | 1 | | | TD[7:0] | | | | | | | | Section 8.1.1.6 |
| | | | | CS[7:0] | | | | | | | | |
| | | | | Status_Register_1 to Status_Register_9 | | | | | | | | |
| Graphic_mode_cfg | 0 | | | 0 | 1 | 0 | 1 | 0 | GMX | - | - | Section 8.1.1.7 |
| Sel_mem_bank | | | | 0 | 0 | 0 | 1 | 0 | SMB[2:0] | | | Section 8.1.1.8 |
| Set_mem_addr | | | | 1 | ADD[6:0] | | | | | | | Section 8.1.1.9 |
| Read_data | 1 | 0 | 1 | RD[7:0] | | | | | | | | Section 8.1.1.10 |
| | | | | 0 | 0 | 0 | RD[4:0] | | | | | |
| Write_data | 0 | | | WD[7:0] | | | | | | | | Section 8.1.1.11 |
| | | | | 0 | 0 | 0 | WD[4:0] | | | | | |

**Table 5. Commands of PCA8539** *…continued*

*Bit positions labeled as - are not implemented have to be always written with 0.*

| Command name | R/$\overline{W}$ | Command select | Bits | | | | | | | | Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RS[1:0] | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| **Display control commands** | | | | | | | | | | | |
| Entry_mode_set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | I_D | - | Section 8.1.2.1 |
| Inversion_mode | | | | 0 | 1 | 0 | 0 | 0 | INV[2:0] | | | Section 8.1.2.2 |
| Frame_frequency | | | | 1 | 0 | 0 | FF[4:0] | | | | | Section 8.1.2.3 |
| Display_control | | | | 0 | 0 | 1 | 0 | 0 | D | - | - | Section 8.1.2.4 |
| Display_config | | | | 0 | 0 | 0 | 0 | 0 | 1 | P | - | Section 8.1.2.5 |
| **Charge pump and LCD bias control commands** | | | | | | | | | | | |
| Charge_pump_ctrl | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | CPE | CPC[1:0] | | Section 8.1.3.1 |
| Set_VLCD | | | | 1 | 0 | 1 | VLCD[8:4] | | | | | Section 8.1.3.2 |
| | | | | 1 | 0 | 0 | 1 | VLCD[3:0] | | | | |
| **Temperature compensation control commands** | | | | | | | | | | | |
| Temperature_ctrl | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | TCE | TMF | TME | Section 8.1.4.1 |
| TC_slope | | | | 0 | 0 | 0 | 0 | 1 | TSA[2:0] | | | Section 8.1.4.2 |
| | | | | 0 | 0 | 0 | 0 | 1 | TSB[2:0] | | | |
| | | | | 0 | 0 | 0 | 1 | 1 | TSC[2:0] | | | |
| | | | | 0 | 0 | 1 | 0 | 0 | TSD[2:0] | | | |

## 8.1.1 General control commands

### 8.1.1.1 Command: Initialize

This command generates a chip-wide reset by setting all command registers to their default values. It must be sent to the PCA8539 after power-on. For further information, see Section 8.2.1 on page 21.

**Table 6. Initialize - Initialize command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 to 0 | - | 00000001 | **initialize** |

### 8.1.1.2 Command: Clear_reset_flag

The Clear_reset_flag command clears the reset flag CRF, see Table 11 on page 11.

**Table 7. Clear_reset_flag - Clear_reset_flag command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 to 0 | - | 00011111 | **clear reset status flag** |

#### 8.1.1.3 Command: OTP_refresh

In order to achieve the specified accuracy of the $V_{LCD}$, the frame frequency, and the temperature measurement, each IC is calibrated during production. These calibration values are stored in One Time Programmable (OTP) cells. Their content is loaded into the associated registers every time when the Initialize command or the OTP_refresh command is sent. This command takes approximately 10 ms to finish.

**Table 8. OTP_refresh - OTP_refresh command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 to 0 | - | 00000010 | **refresh register settings from OTP** |

#### 8.1.1.4 Command: Clock_out_ctrl

When pin CLK is configured as an output pin, the Clock_out_ctrl command enables or disables the clock output on pin CLK.

**Table 9. Clock_out_ctrl - CLK pin input/output switch command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 to 1 | - | 0010000 | fixed value |
| 0 | COE | | **CLK pin setting** |
| | | 0[1] | clock signal not available on pin CLK; pin CLK is in 3-state |
| | | 1 | clock signal available on pin CLK |

[1] Default value.

For lower power consumption, the clock is only active when display (see Table 21), charge pump (see Table 23), or temperature measurement (see Table 25) is enabled.

#### 8.1.1.5 Command: Read_reg_select

The Read_reg_select command allows choosing to read out the temperature or the status registers Checksum to Status_Register_9 of the device (see Table 11).

**Table 10. Read_reg_select - select registers for readout command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 to 2 | - | 000001 | fixed value |
| 1 | XC | | **checksum mode setting** |
| | | 0[1] | XOR checksum |
| | | 1 | CRC-8 checksum |
| 0 | SO | | **readout select** |
| | | 0[1] | temperature |
| | | 1 | status registers |

[1] Default value.

#### 8.1.1.6 Command: Read_status_reg

With the Read_status_reg command the temperature, checksum, and the status registers can be read out. The behavior of the Read_status_reg command is controlled by the SO bit of the Read_reg_select command (see Table 10).

**Table 11. Read_status_reg - readout register command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 1 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| **Temperature readout if SO = 0 (see Table 10)** | | | |
| 7 to 0 | TD[7:0] | 00000000 to 11111111[1] | **temperature readout** |
| **Status readout if SO = 1 (see Table 10)** | | | |
| Checksum | | | |
| 7 to 0 | CS[7:0] | 00000000[1] to 11111111 | **checksum result** from RAM writing with checksum mode set by bit XC (see Table 10) |
| Status_Register_1 | | | |
| 7 | - | 0 | fixed value |
| 6 | GMX | | **multiplex drive mode setting status** |
| 5, 4 | - | 00 | fixed value |
| 3 | I_D | see Table 17 | **address stepping select status** |
| 2 to 0 | - | 000 | fixed value |
| Status_Register_2 | | | |
| 7 to 5 | INV[2:0] | see Table 18 | **inversion mode setting status** |
| 4 to 0 | FF[4:0] | see Table 20 | **frame frequency setting status** |
| Status_Register_3 | | | |
| 7 | D | see Table 21 | **display setting status** |
| 6 to 2 | - | 00000 | fixed value |
| 1 | P | see Table 22 | **display segment setting status** |
| 0 | - | 0 | fixed value |
| Status_Register_4 | | | |
| 7 to 5 | - | 000 | fixed value |
| 4 | CPE | see Table 23 | **charge pump setting status** |
| 3 | - | 0 | fixed value |
| 2, 1 | CPC[1:0] | see Table 23 | **charge pump voltage multiplier setting status** |
| 0 | VLCD8 | see Table 24 | **$V_{LCD}$ values setting** |
| Status_Register_5 | | | |
| 7 to 0 | VLCD[7:0] | see Table 24 | **$V_{LCD}$ values setting** |
| Status_Register_6 | | | |
| 7 | TCE | see Table 25 | **temperature compensation setting status** |
| 6 | TMF | | **temperature measurement filter setting status** |

**Table 11. Read_status_reg - readout register command bit description** *...continued*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 5 to 3 | TSA[2:0] | see Table 26 | **temperature compensation slope A setting status** |
| 2 to 0 | TSB[2:0] | | **temperature compensation slope B setting status** |
| Status_Register_7 | | | |
| 7 | TME | see Table 25 | **temperature measurement setting status** |
| 6 to 4 | TSC[2:0] | see Table 26 | **temperature compensation slope C setting status** |
| 3 to 1 | TSD[2:0] | | **temperature compensation slope D setting status** |
| 0 | - | 0 | fixed value |
| Status_Register_8 | | | |
| 7 to 0 | - | 00000000 | fixed value |
| Status_Register_9 | | | |
| 7 to 3 | - | 00000 | fixed value |
| 2 | QPR | | **charge pump charge status** |
| | | 0 | charge pump has not reached programmed value |
| | | 1 | charge pump has reached programmed value |
| 1 | CRF | | **reset flag status** the reset flag is set whenever a reset occurs; it should be cleared for reset monitoring (see Table 7) |
| | | 0 | no reset has occurred since the reset flag register was cleared last time |
| | | 1[1] | reset has occurred since the reset flag register was cleared last time |
| 0 | COE | see Table 9 | **CLK pin setting status** |

[1] Start-up value.

### 8.1.1.7 Command: Graphic_mode_cfg

The Graphic_mode_cfg command allows setting the multiplex drive mode.

**Table 12. Graphic_mode_cfg - graphic mode command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 to 3 | - | 01010 | fixed value |
| 2 | GMX | | **multiplex drive mode setting** |
| | | 0 | 1:18 multiplex drive mode |
| | | 1[1] | 1:12 multiplex drive mode |
| 1, 0 | - | - -[2] | not implemented |

[1] Default value.

[2] Not implemented, have to be always written with 0.

#### 8.1.1.8 Command: Sel_mem_bank

The Sel_mem_bank command determines which RAM to access.

**Table 13. Sel_mem_bank - RAM access configuration command**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 to 3 | - | 00010 | fixed value |
| 2 to 0 | SMB[2:0] | | **RAM access select** |
| | | 000[1] | general-purpose RAM 1 is selected |
| | | 001 | display RAM bank 1 is selected |
| | | 010 | display RAM bank 2 is selected |
| | | 011 | display RAM bank 3 is selected |
| | | 100 | general-purpose RAM 2 is selected |
| | | 101 to 111 | not implemented |

[1] Default value.

#### 8.1.1.9 Command: Set_mem_addr

The Set_mem_addr command allows setting the RAM address in the address counter to access. The Sel_mem_bank command (see Section 8.1.1.8) determines whether to access the display RAM or the general-purpose RAM.

**Table 14. Set_mem_addr - memory address command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 00 | fixed value |
| 7 | - | 1 | fixed value |
| 6 to 0 | ADD[6:0] | 0000000[1] to 1111111 | **RAM address** |

[1] Default value.

#### 8.1.1.10 Command: Read_data

The Read_data command reads binary 8-bit data from the display RAM or general-purpose RAM.

**Table 15. Read_data - data read bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 1 | fixed value |
| - | RS[1:0] | 01 | fixed value |
| **General-purpose RAM 1** | | | |
| 7 to 0 | RD[7:0] | 00000000 to 11111111 | **read data from general-purpose RAM 1** |
| **Display RAM bank 1 to 3, general-purpose RAM 2** | | | |
| 7 to 5 | - | 000 | fixed value |
| 4 to 0 | RD[4:0] | 00000 to 11111 | **read data from display RAM bank 1 to 3 and general-purpose RAM 2** |

The Sel_mem_bank command (see Section 8.1.1.8) determines whether to read from the display RAM or general-purpose RAM. After reading, the address counter automatically increments or decrements by 1 in accordance with the setting of bit I_D of the Entry_mode_set command (see Section 8.1.2.1).

Only bit 4 to bit 0 of the display RAM or the general-purpose RAM 2 data are valid. Bit 7 to bit 5 are set logic 0.

#### 8.1.1.11 Command: Write_data

The Write_data command writes binary 8-bit data to the display RAM or general-purpose RAM.

**Table 16. Write_data - data write bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 01 | fixed value |
| **General-purpose RAM 1** | | | |
| 7 to 0 | WD[7:0] | 00000000 to 11111111 | **write data to general-purpose RAM 1** |
| **display RAM bank 1 to 3, general-purpose RAM 2** | | | |
| 7 to 5 | - | 000 | not implemented |
| 4 to 0 | WD[4:0] | 00000 to 11111 | **write data to the display RAM bank 1 to 3 and general-purpose RAM 2** |

The Sel_mem_bank command (see Section 8.1.1.8) determines whether to write data into the display RAM or general-purpose RAM. After writing, the address counter automatically increments or decrements by 1 in accordance with the setting of bit I_D of the Entry_mode_set command (see Section 8.1.2.1).

Only bit 4 to bit 0 of the display RAM or the general-purpose RAM 2 data are valid. Bit 7 to bit 5 are not implemented and should always be logic 0.

### 8.1.2 Display control commands

#### 8.1.2.1 Command: Entry_mode_set

The Entry_mode_set command sets the address stepping.

**Table 17. Entry_mode_set - entry mode bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 10 | fixed value |
| 7 to 2 | - | 001010 | fixed value |
| 1 | I_D | | **address stepping select** |
| | | 0 | display RAM or general-purpose RAM address decrements by 1 |
| | | 1[1] | display RAM or general-purpose RAM address increments by 1 |
| 0 | - | -[2] | not implemented |

[1] Default value.

[2] Not implemented, have to be always written with 0.

**Bit I_D:** When bit I_D = 1, the display RAM or general-purpose RAM address increments by 1 when data is written into or read from the display RAM or general-purpose RAM.

When bit I_D = 0 the display RAM or general-purpose RAM address decrements by 1 when data is written into or read from the display RAM or general-purpose RAM.

#### 8.1.2.2 Command: Inversion_mode

The Inversion_mode command allows changing the drive scheme inversion mode.

The waveforms used to drive an LCD (see Figure 24 and Figure 25) inherently produce a DC voltage across the display cell. The PCA8539 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of the compensation method is determined with INV[2:0] in Table 18.

**Table 18. Inversion_mode - inversion mode command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 10 | fixed value |
| 7 to 3 | - | 01000 | fixed value |
| 2 to 0 | INV[2:0] | | **inversion mode setting** |
| | | 000[1] | frame inversion mode |
| | | 001 | 1-line inversion mode |
| | | 010 | 2-line inversion mode |
| | | 011 | 3-line inversion mode |
| | | 100 | 4-line inversion mode |
| | | 101 | 5-line inversion mode |
| | | 110 | 6-line inversion mode |
| | | 111 | 7-line inversion mode |

[1] Default value.

**Line inversion mode (driving scheme A):** In line inversion mode, the DC value is compensated every $n^{th}$ line. Changing the inversion mode to line inversion mode reduces the possibility for flickering but increases the power consumption.

**Frame inversion mode (driving scheme B):** In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is the possibility for flicker to occur.

#### 8.1.2.3 Command: Frame_frequency

With this command, the clock and frame frequency can be programmed when using the internal clock.

**Table 19. Frame-frequency - frame frequency select command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 10 | fixed value |
| 7 to 5 | - | 100 | fixed value |
| 4 to 0 | FF[4:0] | see Table 20 | **frame frequency setting** |

The duty cycle depends on the frequency chosen (see Table 20).

The Frame_frequency command allows configuring the frame frequency and the clock frequency. The default frame frequency of 80 Hz is factory calibrated.

**Table 20. Clock and frame frequency values**

*Duty cycle definition: % HIGH-level time : % LOW-level time.*

| FF[4:0] | Frame frequency (Hz) | Clock frequency (Hz) | Typical duty cycle (%) |
|---|---|---|---|
| 00000 | 45 | 36000 | 50 : 50 |
| 00001 | 50 | 39724 | 44 : 56 |
| 00010 | 55 | 44308 | 38 : 62 |
| 00011 | 60 | 48000 | 33 : 67 |
| 00100 | 65 | 52364 | 27 : 73 |
| 00101 | 70 | 54857 | 23 : 77 |
| 00110 | 75 | 60632 | 15 : 85 |
| 00111[1] | 80 | 64000 | 11 : 89 |
| 01000 | 85 | 67765 | 5 : 95 |
| 01001 | 90 | 72000 | 50 : 50 |
| 01010 | 95 | 76800 | 46 : 54 |
| 01011 | 100 | 82286 | 42 : 58 |
| 01100 | 110 | 88615 | 38 : 62 |
| 01101 | 120 | 96000 | 33 : 67 |
| 01110 | 130 | 104727 | 27 : 73 |
| 01111 | 145 | 115200 | 20 : 80 |
| 10000 | 160 | 128000 | 11 : 89 |
| 10001 | 180 | 144000 | 50 : 50 |
| 10010 | 210 | 164571 | 42 : 58 |
| 10011 | 240 | 192000 | 33 : 67 |
| 10100 | 290 | 230400 | 20 : 80 |
| 10101 to 11111 | 360 | 288000 | 50 : 50 |

[1] Default value.

### 8.1.2.4 Command: Display_control

With the Display_control command, the display can be switched on or off.

**Table 21. Display_control - Display control bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 10 | fixed value |
| 7 to 3 | - | 00100 | fixed value |
| 2 | D | | **display setting** |
| | | 0[1] | display is off |
| | | 1 | display is on |
| 1, 0 | - | - -[2] | not implemented |

[1] Default value.

[2] Not implemented, have to be always written with 0.

#### 8.1.2.5 Command: Display_config

The Display_config command allows setting how the data is displayed.

**Table 22. Display_config - display configuration bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 10 | fixed value |
| 7 to 2 | - | 000001 | fixed value |
| 1 | P | | **display segment setting** |
| | | 0[1] | segment data: left to right;<br>segment data is displayed from segment 0 to segment 99 |
| | | 1 | segment data: right to left;<br>segment data is displayed from segment 99 to segment 0 |
| 0 | - | -[2] | fixed value |

[1] Default value.

[2] Not implemented, have to be always written with 0.

**Bit P:** The P bit is used to flip the display left to right by mirroring the segment data.

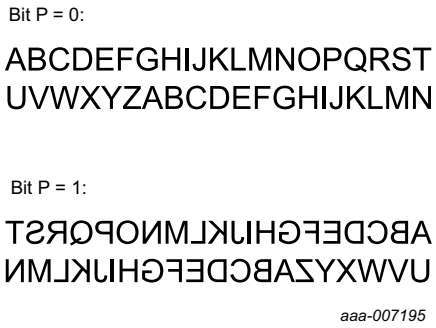



**Fig 3. Illustration of the display configuration bit P**

### 8.1.3 Charge pump and LCD bias control commands

#### 8.1.3.1 Command: Charge_pump_ctrl

The Charge_pump_ctrl command enables or disables the internal $V_{LCD}$ generation and controls the charge pump voltage multiplier setting.

**Table 23. Charge_pump_ctrl - charge pump control command bit description**

| Bit | Symbol | Binary value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 11 | fixed value |
| 7 to 3 | - | 10000 | fixed value |
| 2 | CPE | | **charge pump setting** |
| | | 0[1] | charge pump disabled; no internal $V_{LCD}$ generation; external supply of $V_{LCD}$ |
| | | 1 | charge pump enabled |
| 1 to 0 | CPC[2:0] | | **charge pump voltage multiplier setting** |
| | | 00[1] | $V_{LCD} = 2 \times V_{DD2}$ |
| | | 01 | $V_{LCD} = 3 \times V_{DD2}$ |
| | | 10 | $V_{LCD} = 4 \times V_{DD2}$ |
| | | 11 | $V_{LCD} = V_{DD2}$ (direct mode) |

[1] Default value.

#### 8.1.3.2 Command: Set_VLCD

The Set_VLCD command allows programming the $V_{LCD}$ value. The generated $V_{LCD}$ is independent of the power supply, allowing battery operation of the PCA8539.

**Table 24. Set_VLCD - Set-$V_{LCD}$ command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| **The 5 MSB of VLCD** | | | |
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 11 | fixed value |
| 7 to 5 | - | 101 | fixed value |
| 4 to 0 | VLCD[8:4] | 00000[1] to 11111 | **$V_{LCD}$ value** |
| **The 4 LSB of VLCD** | | | |
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 11 | fixed value |
| 7 to 4 | - | 1001 | fixed value |
| 3 to 0 | VLCD[3:0] | 0000[1] to 1111 | **$V_{LCD}$ value** |

[1] Default value.

### 8.1.4 Temperature compensation control commands

#### 8.1.4.1 Command: Temperature_ctrl

The Temperature_ctrl command enables or disables the temperature measurement block and the temperature compensation of $V_{LCD}$ (see Section 8.4.5).

**Table 25. Temperature_ctrl - temperature measurement control command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 11 | fixed value |
| 7 to 3 | - | 00000 | fixed value |
| 2 | TCE | | **temperature compensation setting** |
| | | 0[1] | temperature compensation of $V_{LCD}$ disabled |
| | | 1 | temperature compensation of $V_{LCD}$ enabled |
| 1 | TMF | | **temperature measurement filter** setting |
| | | 0[1] | digital temperature filter disabled[2] |
| | | 1 | digital temperature filter enabled |
| 0 | TME | | **temperature measurement setting** |
| | | 0[1] | temperature measurement disabled; no temperature readout possible |
| | | 1 | temperature measurement enabled; temperature readout possible |

[1] Default value.

[2] The unfiltered digital value of TD[7:0] is immediately available for the readout and $V_{LCD}$ compensation.

#### 8.1.4.2 Command: TC_slope

The TC_slope command allows setting the temperature coefficients of $V_{LCD}$ corresponding to 4 temperature intervals.

**Table 26. TC_slope - $V_{LCD}$ temperature compensation slope command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| - | R/$\overline{W}$ | 0 | fixed value |
| - | RS[1:0] | 11 | fixed value |
| **TC-slope-A** | | | |
| 7 to 3 | - | 00001 | fixed value |
| 2 to 0 | TSA[2:0] | 000[1] to 111 | **temperature factor A setting**[2] |
| **TC-slope-B** | | | |
| 7 to 3 | - | 00010 | fixed value |
| 2 to 0 | TSB[2:0] | 000[1] to 111 | **temperature factor B setting**[2] |
| **TC-slope-C** | | | |
| 7 to 3 | - | 00011 | fixed value |
| 2 to 0 | TSC[2:0] | 000[1] to 111 | **temperature factor C setting**[2] |
| **TC-slope-D** | | | |
| 7 to 3 | - | 00100 | fixed value |
| 2 to 0 | TSD[2:0] | 000[1] to 111 | **temperature factor D setting**[2] |

[1] Default value.

[2] See Table 28 on page 37.

## 8.2 Start-up and shut-down

### 8.2.1 Initialization

The first command sent to the device after power-on or a reset by using the $\overline{RST}$ pin must be the Initialize command (see Section 8.1.1.1 on page 9).

The Initialize command resets the PCA8539 to the following starting conditions:

1. All backplane and segment driver outputs are set to $V_{SS1}$.
2. Selected drive mode is 1:18 multiplex driving mode.
3. The address counter is cleared (set logic 0).
4. Temperature measurement is disabled.
5. Temperature filter is disabled.
6. The internal $V_{LCD}$ voltage generation is disabled. The charge pump is switched off.
7. The $V_{LCD}$ temperature compensation is disabled.
8. The display is disabled.

The reset state is as shown in Table 27. A code example of the initialization is given in Section 19.1.

**Table 27. Reset state of PCA8539**

| Command name | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **General control commands** | | | | | | | | |
| Clock_out_ctrl | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Read_reg_select | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Graphic_mode_cfg | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Sel_mem_bank | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Set_mem_addr | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Display control commands** | | | | | | | | |
| Entry_mode_set | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| Inversion_mode | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Frame_frequency | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Display_control | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Display_config | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| **Charge pump and LCD bias control commands** | | | | | | | | |
| Charge_pump_ctrl | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Set_VLCD | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| **Temperature compensation control commands** | | | | | | | | |
| Temperature_ctrl | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TC_slope | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Remarks:**

1. Do not transfer data for at least 1 ms after a power-on.
2. After power-on and before enabling the display, the display RAM content must be brought to a defined status by writing meaningful display content (for example, a graphic) otherwise unwanted display artifacts may appear on the display.

### 8.2.2 Reset pin function

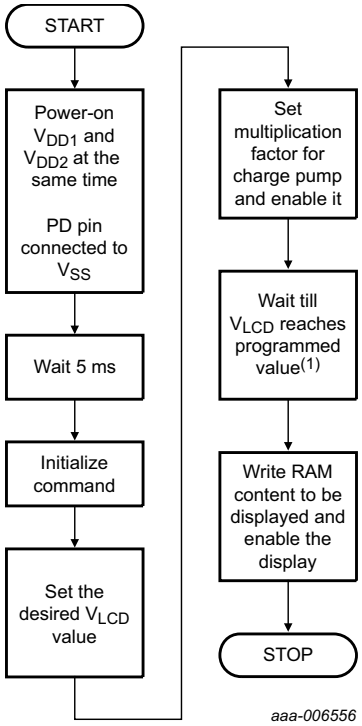
The reset pin ($\overline{RST}$) of the PCA8539 resets all the registers to their default state. The reset state is given in Table 27. The RAM contents remain unchanged. After the reset signal is released, the Initialize command must be sent to complete the initialization of the chip.

### 8.2.3 Power-down pin function

When connected to $V_{DD1}$, the internal circuits are switched off, leaving only 2 μA (typical) as an overall current consumption. When connected to $V_{SS1}$, the PCA8539 runs or starts up to normal mode again. For the start-up and power-down sequences, see Section 8.2.4 and Section 8.2.5.

### 8.2.4 Recommended start-up sequences

This section describes how to proceed with the initialization of the chip in different application modes.




(1) The QPR flag (see Table 11) indicates if the programmed LCD voltage value was reached. The latency time depends on the external capacitor on the $V_{LCD}$ pins. For a capacitor of 100 nF a delay of 50 ms to 60 ms is expected.

**Fig 4. Recommended start-up sequence when using the internal charge pump and the internal clock signal**

When using the internal $V_{LCD}$ generation, the display must not be enabled before the generation of $V_{LCD}$ with the internal charge pump is completed. Otherwise unwanted display artifacts may appear on the display.

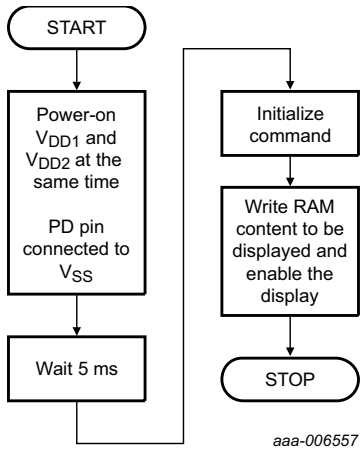
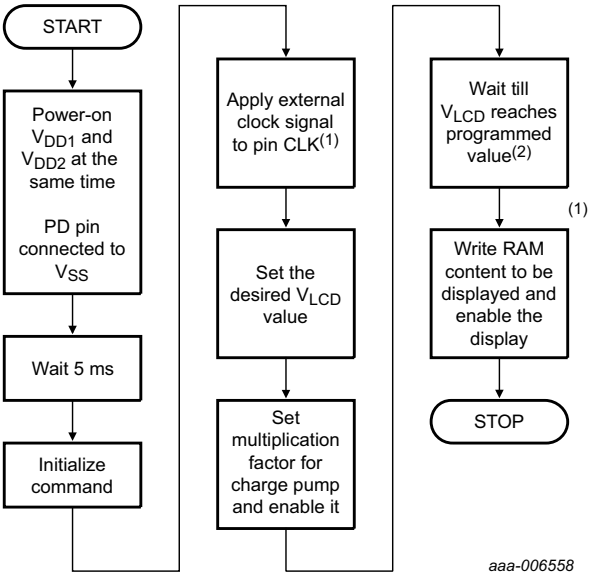



**Fig 5. Recommended start-up sequence when using an externally supplied $V_{LCD}$ and the internal clock signal**




(1) Alternatively, the external clock signal can be applied after the generation of the $V_{LCD}$ voltage.

(2) The QPR flag (see Table 11) indicates if the programmed LCD voltage value was reached. The latency time depends on the external capacitor on the $V_{LCD}$ pins. For a capacitor of 100 nF a delay of 50 ms to 60 ms is expected.

**Fig 6. Recommended start-up sequence when using the internal charge pump and an external clock signal**

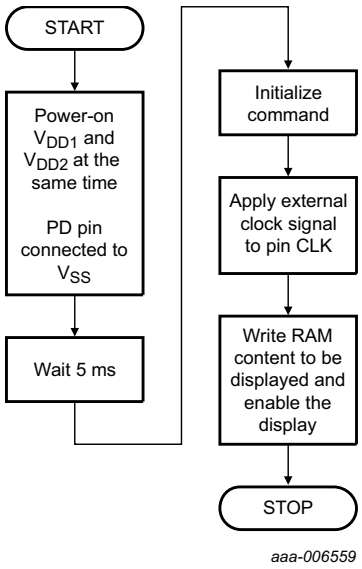



**Fig 7. Recommended start-up sequence when using an externally supplied $V_{LCD}$ and an external clock signal**

### 8.2.5 Recommended power-down sequences

With the following sequences, the PCA8539 can be set to a state of minimum power consumption, called power-down mode.