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PCA8546

4 x 44 automotive LCD driver

Rev. 1 — 13 November 2013 **Product data sheet**

1. General description

The PCA8546 is a peripheral device which generates the drive signals for any multiplexed LCD containing up to four backplanes, and up to 176 elements. The PCA8546 is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus (PCA8546A) or a three line unidirectional SPI-bus (PCA8546B). Communication overheads are minimized using a display RAM with auto-incremented addressing.

For a selection of NXP LCD segment drivers, see .

2. Features and benefits

- AEC-Q100 grade 3 compliant for automotive applications
- Single-chip 176 elements LCD controller and driver
- Wide range for digital power supply: from 1.8 V to 5.5 V
- LCD supply range from 2.5 V up to 9 V
- LCD and logic supplies may be separated
- Low power consumption
- Four backplanes and selectable display bias configuration
- On-chip RAM for display data storage
- 400 kHz I^2C-bus interface (PCA8546A)
- 5 MHz SPI-bus interface (PCA8546B)
- Programmable frame frequency in the range of 60 Hz to 300 Hz in steps of about 10 Hz; factory calibrated
- 176 segments driven allowing:
    - ◆ up to 22 7-segment alphanumeric characters
    - ◆ up to 11 14-segment alphanumeric characters
    - ◆ any graphics of up to 176 elements
- Manufactured in silicon gate CMOS process
- Extended operating temperature range up to 95 °C

3. Applications

- Climate control
- Car radio
- Dashboard display

4. Ordering information

Table 1.   Ordering information

Type number	Interface type	Package		
		Name	**Description**	**Version**
PCA8546ATT	I^{2}C-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCA8546BTT	SPI-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4.1 Ordering options

Table 2.   Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA8546ATT/A	935302989118	PCA8546ATT/AJ	1	tape and reel, 13 inch
PCA8546BTT/A	935302991118	PCA8546BTT/AJ	1	tape and reel, 13 inch

5. Marking

Table 3.   Marking codes

Type number	Marking code
PCA8546ATT/A	PCA8546ATT
PCA8546BTT/A	PCA8546BTT

6. Block diagram

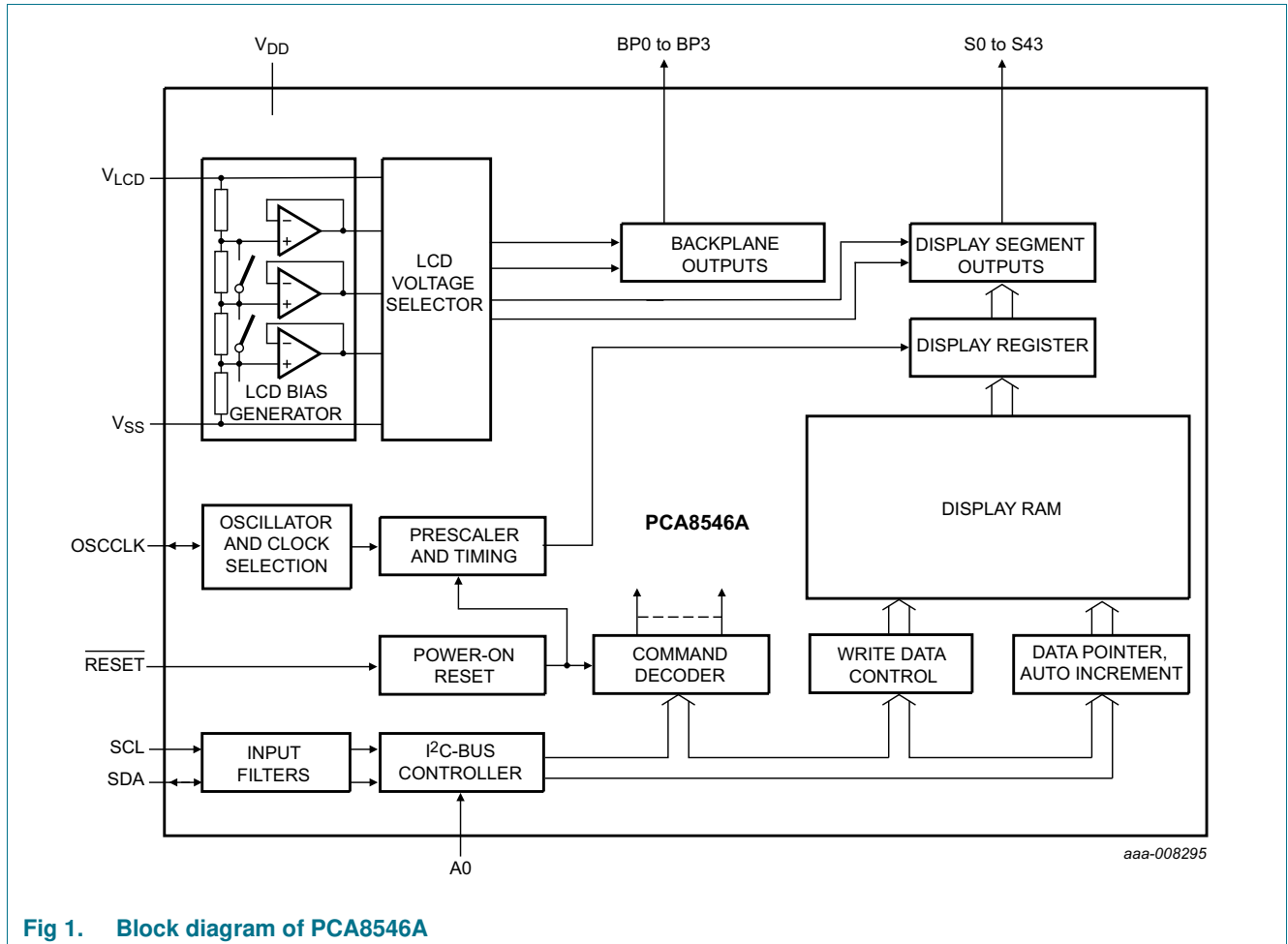**Fig 1.**   **Block diagram of PCA8546A**

Fig 2.   **Block diagram of PCA8546B**
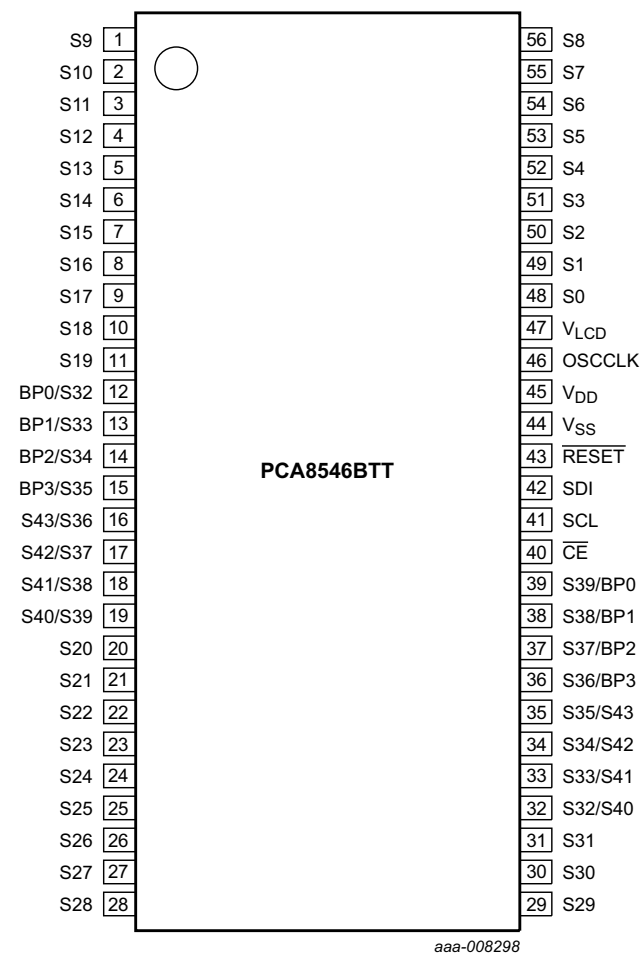
PCA8546

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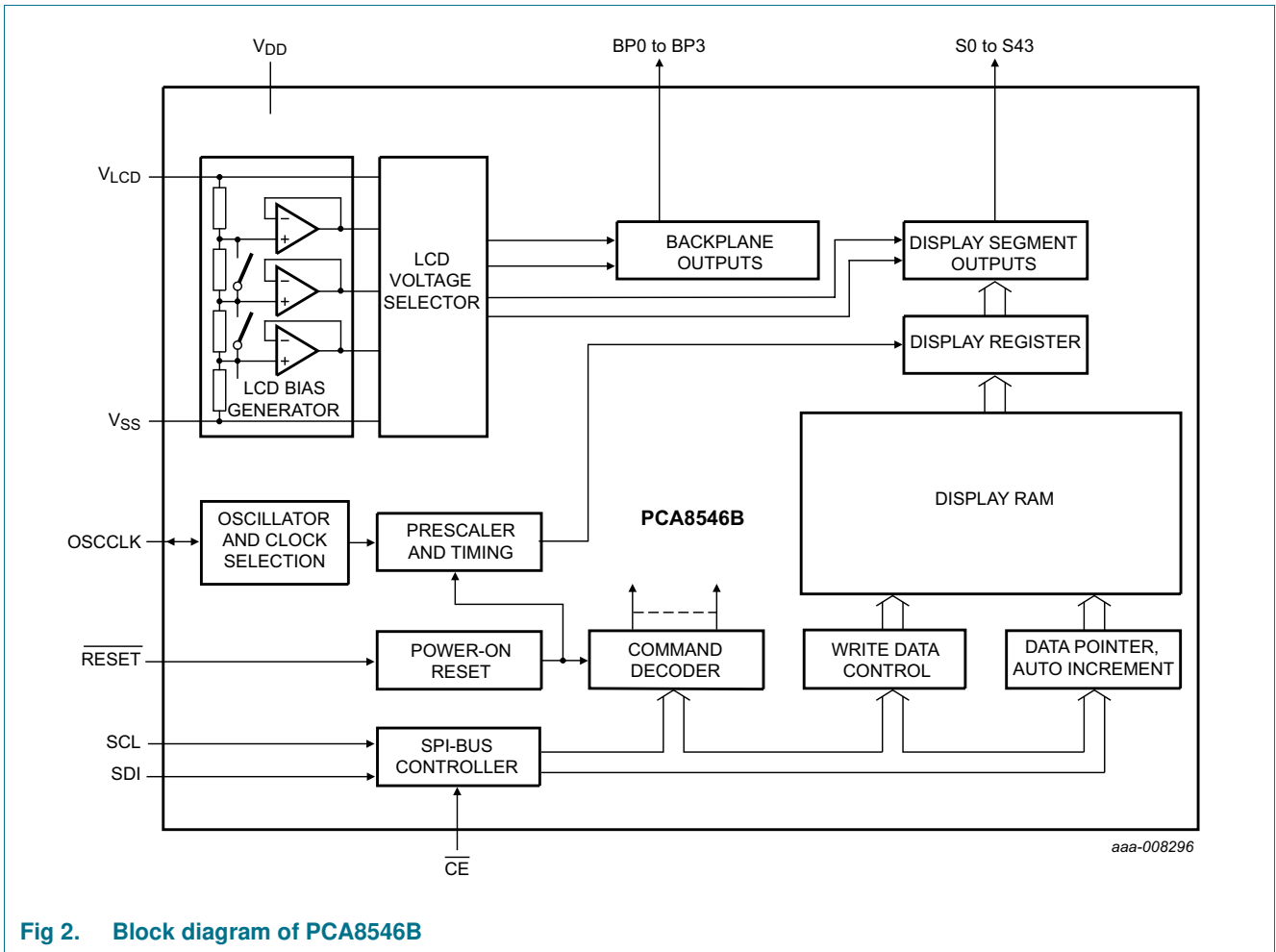
7. Pinning information

7.1 Pinning

PCA8546ATT

Pin	Left	Pin	Right
1	S9	56	S8
2	S10	55	S7
3	S11	54	S6
4	S12	53	S5
5	S13	52	S4
6	S14	51	S3
7	S15	50	S2
8	S16	49	S1
9	S17	48	S0
10	S18	47	V_{LCD}
11	S19	46	OSCCLK
12	BP0/S32	45	V_{DD}
13	BP1/S33	44	V_{SS}
14	BP2/S34	43	$\overline{RESET}$
15	BP3/S35	42	SDA
16	S43/S36	41	SCL
17	S42/S37	40	A0
18	S41/S38	39	S39/BP0
19	S40/S39	38	S38/BP1
20	S20	37	S37/BP2
21	S21	36	S36/BP3
22	S22	35	S35/S43
23	S23	34	S34/S42
24	S24	33	S33/S41
25	S25	32	S32/S40
26	S26	31	S31
27	S27	30	S30
28	S28	29	S29

aaa-008297

Top view. For mechanical details, see Figure 39.

Fig 3.   Pin configuration for TSSOP56 (PCA8546ATT)

PCA8546BTT

Pin	Left	Pin	Right
1	S9	56	S8
2	S10	55	S7
3	S11	54	S6
4	S12	53	S5
5	S13	52	S4
6	S14	51	S3
7	S15	50	S2
8	S16	49	S1
9	S17	48	S0
10	S18	47	V_{LCD}
11	S19	46	OSCCLK
12	BP0/S32	45	V_{DD}
13	BP1/S33	44	V_{SS}
14	BP2/S34	43	$\overline{RESET}$
15	BP3/S35	42	SDI
16	S43/S36	41	SCL
17	S42/S37	40	$\overline{CE}$
18	S41/S38	39	S39/BP0
19	S40/S39	38	S38/BP1
20	S20	37	S37/BP2
21	S21	36	S36/BP3
22	S22	35	S35/S43
23	S23	34	S34/S42
24	S24	33	S33/S41
25	S25	32	S32/S40
26	S26	31	S31
27	S27	30	S30
28	S28	29	S29

aaa-008298

Top view. For mechanical details, see Figure 39.

Fig 4.   Pin configuration for TSSOP56 (PCA8546BTT)

7.2 Pin description

Table 4.   Pin description of PCA8546ATT and PCA8546BTT
Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Pin	Symbol	Type	Description
1 to 11	S9 to S19	output	LCD segment
20 to 31	S20 to S31	output	LCD segment
43	$\overline{RESET}$	input	active LOW reset input
44	V_{SS}	supply	ground supply voltage
45	V_{DD}	supply	supply voltage
46	OSCCLK	input/output	external clock input/internal oscillator output
47	V_{LCD}[1]	supply	LCD supply voltage
48 to 56	S0 to S8	output	LCD segment

Pin layout depending on backplane swap configuration[2]

	BPS = 0[3]	BPS = 1		
12	BP0	S32	output	LCD backplane/LCD segment
13	BP1	S33		
14	BP2	S34		
15	BP3	S35		
16	S43	S36		
17	S42	S37		
18	S41	S38		
19	S40	S39		
32	S32	S40		
33	S33	S41		
34	S34	S42		
35	S35	S43		
36	S36	BP3		
37	S37	BP2		
38	S38	BP1		
39	S39	BP0		

Pin layout depending on product and bus type

	PCA8546ATT	PCA8546BTT	Type	Description
40	A0		input	I²C-bus slave address selection
		$\overline{CE}$	input	SPI-bus chip enable - active LOW
41	SCL		input	I²C-bus serial clock
		SCL	input	SPI-bus serial clock
42	SDA		input/output	I²C-bus serial data
		SDI	input	SPI-bus data input

[1] V_{LCD} must be equal to or greater than V_{DD}.

[2]   Effect of backplane swapping is illustrated in Figure 5 on page 9.

[3]   Bit BPS is explained in Section 8.1.3 on page 8.

8. Functional description

The PCA8546 is a versatile peripheral device designed to interface any microcontroller to a wide variety of LCDs. It can directly drive any multiplexed LCD containing four backplanes and up to 44 segments.

8.1 Commands of PCA8546

The PCA8546 is controlled by 8 commands, which are defined in Table 5. Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCA8546.

Table 5.   Commands of PCA8546

Command name	Register selection RS[1:0][1]		Bits								Reference
			7	6	5	4	3	2	1	0	
initialize											Section 8.1.1
initialize-MSB	0	0	0	0	0	1	0	1	1	0	
initialize-LSB	0	0	0	0	0	0	0	0	1	1	
OTP-refresh	0	0	1	1	1	1	0	0	0	0	Section 8.1.2
mode-settings	0	0	0	1	0	1	BPS	INV	PD	E	Section 8.1.3
oscillator-control	0	0	0	0	0	1	1	EFR	COE	OSC	Section 8.1.4
set-bias-mode	0	0	0	0	0	0	0	1	B[1:0]		Section 8.1.5
frame-frequency	0	0	0	0	1	FD[4:0]					Section 8.1.6
load-data-pointer	0	0	1	0	DP[5:0]						Section 8.1.7
write-RAM-data	0	1	D[7:0]								Section 8.1.8

[1]   Information about control byte and register selection see Section 9.1 on page 29.

8.1.1 Command: initialize

This command generates a chip-wide reset. It consists of two bytes which have to be sent both to the device.

Table 6.   Initialize - initialize command bit description

Bit	Symbol	Value	Description
Initialize-MSB			
7 to 0	-	00010110	fixed value
Initialize-LSB			
7 to 0	-	00000011	fixed value

8.1.2 Command: OTP-refresh

During production of the device, each IC is calibrated to achieve the specified accuracy of the frame frequency. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. The device reads these cells every time the OTP-refresh command is sent. The OTP-refresh command has to be sent after a reset has been made and before the display is enabled.

This command will be completed after a maximum of 30 ms and requires either the internal or external clock to run. If the internal oscillator is not used, then a clock must be supplied to the OSCCLK pin. If the OTP-refresh instruction is sent and no clock is present, then the request is stored until a clock is available.

Remark: It is recommended not to enter power-down mode during the OTP refresh cycle.

Table 7.   OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
7 to 0	-	1111 0000	fixed value

8.1.3 Command: mode-settings

Table 8.   Mode-settings - mode settings command bit description

Bit	Symbol	Value	Description
7 to 4	-	0101	fixed value
3	BPS		**backplane swapping**
		0[1]	backplane configuration 0
		1	backplane configuration 1
2	INV		**set inversion mode**
		0[1][2]	Driving scheme A: LCD line inversion mode
		1	Driving scheme B: LCD frame inversion mode
1	PD		**set power mode**
		1	power-down mode; backplane and segment outputs are connected to V_{SS} and the internal oscillator is switched off
		0[1]	power-up mode
0	E		**display switch**
		0[1]	display disabled; backplane and segment outputs are connected to V_{SS}
		1	display enabled

[1]   Default value.

[2]   See Section 8.1.3.2.

8.1.3.1 Backplane swapping

Backplane swapping can be configured with the BPS bit (see Table 8). It moves the location of the backplane and the associated segment outputs from one side of the PCA8546 to the other. Backplane swapping is sometimes desirable to aid with the routing of PCBs that do not use multiple layers.

The BPS bit has to be set to the required value before enabling the display. Failure to do so does not damage the PCA8546 or the display, however unexpected display content may appear.

BPS = 0

BPS = 1

aaa-008299

Fig 5.   Effect of backplane swapping

8.1.3.2 Line inversion (driving scheme A) and frame inversion (driving scheme B)

The DC offset of the voltage across the LCD is compensated over a certain period: line-wise in line inversion mode (driving scheme A) or frame-wise in frame inversion mode (driving scheme B). With the INV bit (see Table 8), the compensation mode can be switched.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption; therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined; however, since the switching frequency is reduced, there is possibility for flicker to occur.

The waveforms of Figure 14 shows the line inversion mode. Figure 15 shows the frame inversion mode.

8.1.3.3 Power-down mode

The power-down bit (PD) allows the PCA8546 to be put in a minimum power configuration. To avoid display artifacts, enter power-down only after the display has been switched off by setting bit E to logic 0. During power-down, the internal oscillator is switched off.

Table 9.   Effect of the power-down bit (PD)

Effect on function	Mode settings	Effect of setting PD	
		0	**1**
backplane output	E = 1	normal function	V_{SS}
segment output	E = 1	normal function	V_{SS}
internal oscillator	OSC = 0, COE = 1	on	off
OSCCLK pin	OSC = 0, COE = 1	output of internal oscillator frequency	V_{DD}
OSCCLK pin	OSC = 1	input clock	clock input, can be logic 0, logic 1, or left floating

With the following sequence, the PCA8546 can be set to a state of minimum power consumption, called power-down mode.

013aaa447
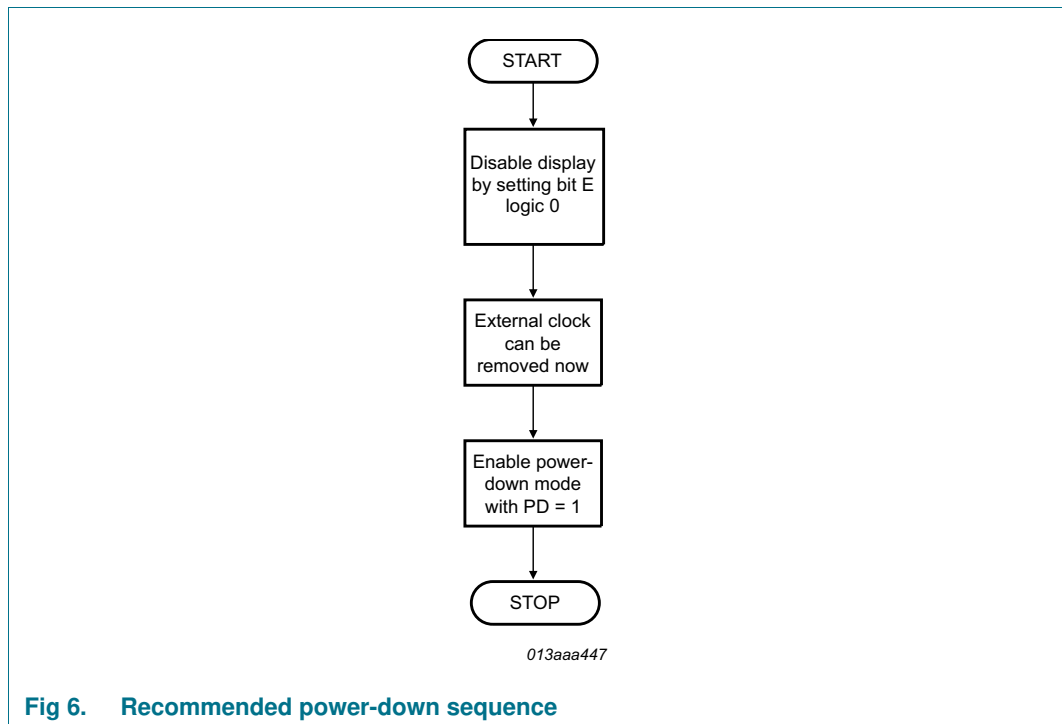
Fig 6.   Recommended power-down sequence

Remarks:

• It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (see Section 10). Otherwise it may cause unwanted display artifacts. If an uncontrolled removal of the supply happens, the PCA8546 does not get damaged.

• Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage is off, or the other way around. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

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- A clock signal must always be supplied to the device when the display is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. First disable the display and afterwards remove the clock signal.

8.1.3.4 Display enable

The display enable bit (E) is used to enable and disable the display. When the display is disabled, all LCD outputs go to V_{SS}. This function is implemented to ensure that no voltage can be induced on the LCD outputs as it may lead to unwanted displays of segments.

Recommended start-up sequences are found in Section 8.2.3

Remark: Display enable is not synchronized to an LCD frame boundary. Therefore using this function to flash a display for prolonged periods is not recommended due to the possible build-up of DC voltages on the display.

8.1.4 Command: oscillator-control

The oscillator-control command switches between internal and external oscillator and enables or disables the pin OSCCLK. It is also defines the external frequency.

Table 10. Oscillator-control - oscillator control command bit description

Bit	Symbol	Value	Description
7 to 3	-	00011	fixed value
2	EFR		**external clock frequency** applied on pin OSCCLK
		0[1]	9.6 kHz
		1	230 kHz
1	COE		**clock output enable for pin OSCCLK**
		0[1]	clock signal not available on pin OSCCLK; pin OSCCLK is in 3-state
		1	clock signal available on pin OSCCLK
0	OSC		**oscillator source**
		0[1]	internal oscillator running
		1	external oscillator used; pin OSCCLK becomes an input; used in combination with EFR to determine input frequency

[1] Default value.

The bits OSC, COE, and EFR control the source and frequency of the clock used to generate the LCD signals (see Figure 7). Valid combinations are shown in Table 11.

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(1)   Can only be used with the internal oscillator (OSC = 0).

(2)   Can only be used with an external oscillator (OSC = 1).

(3)   Nominal value for divide factor q is 24; source clock is 230 kHz (see Section 8.1.6).

Fig 7.   Oscillator selection

Table 11.   Valid combinations of bits OSC, EFR, and COE

OSC	COE	EFR	OSCCLK pin	Clock source
0	0	not used	inactive; may be left floating	internal oscillator used
0	1	not used	output of internal oscillator frequency (prescaler)	internal oscillator used
1	not used	0	9.6 kHz input	OSCCLK pin
1	not used	1	230 kHz input	OSCCLK pin

Table 12.   Typical use of bits OSC, EFR, and COE

Usage	OSC	COE	EFR
LCD with internal oscillator	0	0	not used
LCD with external oscillator (230 kHz)	1	not used	1
LCD with external oscillator (9.6 kHz)	1	not used	0

8.1.4.1   Oscillator

The system is designed to operate from a 9.6 kHz or a 230 kHz clock. This clock can be sourced internally or externally. The internal logic and LCD drive signals of the PCA8546 are timed either by the internal oscillator or from the clock externally supplied.

Internal clock: When the internal oscillator is used, all LCD signals are generated from it. The oscillator runs at nominal 230 kHz. The relationship between this frequency and the LCD frame frequency is detailed in Section 8.1.6. Control over the internal oscillator is made with the OSC bit (see Section 8.1.4).

It is possible to make the internal oscillator signal available on pin OSCCLK by using the oscillator-control command (see Table 10) and configuring the clock output enable (COE) bit. If not required, the pin OSCCLK should be left open or connected to V_{SS}. At power-on the signal at pin OSCCLK is disabled and pin OSCCLK is in 3-state.

Clock output is only valid when using the internal oscillator. The signal appears on the OSCCLK pin.

An intermediate clock frequency is available at the OSCCLK pin. The duty cycle of this clock varies with the chosen divide ratio.

Table 13. OSCCLK pin state depending on configuration

PD	OSC	COE	EFR	OSCCLK pin[1]
power-down	n.a.	off	n.a.	3-state[2]
power-down	n.a.	on	n.a.	V_{DD}
power-up	internal oscillator	off	n.a.	3-state
		on	n.a.	9.6 kHz output[3]
	external oscillator	n.a.	9.6 kHz	9.6 kHz input
			230 kHz	230 kHz input

[1] When $\overline{RESET}$ is active, the pin OSCCLK is in 3-state.

[2] In this state, an external clock may be applied, but it is not a requirement.

[3] 9.6 kHz is the nominal frequency with q = 24, see Table 14.

External clock: In applications where an external clock must be applied to the PCA8546, bit OSC (see Table 10) has to be set logic 1. In this case pin OSCCLK becomes an input.

The OSCCLK signal must switch between the V_{SS} and the V_{DD} voltage supplied to the chip.

The EFR bit determines the external clock frequency (230 kHz or 9.6 kHz). The clock frequency ($f_{clk(ext)}$) in turn determines the LCD frame frequency, see Table 14.

Remark: If an external clock is used, then this clock signal must always be supplied to the device when the display is on. Removing the clock may freeze the LCD in a DC state which damages the LCD material.

8.1.4.2 Timing and frame frequency

The timing of the PCA8546 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 14). The frame frequency is a fixed division of the internal clock or of the frequency applied to pin OSCCLK when an external clock is used.

Table 14. LCD frame frequencies

Frame frequency	Typical external frequency (Hz)	Nominal frame frequency (Hz)	EFR bit	Value of q[1]
$f_{fr(LCD)} = \dfrac{f_{clk(ext)}}{48}$	9600	200	0	-
$f_{fr(LCD)} = \dfrac{f_{clk(ext)}}{48 \cdot q}$	230000	200	1	24

[1] Other values of the frame frequency prescaler see Table 17.

When the internal clock is used, or an external clock with EFR = 1, the LCD frame frequency can be programmed by software in steps of approximately 10 Hz in the range of 60 Hz to 300 Hz (see Table 17). Furthermore the internal oscillator is factory calibrated, see Table 32 on page 42.

8.1.5 Command: set-bias-mode

The set-bias-mode command allows setting the bias level.

Table 15.   Set-bias-mode - set bias mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	000001	fixed value
1 to 0	B[1:0]	00[1]. 01	¼ bias
		11	⅓ bias
		10	½ bias

[1]   Default value.

8.1.6 Command: frame-frequency

With the frame-frequency command, the frame frequency for the display can be
configured. The clock frequency determines the frame frequency.

**Table 16.   Frame-frequency - frame frequency and output clock frequency command bit
description**

Bit	Symbol	Value	Description
7 to 5	-	001	fixed value
4 to 0	FD[4:0]	see Table 17	frequency prescaler

When using an **external clock** it can be either a 230 kHz or a 9.6 kHz clock signal. The
EFR bit (see Table 10) has to be set according to the external clock frequency.

When EFR is set to 9.6 kHz, then the LCD frame frequency is calculated with Equation 1:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48} \tag{1}$$

When EFR is set to 230 kHz, then the LCD frame frequency is calculated with Equation 2:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48 \cdot q} \tag{2}$$

where q is the frequency divide factor (see Table 17).

Remark: $f_{clk(ext)}$ is the external input clock frequency to pin OSCCLK.

When the **internal oscillator** is used, the intermediate frequency may be output on the
OSCCLK pin. Its frequency is given in Table 17.

Table 17.   Frame frequency prescaler values for 230 kHz clock operation

FD[4:0]	Nominal LCD frame frequency (Hz)[1]	Divide factor, q	Intermediate clock frequency (Hz)
00000	59.9	80	2875
00001	70.5	68	3382
00010	79.9	60	3833
00011	90.4	53	4340
00100	99.8	48	4792
00101	108.9	44	5227
00110	119.8	40	5750
00111	129.5	37	6216

Table 17.   Frame frequency prescaler values for 230 kHz clock operation *...continued*

FD[4:0]	Nominal LCD frame frequency (Hz)[1]	Divide factor, q	Intermediate clock frequency (Hz)
01000	140.9	34	6765
01001	149.7	32	7188
01010	159.7	30	7667
01011	171.1	28	8214
01100	177.5	27	8519
01101	191.7	25	9200
01110[2]	199.7	24	9583
01111	208.3	23	10000
10000	217.8	22	10455
10001	228.3	21	10952
10010	239.6	20	11500
10011	252.2	19	12105
10100	266.2	18	12778
10101	281.9	17	13529
10110	299.5	16	14375
10111 to 11111	not used		

[1]   Nominal frame frequency calculated for the default clock frequency of 230 kHz.

[2]   Default value.

8.1.7 Command: load-data-pointer

The load-data-pointer command defines the start address of the display RAM, see
Table 18. The data pointer is auto incremented after each RAM write.

Table 18.   Load-data-pointer - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 6	-	10	fixed value
5 to 0	DP[5:0]	000000[1] to 101011	6-bit binary value of 0 to 43

[1]   Default value.

Remark: Data pointer values outside of the valid range are ignored and no RAM content
is transferred until a valid data pointer value is set.

Filling of the display RAM is described in Section 8.9.

8.1.8 Command: write-RAM-data

This command initiates the transfer of data to the display RAM. Data is written into the
address defined by the load-data-pointer command. RAM filling is described in
Section 8.9.

Table 19.   Write-RAM-data - write RAM data command bit description
For this command to be effective bit RS[1:0] of the control byte has to be set logic 01, see Table 23 on page 29.

Bit	Symbol	Value	Description
7 to 0	D[7:0]	0000 0000 to 1111 1111	writing data byte-wise to RAM

8.2 Start-up and shut-down

8.2.1 Reset and Power-On Reset (POR)

After power-on the PCA8546 has to be initialized by sending the two bytes of the initialize command (see Section 8.1.1 and Table 6).

After a reset and the initialization the starting conditions of the PCA8546 are as follows:

1. The display is disabled.

2. All backplane and segment outputs are set to V_{SS}.

3. The data pointers are cleared (set logic 0).

4. RAM data is not initialized. Its content can be considered to be random.

5. The internal oscillator is running; no clock signal is available on pin OSCCLK; pin OSCCLK is in 3-state.

The state after a reset and the initialization is shown in Table 20.

Table 20. Starting conditions

Associated command	Bits							
	7	6	5	4	3	2	1	0
mode-settings	-	-	-	-	BPS = 0	INV = 0	PD = 0	E = 0
oscillator-control	-	-	-	-	-	EFR = 0	COE = 0	OSC = 0
set-bias-mode	-	-	-	-	-	-	B[1:0] = 00	
frame-frequency	-	-	-	FD[4:0] = 0 1110				
load-data-pointer	-	-	DP[5:0] = 00 0000					

After Power-On Reset (POR) and the initialize command and before enabling the display, the RAM content should be brought to a defined state by writing meaningful content (for example, a graphic) otherwise unwanted display artifacts may appear on the display.

8.2.2 RESET pin function

The $\overline{\text{RESET}}$ pin sets the PCA8546 in a defined mode. The RAM content remains unchanged. After the reset signal is removed, the initialize command (see Section 8.1.1 and Table 6) has to be sent to the PCA8546. See Section 8.2.1 for details.

8.2.3 Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.

In general, the sequence should always be:

1. Power-on or reset the device,

2. send the initialize command,

3. set the display and functional modes,

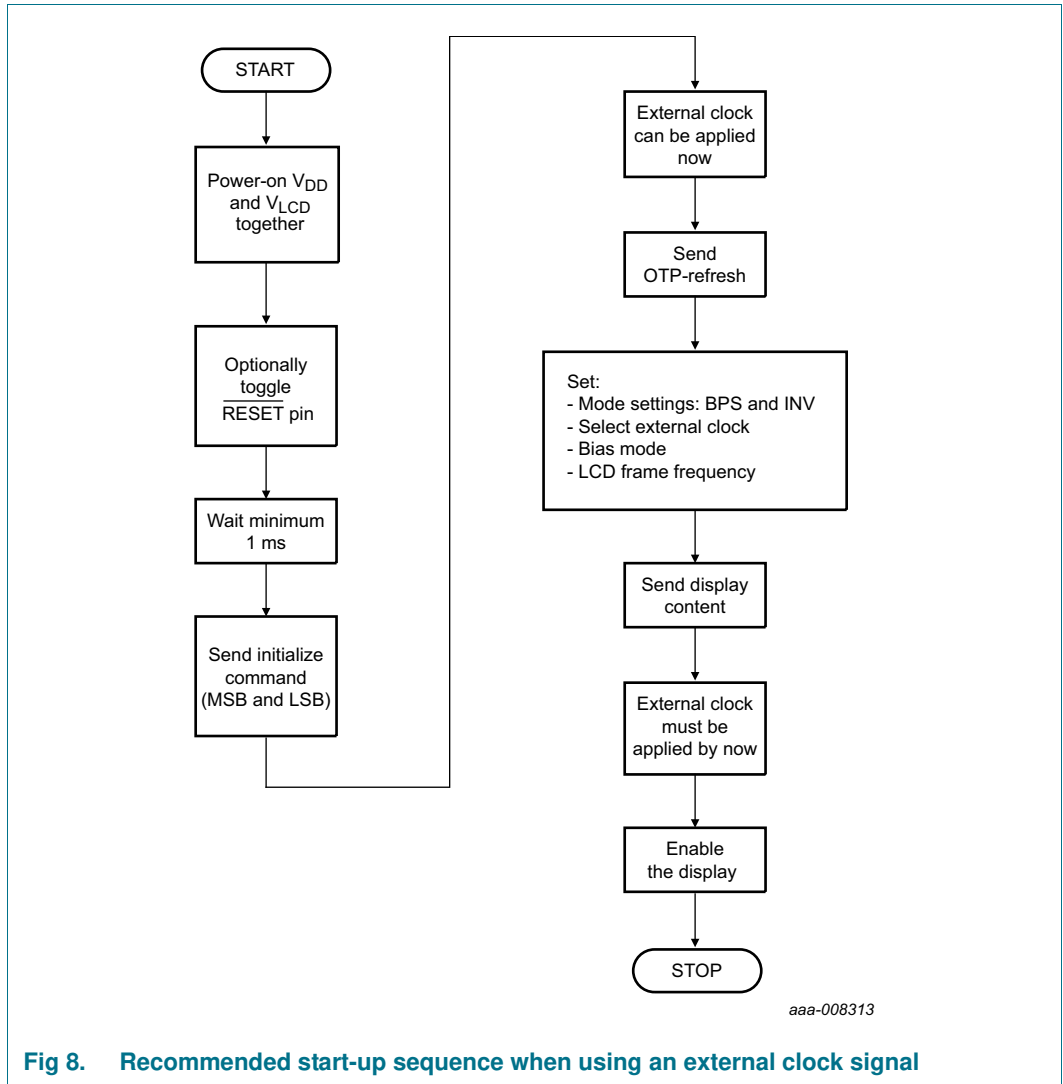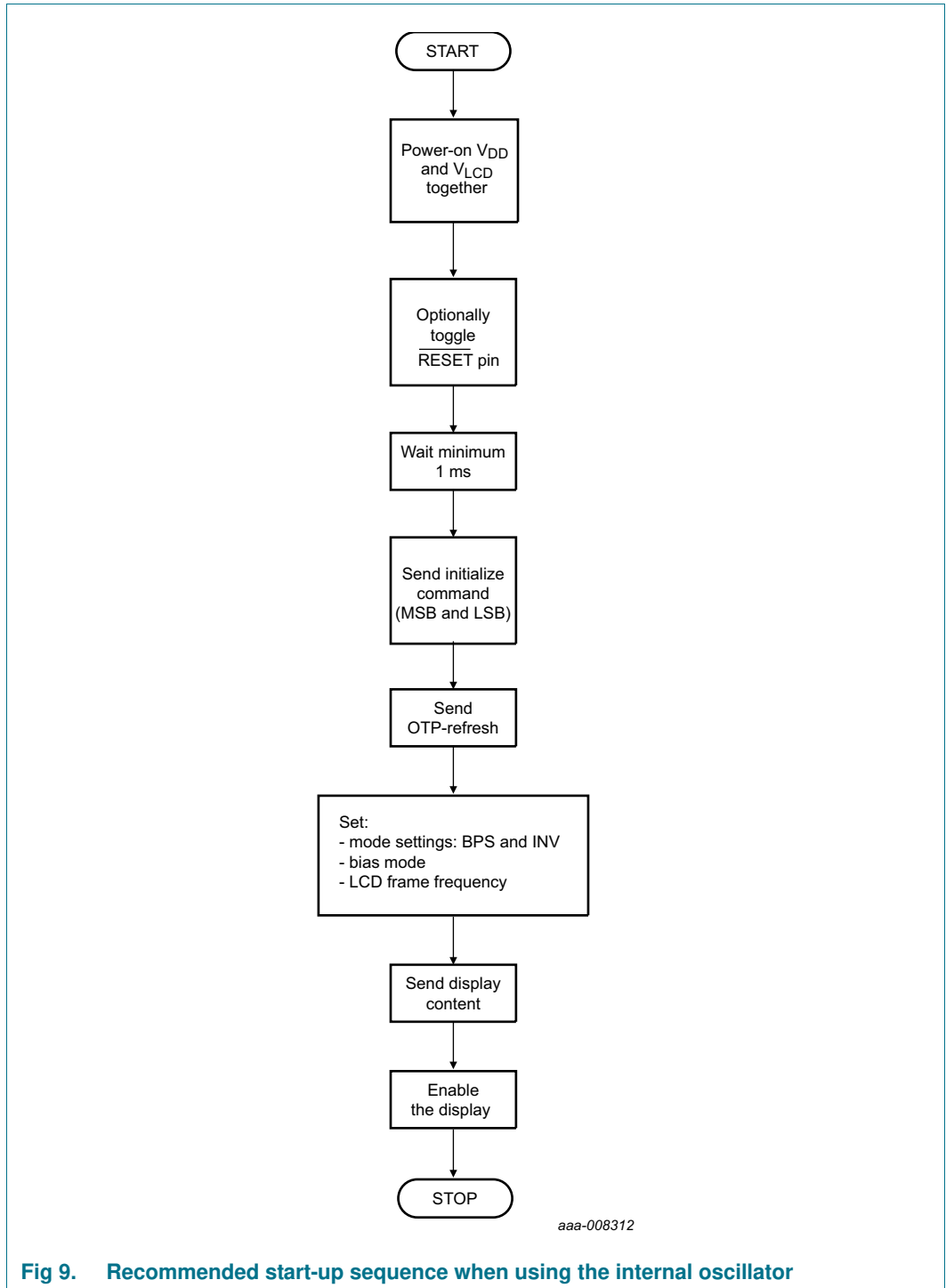4. fill the display memory and then

5. turn on the display.

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Fig 8.   Recommended start-up sequence when using an external clock signal

Fig 9.   **Recommended start-up sequence when using the internal oscillator**

8.3 Possible display configurations

The PCA8546 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 10). It can drive multiplexed LCD with 4 backplanes and up to 44 segments.
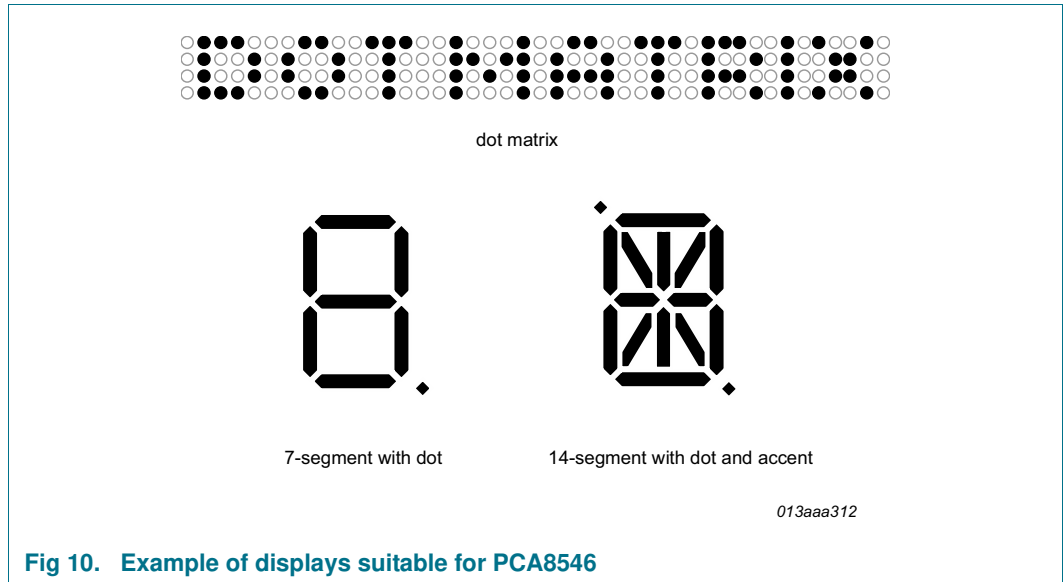

dot matrix

7-segment with dot   14-segment with dot and accent

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Fig 10. Example of displays suitable for PCA8546

Table 21. Display configuration

Number of			Digits/Characters		Dot matrix/ Elements
Backplanes	**Segments**	**Icons**	**7 segment**[1]	**14 segment**[2]	
4	44	176	22	11	176

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

The display configuration in Table 21 can be implemented in the typical systems shown in Figure 11 and Figure 12.
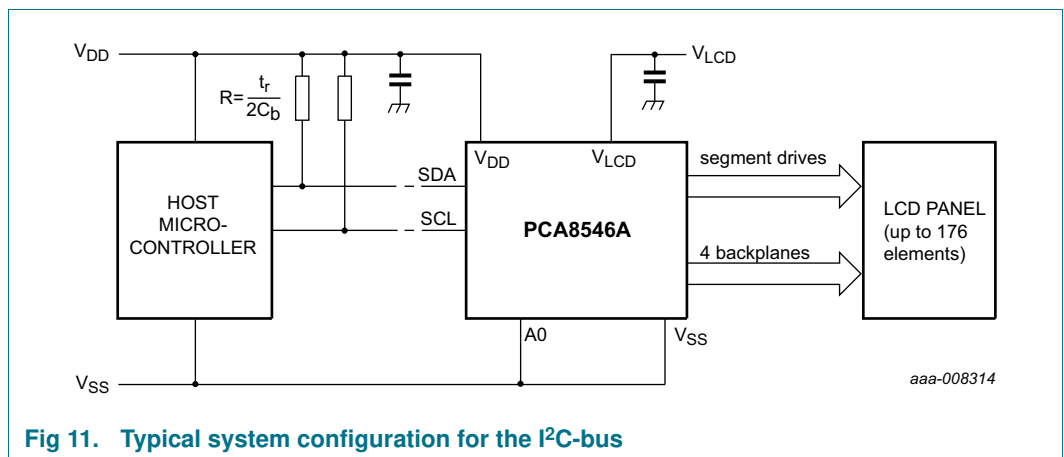

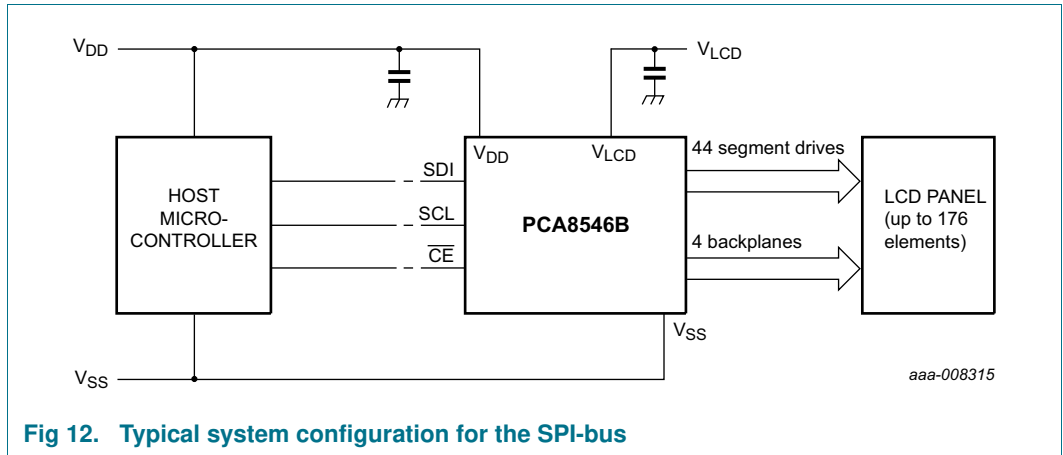**Fig 11. Typical system configuration for the I²C-bus**

Fig 12. Typical system configuration for the SPI-bus

The host microcontroller maintains the two line I2C-bus or a three line SPI-bus communication channel with the PCA8546. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, V_{LCD}) and the LCD panel selected for the application.

The minimum recommended values for external capacitors on V_{DD} and V_{LCD} are 100 nF respectively. Decoupling of V_{LCD} helps to reduce display artifacts. The decoupling capacitors should be placed close to the IC with short connections to the respective supply pin and V_{SS}.

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8.4 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the set-bias-mode command (see Table 15).

Fractional LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations, the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 22.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 22. Preferred LCD drive modes: summary of characteristics

LCD multiplex drive mode	Number of:		LCD bias configuration	$\dfrac{V_{off(RMS)}}{V_{LCD}}$	$\dfrac{V_{on(RMS)}}{V_{LCD}}$	$D = \dfrac{V_{on(RMS)}}{V_{off(RMS)}}$ [1]	V_{LCD} [2]
	Backplanes	Levels					
1:4 [3]	4	3	$\frac{1}{2}$	0.433	0.661	1.527	2.309$V_{off(RMS)}$
1:4	4	4	$\frac{1}{3}$	0.333	0.577	1.732	3.0$V_{off(RMS)}$
1:4 [3]	4	5	$\frac{1}{4}$	0.331	0.545	1.646	3.024$V_{off(RMS)}$

[1] Determined from Equation 5.

[2] Determined from Equation 4.

[3] In these examples, the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a reduction of the LCD voltage V_{LCD}.

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast.

Bias is calculated by $\dfrac{1}{1 + a}$, where the values for a are

   a = 1 for $\frac{1}{2}$ bias

   a = 2 for $\frac{1}{3}$ bias

   a = 3 for $\frac{1}{4}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 3

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \tag{3}$$

where V_{LCD} is the resultant voltage at the LCD segment and where the value for n is

   n = 4 for 1:4 multiplex drive

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \tag{4}$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 5:

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$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \tag{5}$$

V_{LCD} is sometimes referred to as the LCD operating voltage.

8.4.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel gets switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 13. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \tag{6}$$

$$V_{off(RMS)} \leq V_{th(off)} \tag{7}$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 3 to Equation 5) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

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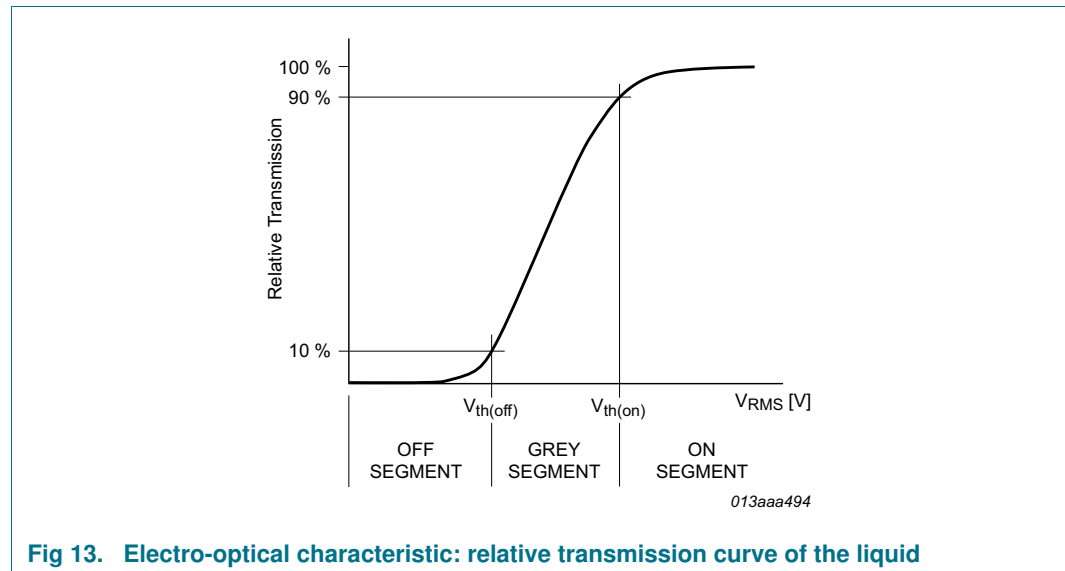
Fig 13. Electro-optical characteristic: relative transmission curve of the liquid

8.5 LCD drive mode waveforms
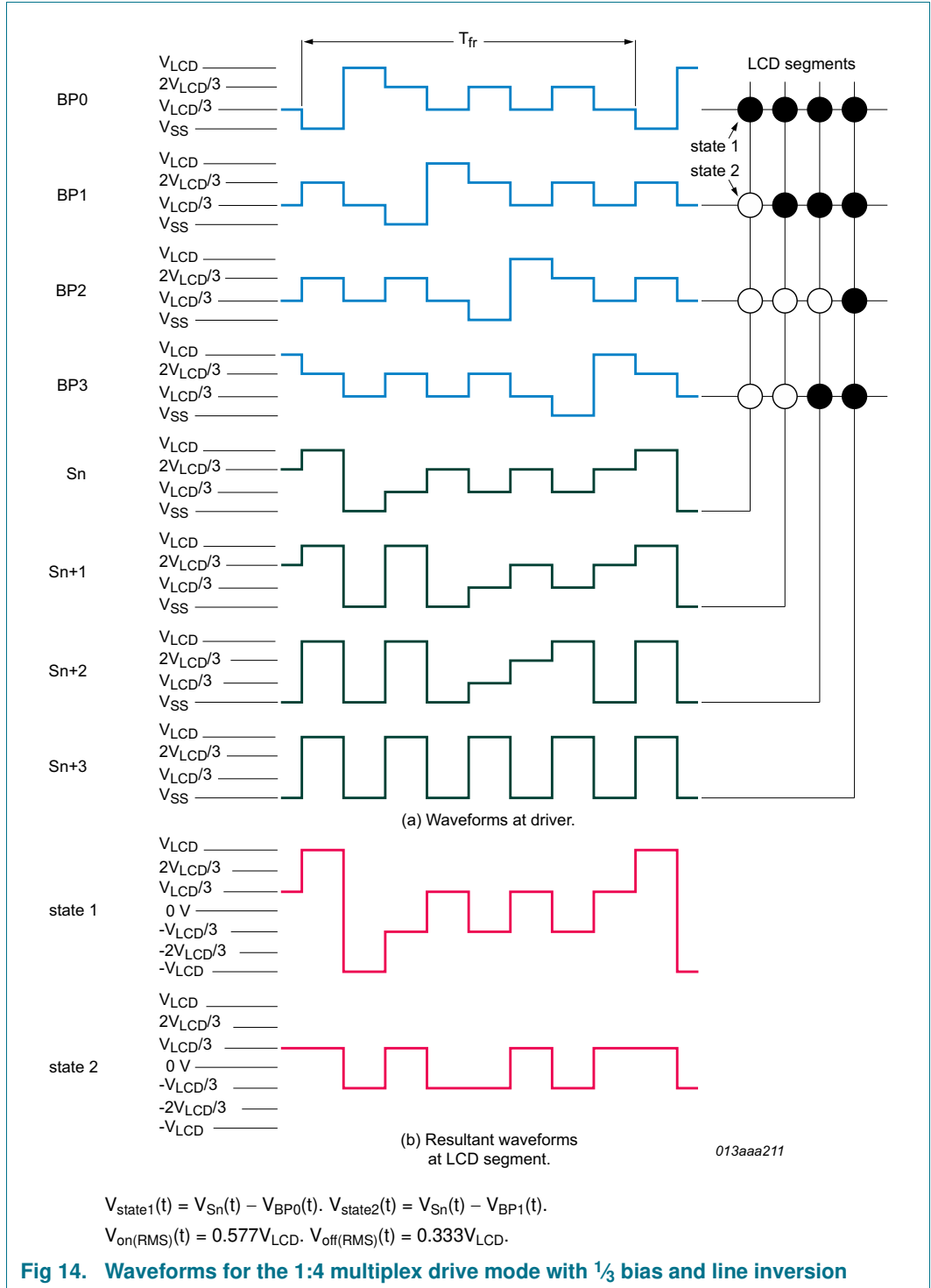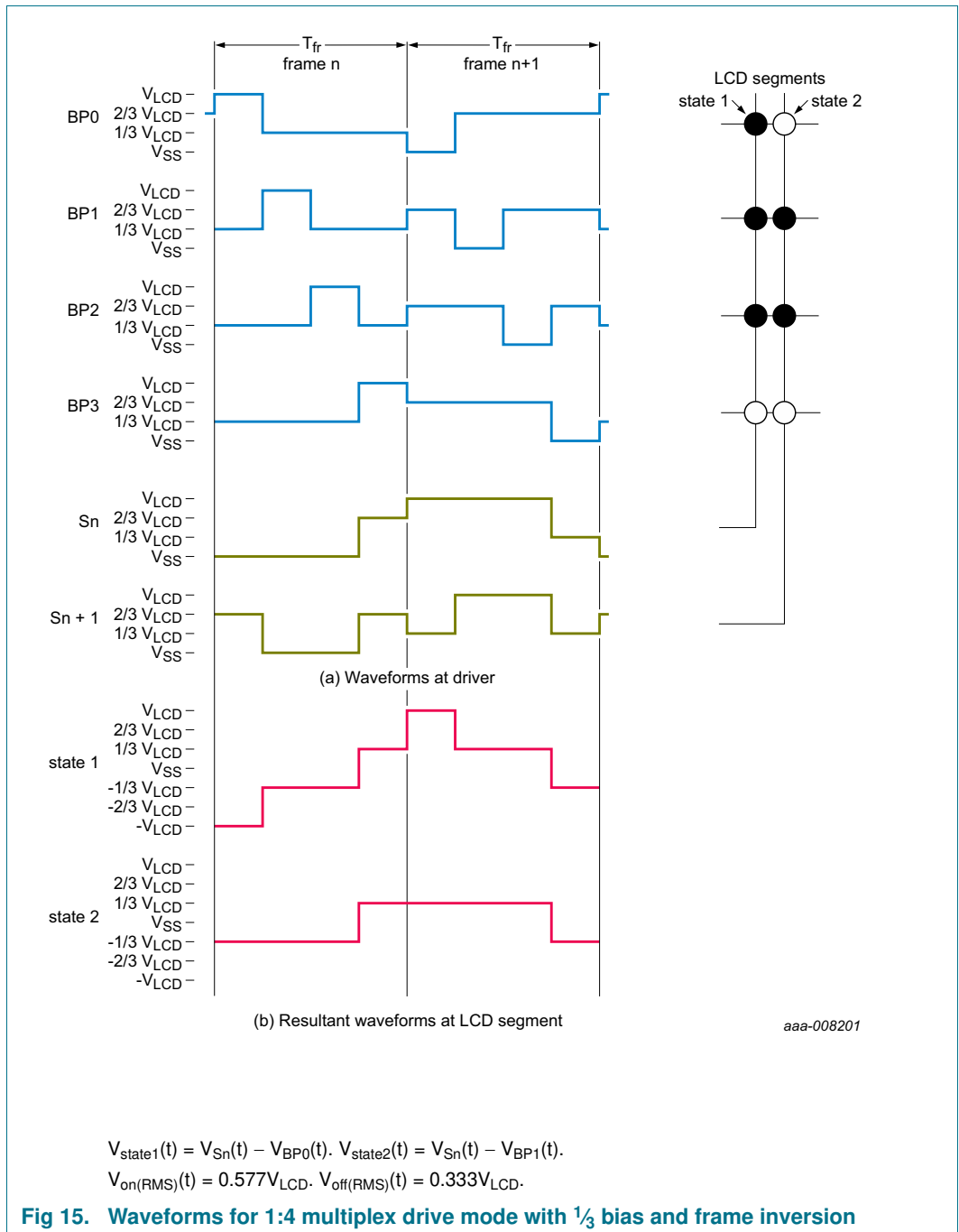
8.5.1 $\frac{1}{3}$ bias and line inversion

(a) Waveforms at driver.

(b) Resultant waveforms at LCD segment.

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$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.577V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 14. Waveforms for the 1:4 multiplex drive mode with $\frac{1}{3}$ bias and line inversion

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8.5.2 ⅓ bias and frame inversion

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.577V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 15.   Waveforms for 1:4 multiplex drive mode with ⅓ bias and frame inversion

8.6 Display register

The display register holds the display data while the corresponding multiplex signals are generated.