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# PCA8561

## Automotive 18 × 4 LCD segment driver

Rev. 4 — 27 March 2015

Product data sheet

### 1. General description

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PCA8561 is an ultra low-power LCD segment driver with 4 backplane- and 18 segment-driver outputs, with either an I<sup>2</sup>C- or an SPI-bus interface. It comprises an internal oscillator, bias generation, instruction decoding, and display controller.

For a selection of NXP LCD segment drivers, see [Table 24 on page 45](#).

### 2. Features and benefits

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- AEC-Q100 grade 2 (up to 105 °C) compliant for automotive applications
- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, 1/2, or 1/3
- Internal LCD bias generation with buffers
- 18 segment drives:
  - ◆ Up to 9 7-segment numeric characters
  - ◆ Up to 4 14-segment alphanumeric characters
  - ◆ Any graphics of up to 72 segments/elements
- Auto-incrementing display data and instruction loading
- Versatile blinking modes
- Independent supplies of V<sub>LCD</sub> and V<sub>DD</sub>
- Power supply ranges:
  - ◆ 1.8 V to 5.5 V for V<sub>LCD</sub>
  - ◆ 1.8 V to 5.5 V for V<sub>DD</sub>
- Ultra low-power consumption
- 400 kHz I<sup>2</sup>C-bus interface (PCA8561AHN)
- 5 MHz SPI-bus interface (PCA8561BHN)
- Internally generated or externally supplied clock signal
- Tiny package: HVQFN32, 5 mm × 5 mm

### 3. Applications

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- Small displays integrated
  - ◆ in a car instrument cluster
  - ◆ in a control knob
- Battery operated applications
- Healthcare devices



## 4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8561AHN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads;32 terminals; body 5 × 5 × 0.85 mm	SOT617-3
PCA8561BHN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads;32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

### 4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Interface type	Delivery form	IC revision
PCA8561AHN/A	PCA8561AHN/AY	935304072518	I <sup>2</sup> C-bus	tape and reel, 13 inch, dry pack	1
PCA8561BHN/A	PCA8561BHN/AY	935305329518	SPI-bus	tape and reel, 13 inch, dry pack	1

## 5. Marking

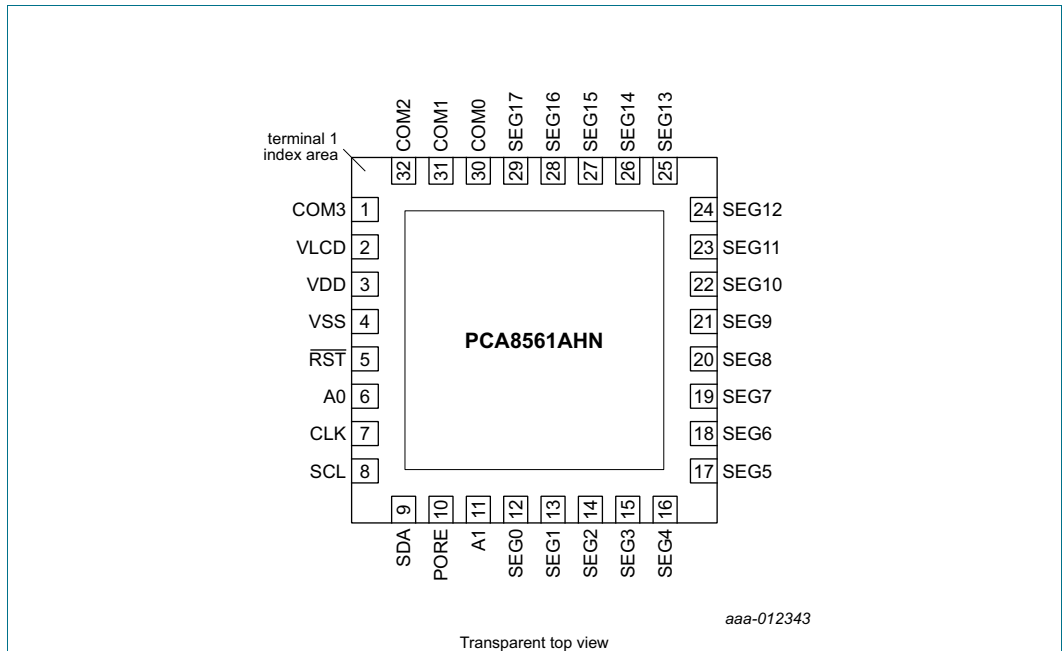
Table 3. Marking codes

Type number	Marking code
PCA8561AHN/A	8561A
PCA8561BHN/A	8561B



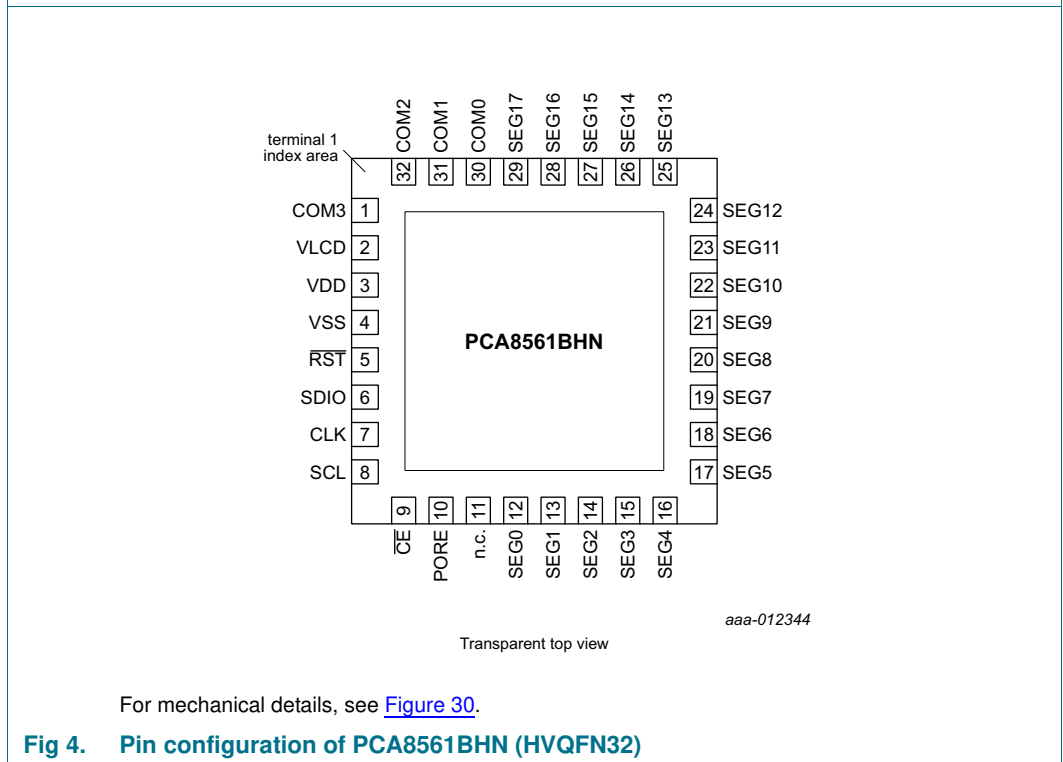
## 7. Pinning information

### 7.1 Pinning



For mechanical details, see [Figure 30](#).

**Fig 3. Pin configuration of PCA8561AHN (HVQFN32)**



For mechanical details, see [Figure 30](#).

**Fig 4. Pin configuration of PCA8561BHN (HVQFN32)**

## 7.2 Pin description

**Table 4. Pin description**

Input or input/output pins must always be at a defined level ( $V_{SS}$  or  $V_{DD}$ ) unless otherwise specified.

Pin	Symbol	Type	Description
1	COM3	output	LCD backplane output
2	VLCD	supply	LCD supply voltage
3	VDD	supply	supply voltage
4	VSS <sup>[1]</sup>	supply	ground supply
5	$\overline{RST}$	input	reset input, active LOW
7	CLK	input/output	internal oscillator output, external oscillator input <ul style="list-style-type: none"> <li>• must be left open if unused</li> </ul>
8	SCL	input	serial clock input
10	PORE <sup>[2]</sup>	input	Power-On Reset (POR) enable <ul style="list-style-type: none"> <li>• connect to <math>V_{DD}</math> for enabling POR</li> <li>• connect to <math>V_{SS}</math> (or leave open) for disabling POR</li> </ul>
12 to 29	SEG0 to SEG17	output	LCD segment outputs
30 to 32	COM0 to COM2	output	LCD backplane outputs

### Pin layout depending on product and bus type

	PCA8561AHN (I <sup>2</sup> C-bus)	PCA8561BHN (SPI-bus)		
6	A0 <sup>[2]</sup>	-	input	hardware device address selection; <ul style="list-style-type: none"> <li>• connect to <math>V_{SS}</math> (or leave open) for logic 0</li> <li>• connect to <math>V_{DD}</math> for logic 1</li> </ul>
	-	SDIO	input/output	serial data input/output
9	SDA	-	output	serial data output
	-	$\overline{CE}$	input	chip enable input, active LOW
11	A1 <sup>[2]</sup>	-	input	hardware device address selection; <ul style="list-style-type: none"> <li>• connect to <math>V_{SS}</math> (or leave open) for logic 0</li> <li>• connect to <math>V_{DD}</math> for logic 1</li> </ul>
	-	n.c.	-	not connected

[1] The die paddle (exposed pad) is connected to  $V_{SS}$  and should be electrically isolated.

[2] A series resistance between  $V_{DD}$  and the pin must not exceed 1 k $\Omega$  to ensure proper functionality, see [Section 16.3](#).

## 8. Functional description

### 8.1 Registers of the PCA8561

The registers of the PCA8561 are arranged in bytes with 8 bit, addressed by an address pointer. [Table 5](#) depicts the layout.

**Table 5. Registers of the PCA8561**

Bits labeled as 0 must always be written with logic 0; bits labeled as - are ignored by the device.

Register name	Address	Bits								Reference
		AP[4:0]	7	6	5	4	3	2	1	
<b>Command registers</b>										
Software_reset	00h	SR[7:0]								<a href="#">Table 9</a>
Device_ctrl	01h	0	0	0	FF[2:0]			OSC	COE	<a href="#">Table 6</a>
Display_ctrl_1	02h	0	0	0	BOOST	MUX[1:0]		B	DE	<a href="#">Table 7</a>
Display_ctrl_2	03h	0	0	0	0	0	BL[1:0]		INV	<a href="#">Table 8</a>
<b>Display data registers<sup>[1]</sup></b>										
COM0	04h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	<a href="#">Table 10</a>
	05h	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	
	06h	-	-	-	-	-	-	SEG17	SEG16	
COM1	07h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	08h	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	
	09h	-	-	-	-	-	-	SEG17	SEG16	
COM2	0Ah	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	0Bh	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	
	0Ch	-	-	-	-	-	-	SEG17	SEG16	
COM3	0Dh	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
	0Eh	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	
	0Fh	-	-	-	-	-	-	SEG17	SEG16	

[1] See [Table 10](#).

For writing to the registers, send the address byte first, then write the data to the register (see [Section 11.1.4](#) and [Section 11.2.1](#)). The address byte works as an address pointer. For the succeeding registers, the address pointer is automatically incremented by 1 (see [Figure 5](#)) and all following data are written into these register addresses. After address 10h, the auto-incrementing will stop and data are ignored.

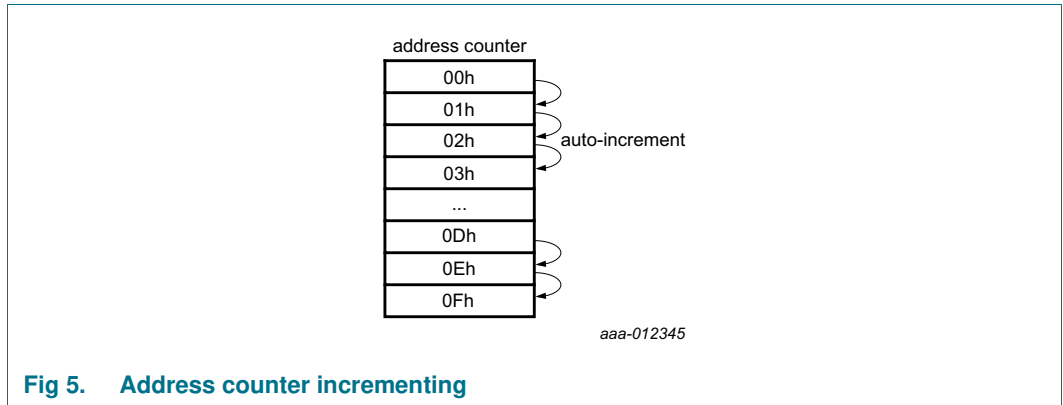


Fig 5. Address counter incrementing

## 8.2 Command registers of the PCA8561

### 8.2.1 Command: Device\_ctrl

The Device\_ctrl command sets the device into a defined state. It should be executed before enabling the display (see bit DE in [Table 7](#)).

Table 6. Device\_ctrl - device control command register (address 01h) bit description

Bit	Symbol	Value	Description
7 to 5	-	000	default value
4 to 2	FF[2:0]	<b>frame frequency selection</b>	
		000	f <sub>fr</sub> = 32 Hz
		001 <sup>[1]</sup>	f <sub>fr</sub> = 64 Hz
		010	f <sub>fr</sub> = 96 Hz
		011	f <sub>fr</sub> = 128 Hz
		100	f <sub>fr</sub> = 160 Hz
		101	f <sub>fr</sub> = 192 Hz
		110	f <sub>fr</sub> = 224 Hz
111	f <sub>fr</sub> = 256 Hz		
1	OSC	<b>internal oscillator control</b>	
		0 <sup>[1]</sup>	enabled
		1	disabled
0	COE	<b>clock output enable</b>	
		0 <sup>[1]</sup>	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

[1] Default value.

#### 8.2.1.1 Internal oscillator and clock output

Bit OSC enables or disables the internal oscillator. When the internal oscillator is used, bit COE allows making the clock signal available on pin CLK. If this is not intended, pin CLK should be left open. The design ensures that the duty cycle of the clock output is 50 : 50 (% HIGH-level time : % LOW-level time).



In applications where an external clock has to be applied to the PCA8561, bit OSC must be set logic 1 and COE logic 0. In this case pin CLK becomes an input.

In power-down mode (see [Section 8.3.1](#))

- if pin CLK is configured as an output, there is no signal on CLK
- if pin CLK is configured as an input, the signal on CLK can be removed.

**Remark:** A clock signal must always be supplied to the device if the display is enabled (see bit DE in [Table 7 on page 8](#)). Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

### 8.2.2 Command: Display\_ctrl\_1

The Display\_ctrl\_1 command allows configuring the basic display set-up.

**Table 7. Display\_ctrl\_1 - display control command 1 register (address 02h) bit description**

Bit	Symbol	Value	Description
7 to 5	-	000	default value
4	BOOST	<b>large display mode support</b>	
		0 <sup>[1]</sup>	standard power drive scheme
		1	enhanced power drive scheme for higher display loads
3 to 2	MUX[1:0]	<b>multiplex drive mode selection</b>	
		00 <sup>[1]</sup>	1:4 multiplex drive mode; COM0 to COM3 (n <sub>MUX</sub> = 4)
		01	1:3 multiplex drive mode; COM0 to COM2 (n <sub>MUX</sub> = 3)
		10	1:2 multiplex drive mode; COM0 and COM1 (n <sub>MUX</sub> = 2)
		11	static drive mode; COM0 (n <sub>MUX</sub> = 1)
1	B <sup>[2]</sup>	<b>bias mode selection</b>	
		0 <sup>[1]</sup>	1/3 bias (a <sub>bias</sub> = 2)
		1	1/2 bias (a <sub>bias</sub> = 1)
0	DE	<b>display enable<sup>[3]</sup></b>	
		0 <sup>[1]</sup>	display disabled; device is in power-down mode
		1	display enabled; device is in power-on mode

[1] Default value.

[2] Not applicable for static drive mode.

[3] See [Section 8.3.1](#).

#### 8.2.2.1 Enhanced power drive mode

By setting the BOOST bit to logic 1, the driving capability of the display signals is increased to cope with large displays with a higher effective capacitance. Setting this bit increases the current consumption on V<sub>LCD</sub>.

#### 8.2.2.2 Multiplex drive mode

MUX[1:0] sets the multiplex driving scheme and the associated backplane drive signals, which are active. For further details, see [Section 9.2 on page 15](#).

8.2.3 Command: Display\_ctrl\_2

Table 8. Display\_ctrl\_2 - display control command 2 register (address 03h) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	default value
2 to 1	BL[1:0]	<b>blink control</b>	
		00 <sup>[1]</sup>	blinking off
		01	blinking on, $f_{blink} = 0.5 \text{ Hz}$
		10	blinking on, $f_{blink} = 1 \text{ Hz}$
		11	blinking on, $f_{blink} = 2 \text{ Hz}$
0	INV	<b>inversion mode selection</b>	
		0 <sup>[1]</sup>	line inversion (driving scheme A)
		1	frame inversion (driving scheme B)

[1] Default value.

8.2.3.1 Blinking

The whole display blinks at frequencies selected by the blink control bits BL[1:0], see [Table 8](#). The blink frequencies are derived from the clock frequency. During the blank-out phase of the blinking period, the display is turned off.

If an external clock with frequency  $f_{clk(ext)}$  is used, the blinking frequency is determined by [Equation 1](#). For notation, see [Section 9.2](#).

$$f_{blink(eff)} = \frac{2 \times n_{MUX} \times f_{fr} \times f_{blink}}{f_{clk(ext)}} \tag{1}$$

8.2.3.2 Line inversion (driving scheme A) and frame inversion (driving scheme B)

The waveforms used to drive LCD inherently produce a DC voltage across the display cell. The PCA8561 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of compensation method is determined with the INV bit.

### 8.3 Starting and resetting the PCA8561

If the internal Power-On Reset (POR) is enabled by connecting pin PORE to  $V_{DD}$ , the chip resets automatically when  $V_{DD}$  rises above the minimum supply voltage. No further action is required.

If the internal POR is disabled by connecting pin PORE to  $V_{SS}$ , the chip must be reset by driving the  $\overline{RST}$  pin to logic 0 for at least 10  $\mu\text{s}$ , see [Figure 6](#).

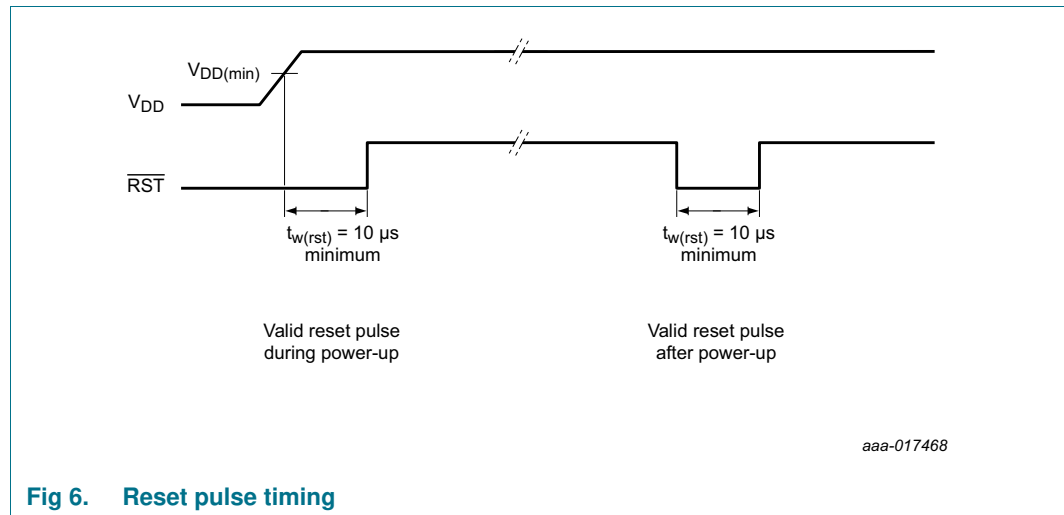


Fig 6. Reset pulse timing

Alternatively a software reset can be applied (see [Section 8.3.4](#)).

Following a reset, the register 00h has to be rewritten with 0h by the next command byte or the address pointer AP[4:0] has to be set to the required address after a new START procedure.

#### 8.3.1 Power-down mode

After a reset, the PCA8561 remains in power-down mode. In power-down mode the oscillator is switched off and there is no output on pin CLK. The register settings remain unchanged and the bus remains active. To enable the PCA8561, bit DE (command Display\_ctrl\_1, see [Table 7 on page 8](#)) must be set to logic 1.

#### 8.3.2 Power-On Reset (POR)

If pin PORE is connected to  $V_{DD}$ , the PCA8561 comprises an internal POR, which puts the device into the following starting conditions:

- All backplane and segment outputs are set to  $V_{SS}$
- The selected drive mode is: 1:4 multiplex with  $\frac{1}{3}$  bias
- Blinking is switched off
- The address pointer is cleared (set to logic 0)
- The display and the internal oscillator are disabled
- The display registers are set to logic 0
- The bus interface is initialized

**Remark:** The internal POR can be disabled by connecting pin PORE to  $V_{SS}$ . In this case, the internal registers are not defined and require a hardware reset according to [Section 8.3.3](#) or a software reset, see [Section 8.3.4](#).

### 8.3.3 Hardware reset: $\overline{RST}$ pin

At power-on the PCA8561 can be reset to the following starting conditions by pulling pin  $\overline{RST}$  low:

- All backplane and segment outputs are set to  $V_{SS}$
- The selected drive mode is: 1:4 multiplex with  $\frac{1}{3}$  bias
- Blinking is switched off
- The bus interface is initialized
- The address pointer is cleared (set to logic 0)
- The display and the internal oscillator are disabled
- The display registers are set to logic 0

**Remark:** The hardware reset overrides the POR see [Section 8.3.2](#).

### 8.3.4 Command: Software\_reset

The internal registers including the display registers and the address pointer (set to logic 0) of the device are reset by the Software\_reset command.

**Table 9. Software\_reset - software reset command register (address 00h) bit description**  
This register can only be written but not read.

Bit	Symbol	Value	Description
7 to 0	SR[7:0]		<b>software reset</b>
		00000000 <sup>[1]</sup>	no reset
		00101100	software reset

[1] Default value.

## 8.4 Display data register mapping

The example in [Table 10](#) and [Figure 7](#) illustrates the segment and backplane mapping of the display in relation to the display RAM.

For example, in 1:4 multiplex drive mode, the backplanes are served by signals COM0 to COM3 and the segments are driven by signals SEG0 to SEG17. Contents of addresses 04h to 06h are allocated to the first row (COM0) starting with the LSB driving the leftmost element and moving forward to the right with increasing bit position. If a bit is logic 0, the element is off, if it is logic 1 the element is turned on. All register content is LSB to MSB left to right. Addresses 07h to 09h serve COM1 signals, addresses 0Ah to 0Ch serve COM2 signals, and addresses 0Dh to 0Fh serve COM3 signals.

For displays with fewer segments/elements the unused bits are ignored.

Table 10. Register to segment and backplane mapping

Backplanes <sup>[1]</sup>	Segments					
	SEG0 to SEG7		SEG8 to SEG15		SEG16 to SEG17	
	LSB	MSB	LSB	MSB	LSB	MSB
<b>1:4 multiplex drive mode</b>						
COM0	content of 04h		content of 05h		content of 06h <sup>[2]</sup>	
COM1	content of 07h		content of 08h		content of 09h <sup>[2]</sup>	
COM2	content of 0Ah		content of 0Bh		content of 0Ch <sup>[2]</sup>	
COM3	content of 0Dh		content of 0Eh		content of 0Fh <sup>[2]</sup>	
<b>1:3 multiplex drive mode</b>						
COM0	content of 04h		content of 05h		content of 06h <sup>[2]</sup>	
COM1	content of 07h		content of 08h		content of 09h <sup>[2]</sup>	
COM2	content of 0Ah		content of 0Bh		content of 0Ch <sup>[2]</sup>	
<b>1:2 multiplex drive mode</b>						
COM0	content of 04h		content of 05h		content of 06h <sup>[2]</sup>	
COM1	content of 07h		content of 08h		content of 09h <sup>[2]</sup>	
<b>static drive mode</b>						
COM0	content of 04h		content of 05h		content of 06h <sup>[2]</sup>	

[1] See also [Section 9.3.1 on page 23](#).

[2] Bits [7:2] are ignored.

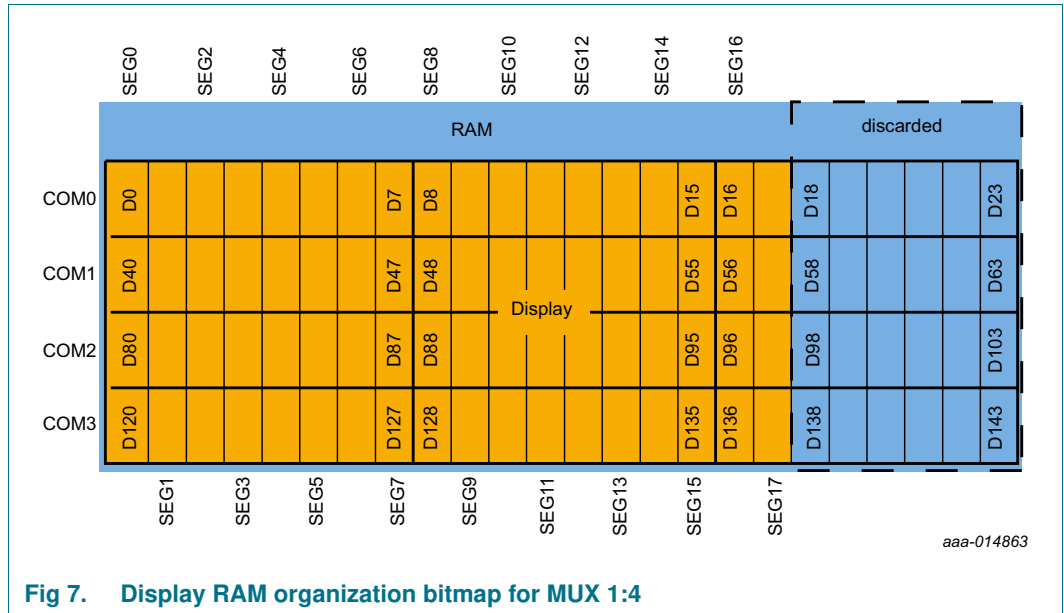


Fig 7. Display RAM organization bitmap for MUX 1:4

## 9. Possible display configurations

The possible display configurations of the PCA8561 depend on the number of active backplane outputs required. A selection of display configurations is shown in [Table 11](#). All of these configurations can be implemented in the typical systems shown in [Figure 9](#) or [Figure 10](#).

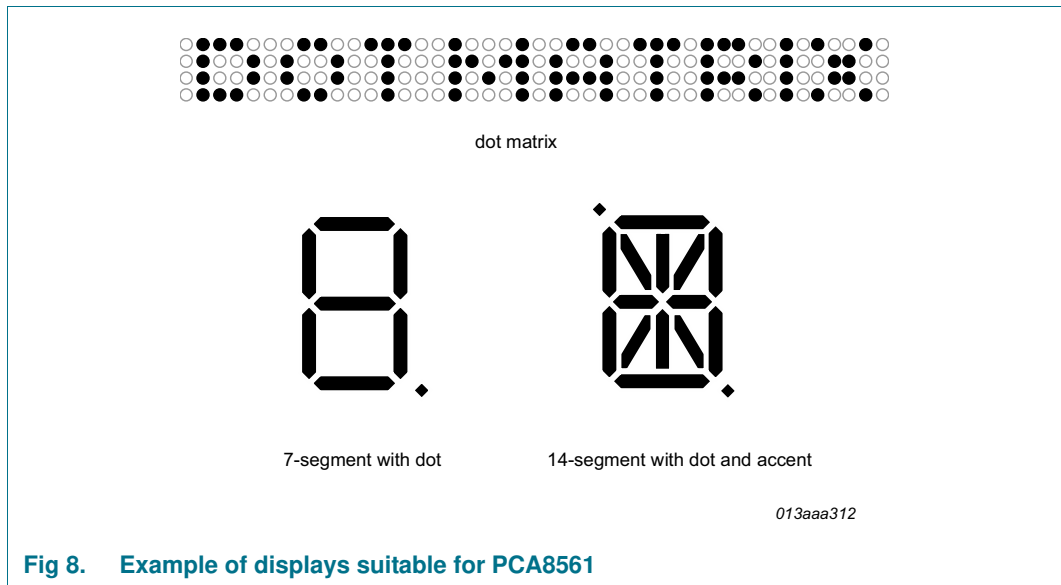


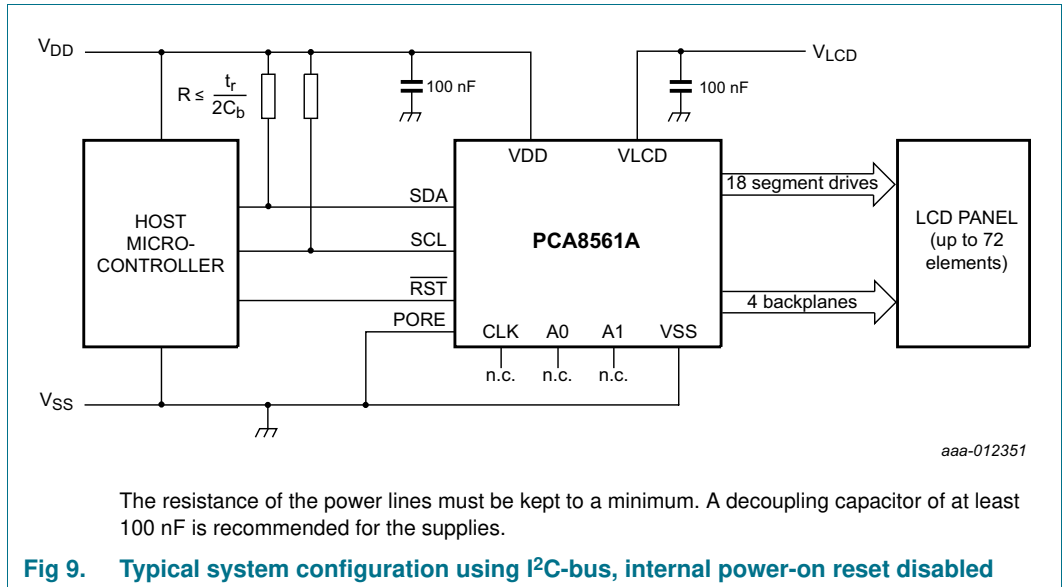
Fig 8. Example of displays suitable for PCA8561

Table 11. Selection of possible display configurations

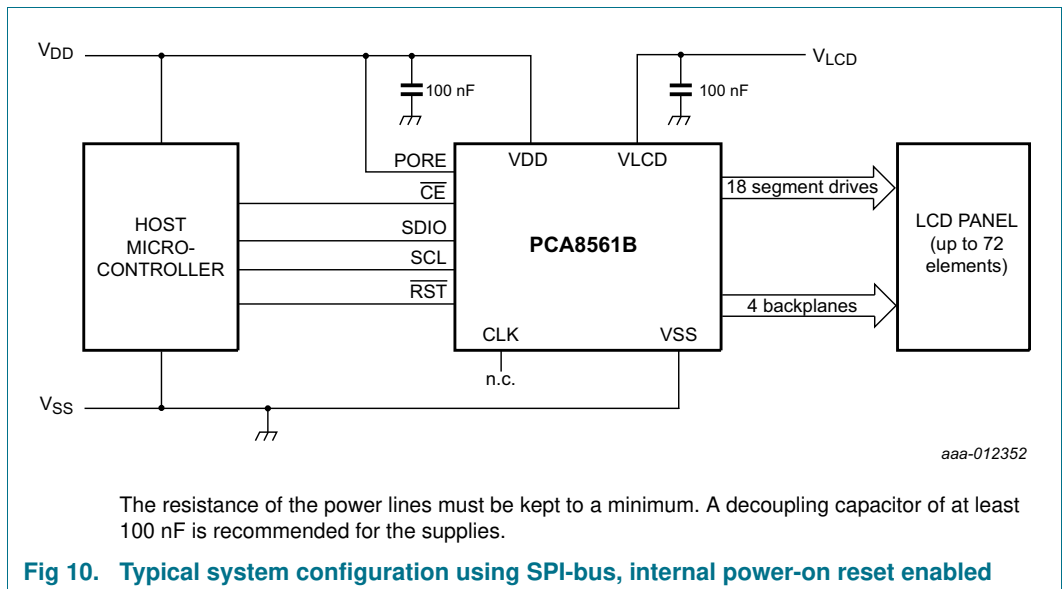
Number of				
Backplanes	Icons	Digits/Characters		Dot matrix: segments/elements
		7-segment <sup>[1]</sup>	14-segment <sup>[2]</sup>	
4	72	9	4	72 dots (4 × 18)
3	54	6	3	54 dots (3 × 18)
2	36	4	2	36 dots (2 × 18)
1	18	2	1	18 dots (1 × 18)

[1] 7 segment display has 8 segments/elements including the decimal point.

[2] 14 segment display has 16 segments/elements including decimal point and accent dot.



The host microcontroller manages the 2-line I<sup>2</sup>C-bus communication channel with the PCA8561. The internal oscillator is used and the internal POR is disabled in the example (Figure 9). The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the reset, the power supplies (V<sub>DD</sub>, V<sub>SS</sub>, and V<sub>LCD</sub>) and the LCD panel chosen for the application.



The host microcontroller manages the 3-line SPI-bus communication channel with the PCA8561. The internal oscillator is enabled and the internal POR is enabled in the example (Figure 10). The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are reset, the power supplies (V<sub>DD</sub>, V<sub>SS</sub>, and V<sub>LCD</sub>) and the LCD panel chosen for the application.

### 9.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between  $V_{LCD}$  and  $V_{SS}$ . These intermediate levels are tapped off at positions of  $\frac{1}{3}$  and  $\frac{2}{3}$ , or  $\frac{1}{2}$ , depending on the bias mode chosen. To keep current consumption to a minimum, on-chip low-power buffers provide these levels to the display.

### 9.2 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the Display\_ctrl\_1 command (see Table 7). The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of  $V_{LCD}$  and the resulting discrimination ratios (D) are given in Table 12.

Table 12. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	$\infty$
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for  $V_{LCD}$  is determined by equating  $V_{off(RMS)}$  with a defined LCD threshold voltage ( $V_{th(off)}$ ), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is  $V_{LCD} > 3V_{th(off)}$ .

Multiplex drive modes of 1:3 and 1:4 with  $\frac{1}{2}$  bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated with Equation 2

$$\frac{1}{1 + a_{bias}} \tag{2}$$

The values for  $a_{bias}$  are:

$$a_{bias} = 1 \text{ for } \frac{1}{2} \text{ bias}$$

$$a_{bias} = 2 \text{ for } \frac{1}{3} \text{ bias}$$

The RMS on-state voltage ( $V_{on(RMS)}$ ) for the LCD is calculated with Equation 3:

$$V_{on(RMS)} = V_{LCD} \sqrt{\frac{a_{bias}^2 + 2a_{bias} + n_{MUX}}{n_{MUX} \times (1 + a_{bias})^2}} \tag{3}$$



where the values for  $n_{MUX}$  are

- $n_{MUX} = 1$  for static drive mode
- $n_{MUX} = 2$  for 1:2 multiplex drive mode
- $n_{MUX} = 3$  for 1:3 multiplex drive mode
- $n_{MUX} = 4$  for 1:4 multiplex drive mode

The RMS off-state voltage ( $V_{off(RMS)}$ ) for the LCD is calculated with [Equation 4](#):

$$V_{off(RMS)} = V_{LCD} \sqrt{\frac{a_{bias}^2 - 2a_{bias} + n_{MUX}}{n_{MUX} \times (1 + a_{bias})^2}} \quad (4)$$

Discrimination is a term which is defined as the ratio of the on and off RMS voltages ( $V_{on(RMS)}$  to  $V_{off(RMS)}$ ) across a segment. It can be thought of as a measurement of contrast. Discrimination is determined from [Equation 5](#):

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a_{bias}^2 + 2a_{bias} + n_{MUX}}{a_{bias}^2 - 2a_{bias} + n_{MUX}}} \quad (5)$$

Using [Equation 5](#), the discrimination for an LCD drive mode of 1:3 multiplex with  $\frac{1}{2}$  bias is  $\sqrt{3} = 1.732$  and the discrimination for an LCD drive mode of 1:4 multiplex with  $\frac{1}{2}$  bias is  $\frac{\sqrt{21}}{3} = 1.528$ .

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage  $V_{LCD}$  as follows:

- 1:3 multiplex ( $\frac{1}{2}$  bias):  $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex ( $\frac{1}{2}$  bias):  $V_{LCD} = \left[ \frac{4 \times \sqrt{3}}{3} \right] = 2.309V_{off(RMS)}$

These compare with  $V_{LCD} = 3V_{off(RMS)}$  when  $\frac{1}{3}$  bias is used.

$V_{LCD}$  is sometimes referred as the LCD operating voltage.

### 9.2.1 Electro-optical performance

Suitable values for  $V_{on(RMS)}$  and  $V_{off(RMS)}$  are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at  $V_{th(off)}$ ) and the other at 90 % relative transmission (at  $V_{th(on)}$ ), see [Figure 11](#). For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (6)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (7)$$

$V_{on(RMS)}$  (see [Equation 3](#)) and  $V_{off(RMS)}$  (see [Equation 5](#)) are properties of the display driver and are affected by the selection of  $a_{bias}$ ,  $n_{MUX}$ , and the  $V_{LCD}$  voltage.

$V_{th(off)}$  and  $V_{th(on)}$  are properties of the LCD liquid and can be provided by the module manufacturer.  $V_{th(off)}$  is sometimes named  $V_{th}$ .  $V_{th(on)}$  is sometimes named saturation voltage  $V_{sat}$ .

It is important to match the module properties to those of the driver in order to achieve optimum performance.

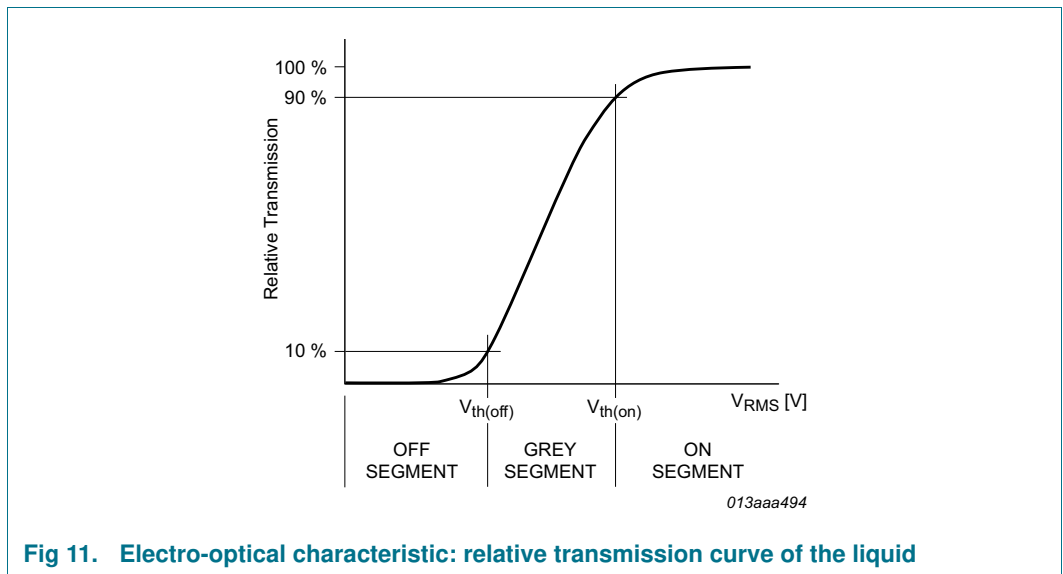


Fig 11. Electro-optical characteristic: relative transmission curve of the liquid

9.2.2 LCD drive mode waveforms

9.2.2.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (COMn) and segment (SEGN) drive waveforms for this mode are shown in [Figure 12](#).

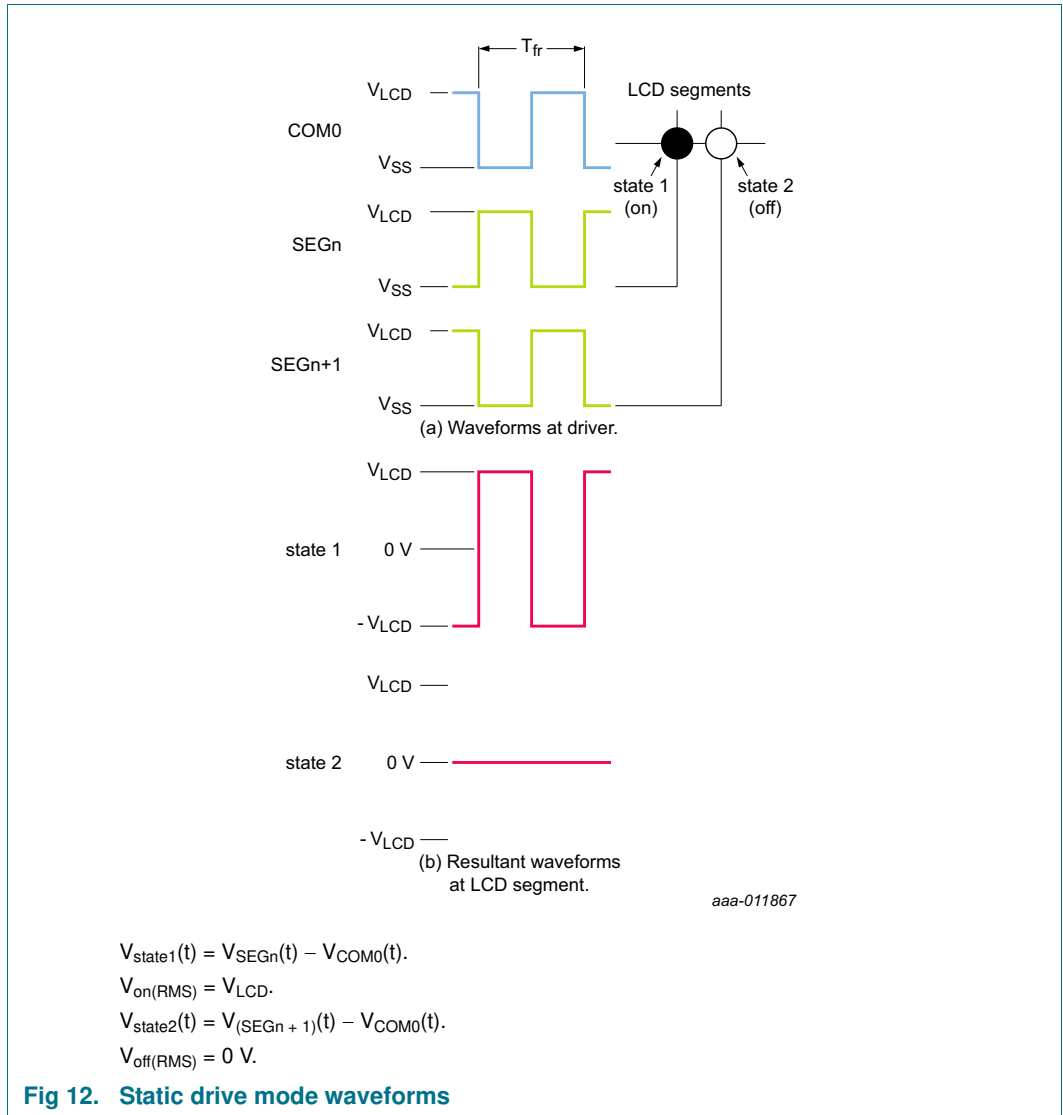
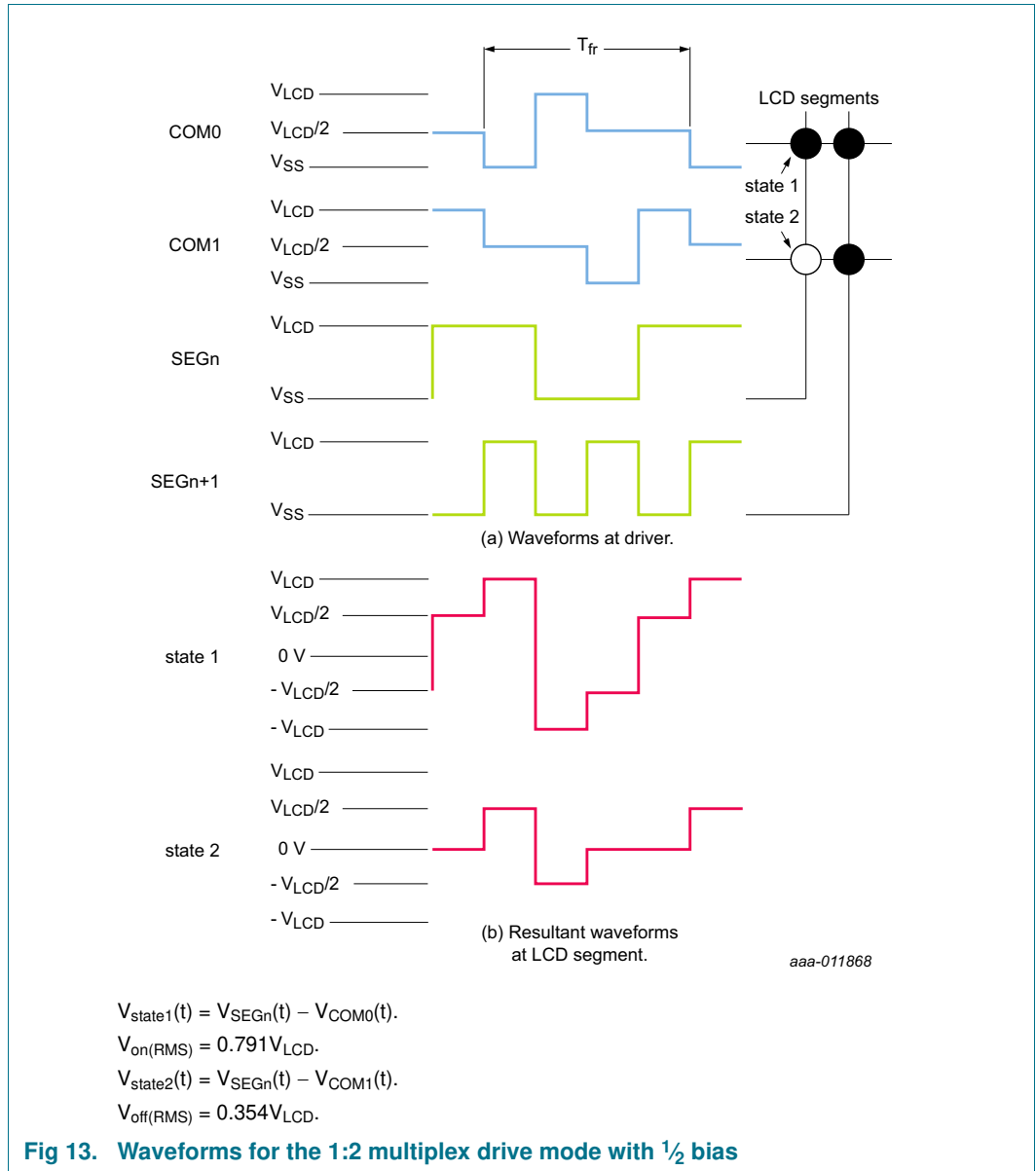
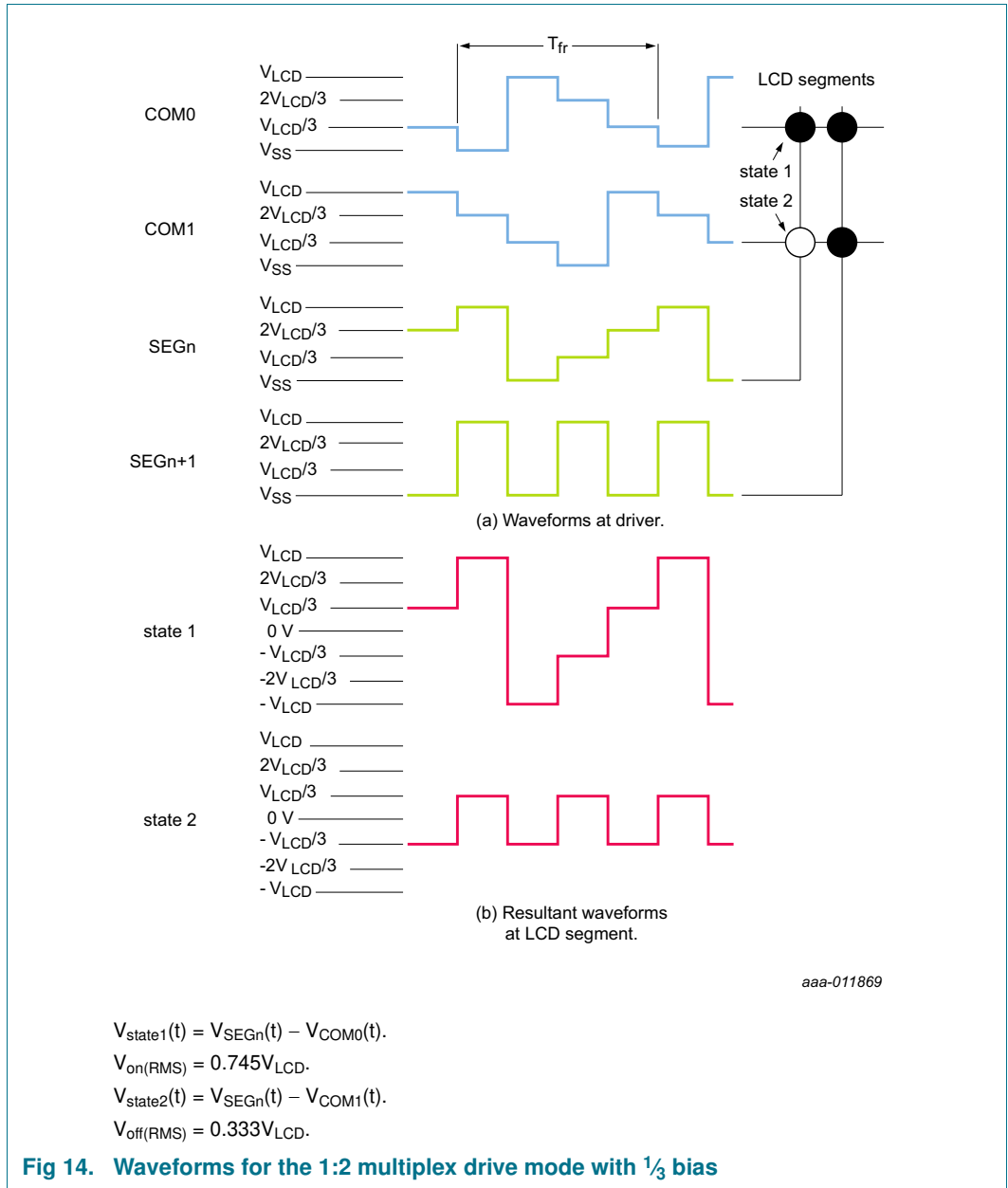


Fig 12. Static drive mode waveforms

9.2.2.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA8561 allows the use of 1/2 bias or 1/3 bias in this mode as shown in Figure 13 and Figure 14.





9.2.2.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 15.

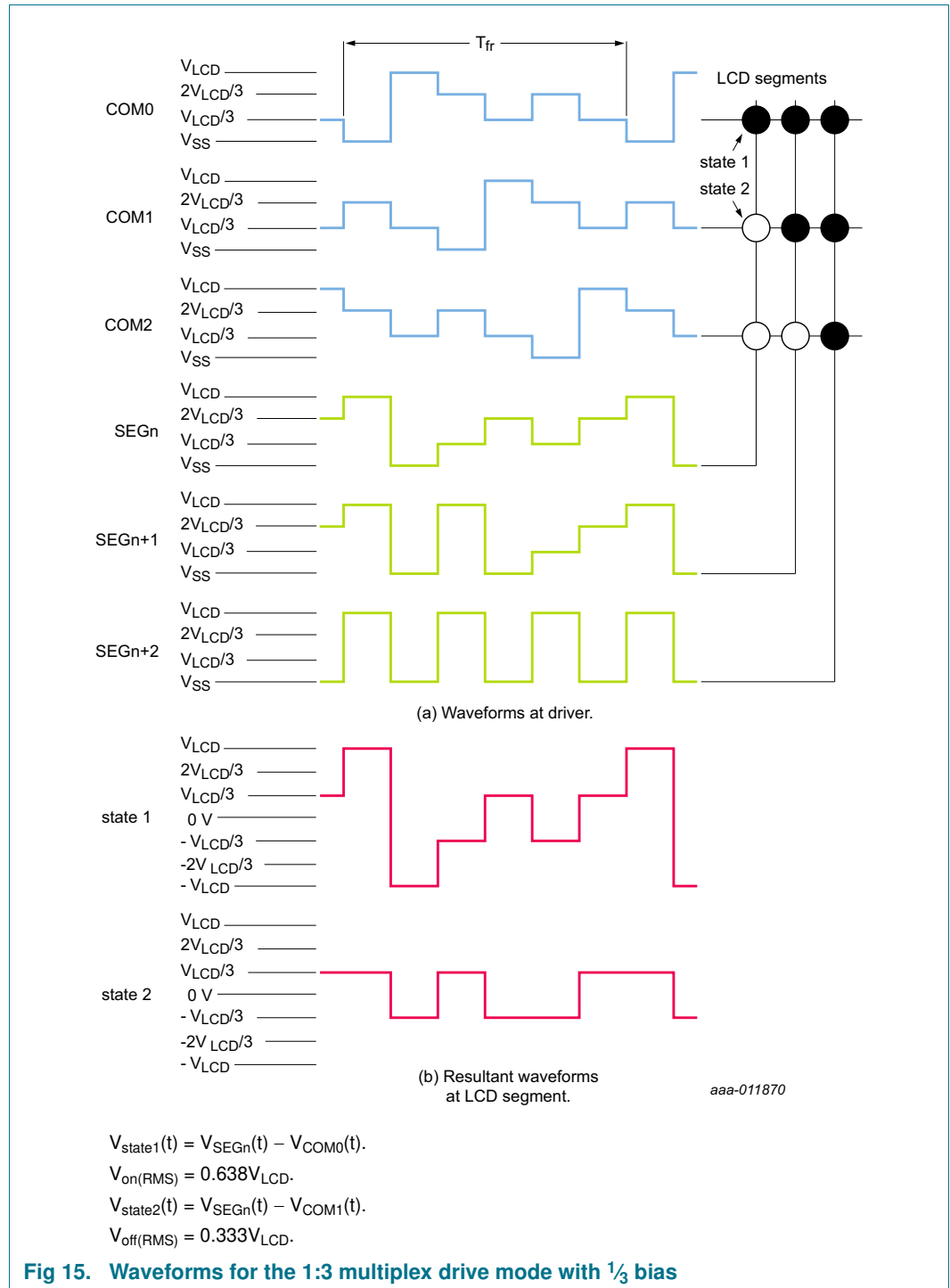
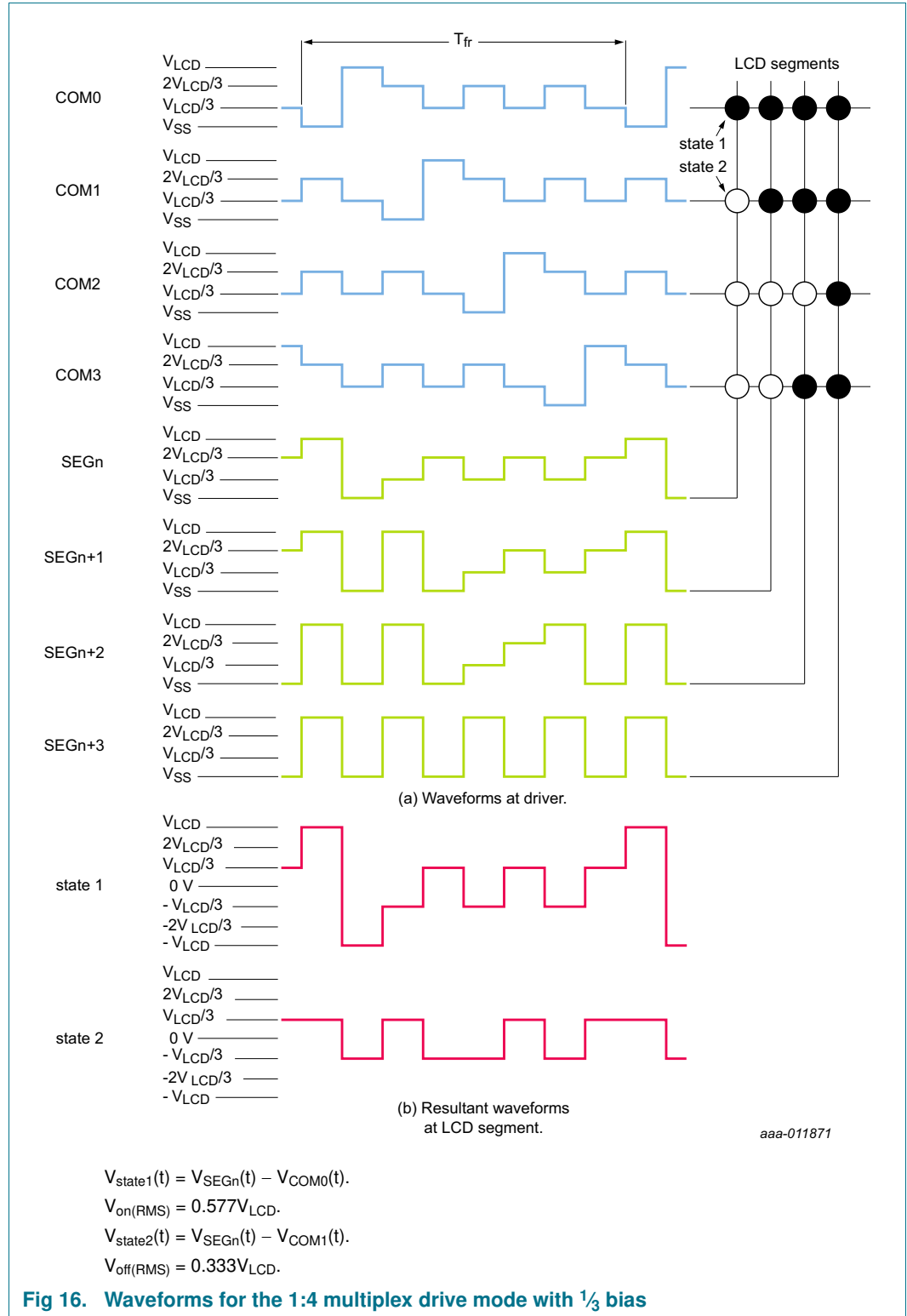


Fig 15. Waveforms for the 1:3 multiplex drive mode with 1/3 bias

9.2.2.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 16.



## 9.3 Backplane and segment outputs

### 9.3.1 Backplane outputs

The LCD drive section includes four backplane outputs COM0 to COM3, which must be directly connected to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, COM3 carries the same signal as COM1, therefore these two outputs can be tied together to give enhanced drive capabilities
- In 1:2 multiplex drive mode, COM0 and COM2, respectively, COM1 and COM3 all carry the same signals and may also be paired to increase the drive capabilities
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements

### 9.3.2 Segment outputs

The LCD drive section includes 18 segment outputs SEG0 to SEG17, which must be directly connected to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display registers. When less than 18 segment outputs are required, the unused segment outputs must be left open-circuit.



## 10. Power Sequencing

### 10.1 Power-on

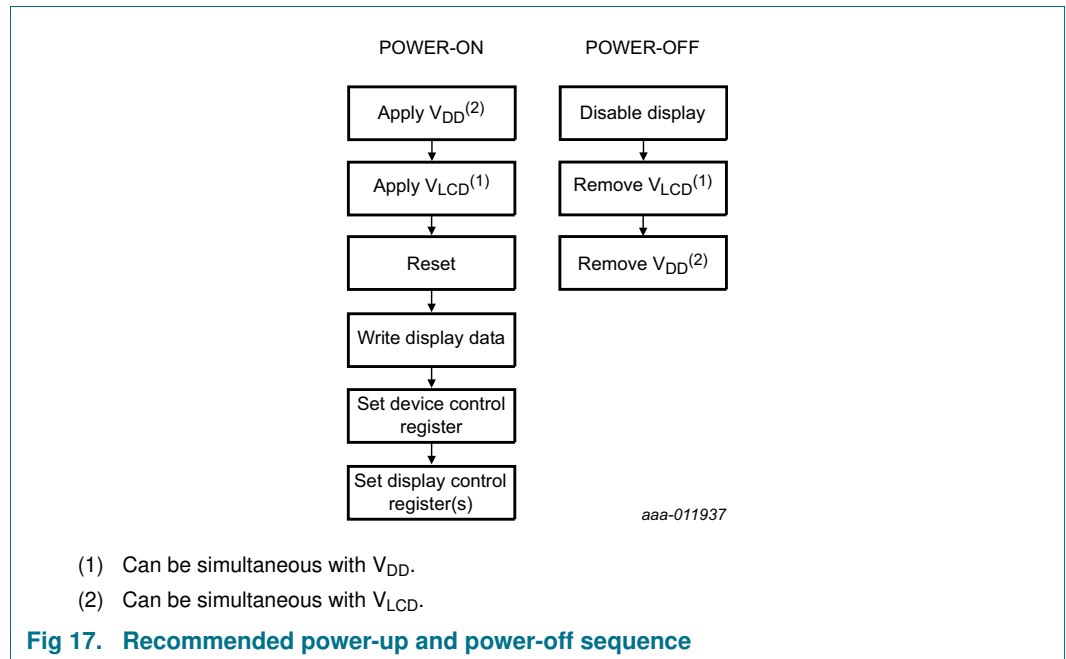
To avoid unwanted artifacts on the display,  $V_{LCD}$  must never be asserted before  $V_{DD}$ , it is permitted to assert  $V_{DD}$  and  $V_{LCD}$  at the same time.

### 10.2 Power-off

Before turning the power to the device off, the display must be disabled by setting bit DE to logic 0. To avoid unwanted artifacts on the display,  $V_{LCD}$  must never be connected, while  $V_{DD}$  is switched off. It is permitted to switch off  $V_{DD}$  and  $V_{LCD}$  simultaneously.

### 10.3 Power sequences

[Figure 17](#) depicts the recommended power-up and power-off sequence.



## 11. Bus interfaces

### 11.1 I<sup>2</sup>C-bus interface of the PCA8561A

The I<sup>2</sup>C-bus is for bidirectional, two-line communication between different ICs. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. Both data and clock lines remain HIGH when the bus is not busy. The PCA8561 acts as a slave receiver when being written to and as a slave transmitter when being read from.

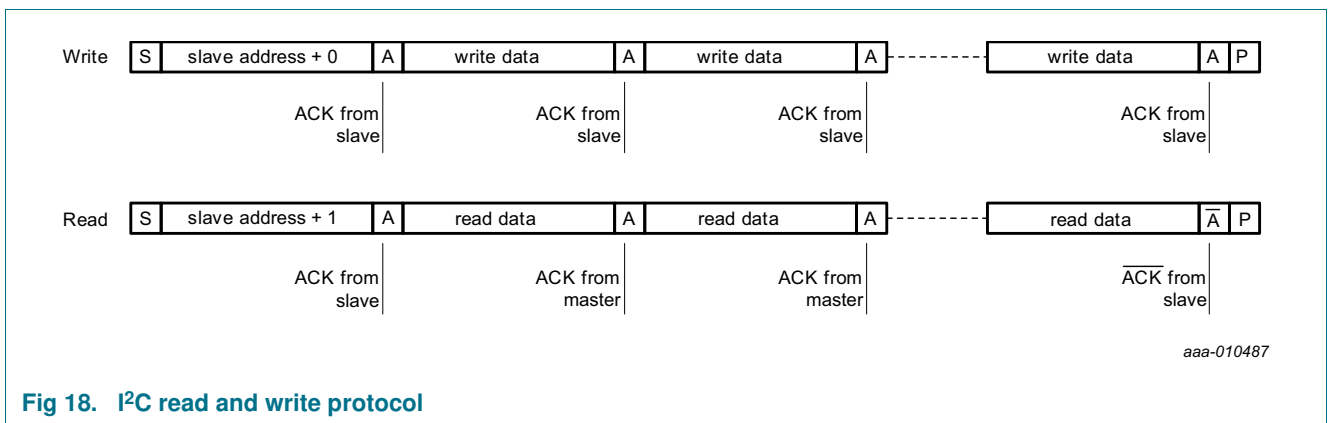


Fig 18. I<sup>2</sup>C read and write protocol

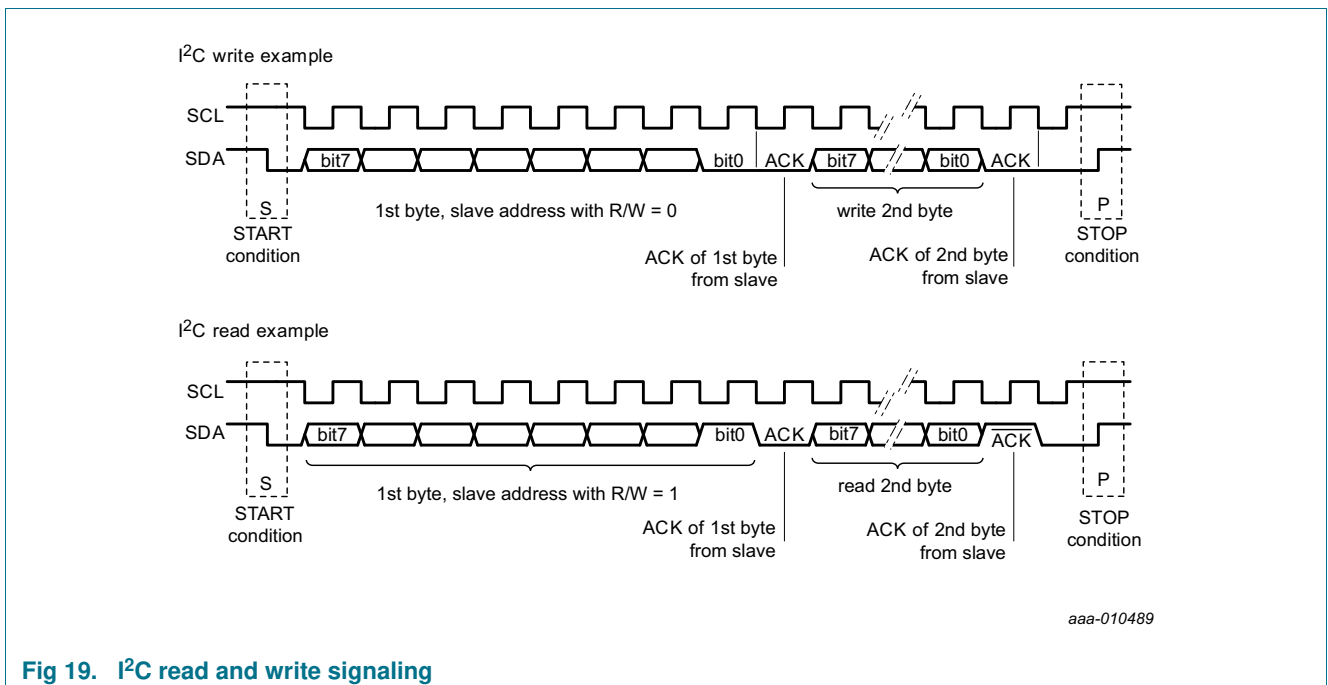


Fig 19. I<sup>2</sup>C read and write signaling

#### 11.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as STOP or START conditions.