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PCA8576C

Automotive LCD driver for low multiplex rates

Rev. 3 — 8 April 2015

Product data sheet

1. General description

The PCA8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)¹ with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCA8576C is compatible with most microcontrollers and communicates via the two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing and by hardware subaddressing.

For a selection of NXP LCD segment drivers, see [Table 21 on page 45](#).

2. Features and benefits

- AEC-Q100 compliant for automotive applications
- Single-chip LCD controller and driver
- 40 segment drives:
 - ◆ Up to twenty 7-segment alphanumeric characters
 - ◆ Up to ten 14-segment alphanumeric characters
 - ◆ Any graphics of up to 160 elements
- Versatile blinking modes
- No external components required (even in multiple device applications)
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, 1/2, or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Wide logic LCD supply range:
 - ◆ From 2 V for low-threshold LCDs
 - ◆ Up to 6 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- May be cascaded for large LCD applications (up to 2560 segments possible)
- No external components
- Separate or combined LCD and logic supplies
- Optimized pinning for plane wiring in both and multiple PCA8576C applications
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 19](#).



3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
PCA8576CT	VSO56	plastic very small outline package, 56 leads	SOT190-1

3.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA8576CH/Q900/1	935290244157	PCA8576CH/Q900,157	1	tray pack
	935290244118	PCA8576CH/Q900/1,1	1	tape and reel, 13 inch
PCA8576CT/Q900/1	935301673518	PCA8576CT/Q900/1Y	1	tape and reel, 13 inch

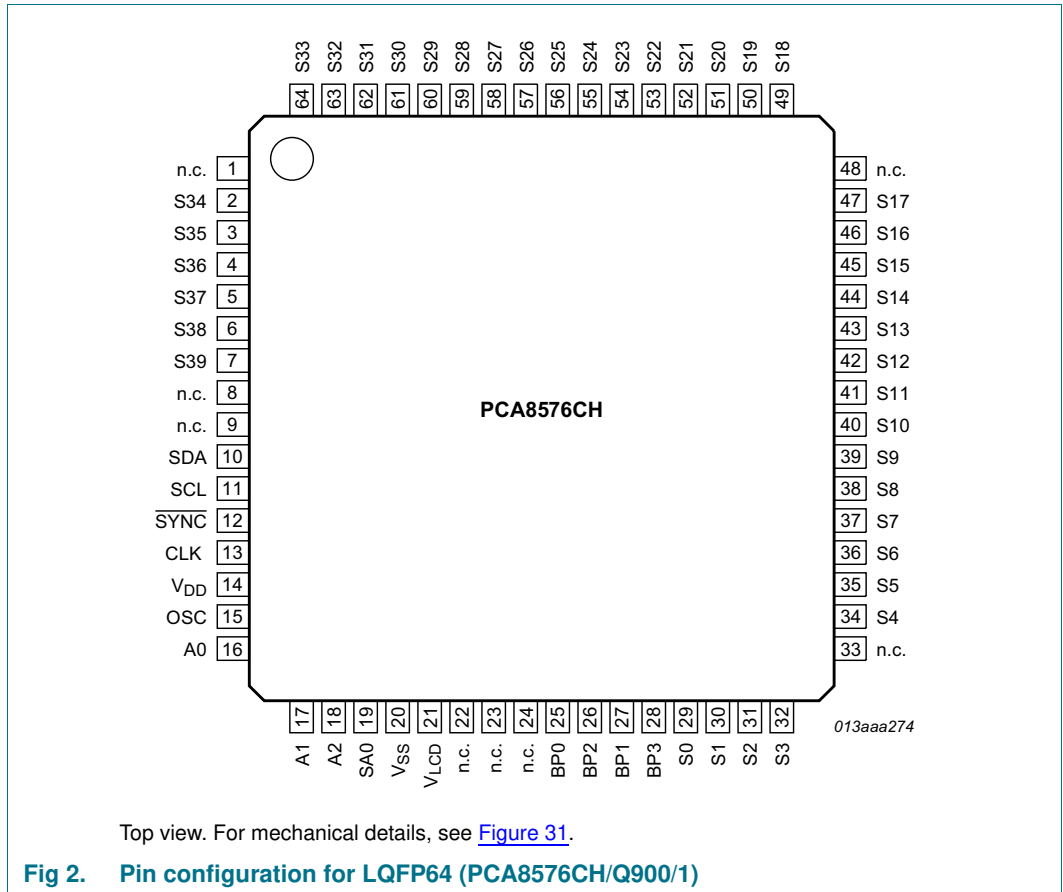
4. Marking

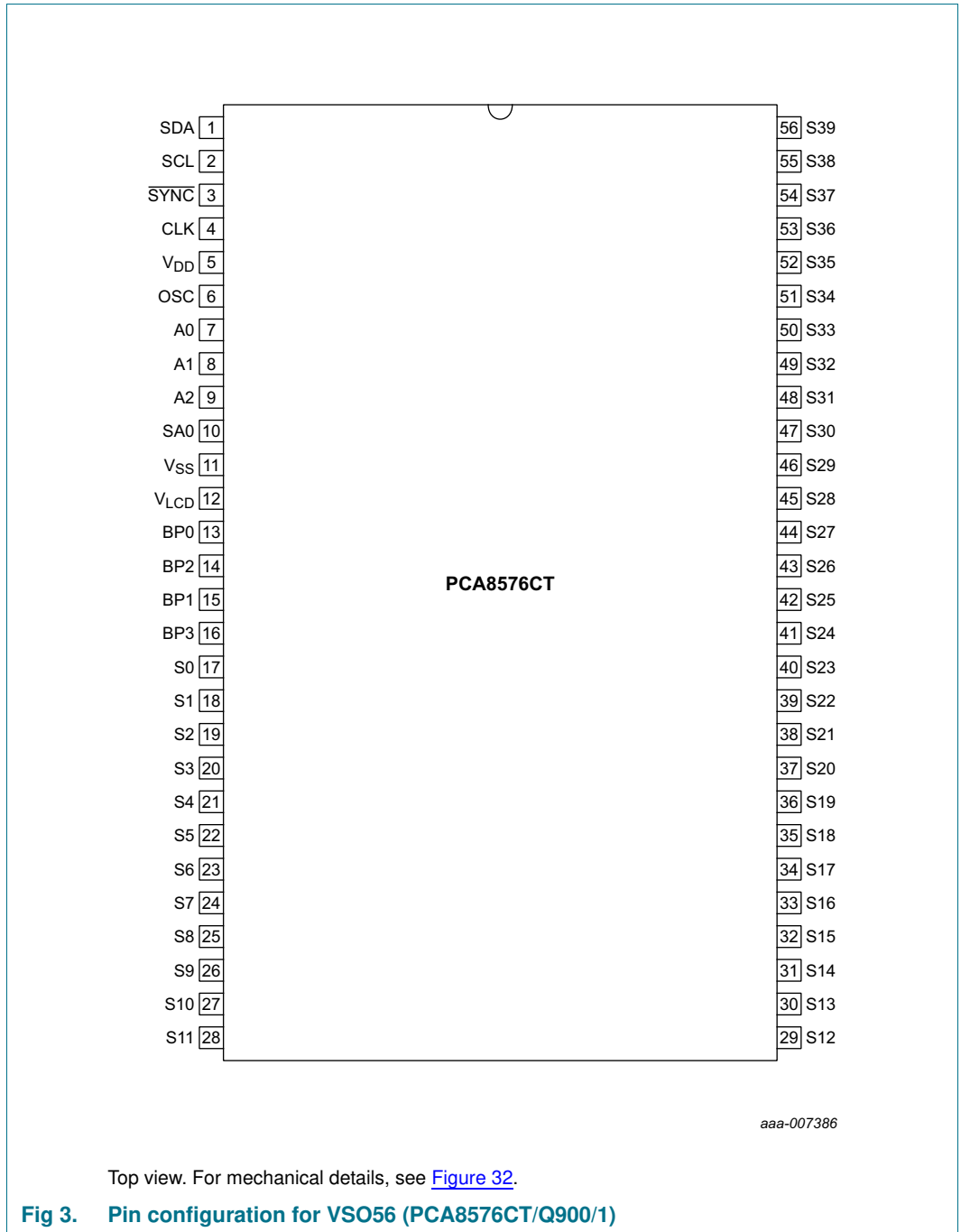
Table 3. Marking codes

Type number	Marking code
PCA8576CH/Q900/1	PCA8576CQ900
PCA8576CT/Q900/1	PCA8576CT/Q

6. Pinning information

6.1 Pinning





6.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin			Description
	LQFP64 (PCA8576CH/Q900/1)	VSO56 (PCA8576CT)	Type	
SDA	10	1	input/output	I ² C-bus serial data input and output
SCL	11	2	input	I ² C-bus serial clock input
SYNC	12	3	input/output	cascade synchronization input and output
CLK	13	4	input/output	external clock input/output
V _{DD}	14	5	supply	supply voltage
OSC	15	6	input	internal oscillator enable input
A0 to A2	16 to 18	7 to 9	input	subaddress inputs
SA0	19	10	input	I ² C-bus address input; bit 0
V _{SS}	20	11	supply	ground supply voltage
V _{LCD}	21	12	supply	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	13 to 16	output	LCD backplane outputs
S0 to S39	2 to 7, 29 to 32, 34 to 47, 49 to 64	17 to 56	output	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	-	not connected; do not connect and do not use as feed through

7. Functional description

The PCA8576C is a versatile peripheral device designed to interface between any microprocessor or microcontroller to a wide variety of LCD segment or dot matrix displays (see [Figure 4](#)). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

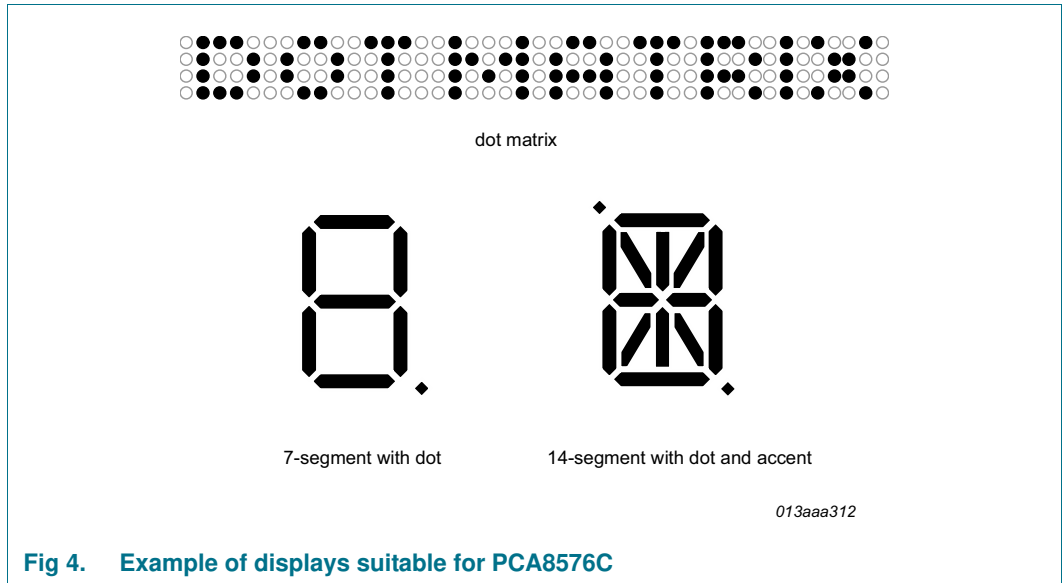


Fig 4. Example of displays suitable for PCA8576C

The possible display configurations of the PCA8576C depend on the number of active backplane outputs required. A selection of display configurations is shown in [Table 5](#). All of these configurations can be implemented in the typical system shown in [Figure 5](#).

Table 5. Selection of possible display configurations

Number of				
Backplanes	Icons	Digits/Characters		Dot matrix/ Elements
		7-segment	14-segment	
4	160	20	10	160 dots (4 × 40)
3	120	15	7	120 dots (3 × 40)
2	80	10	5	80 dots (2 × 40)
1	40	5	2	40 dots (1 × 40)

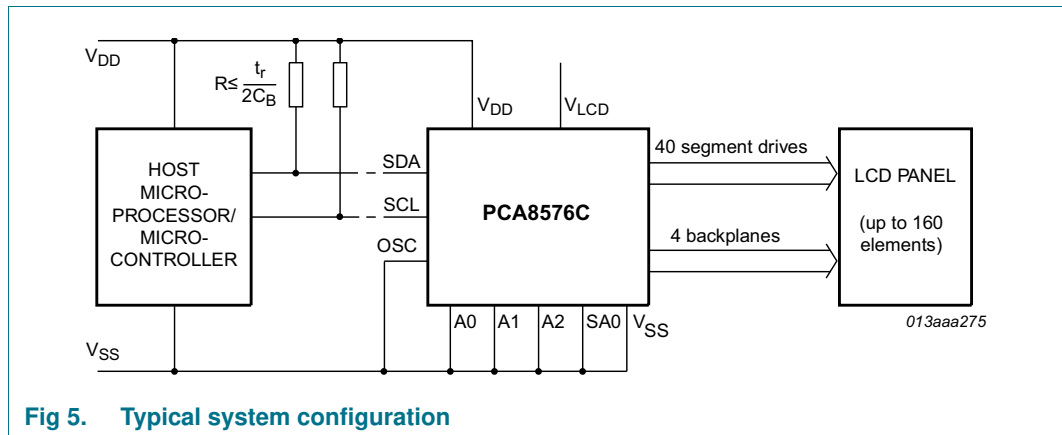


Fig 5. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the PCA8576C.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (pins V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-On-Reset (POR)

At power-on the PCA8576C resets to the following starting conditions:

- All backplane and segment outputs are set to V_{DD}
- The selected drive mode is 1:4 multiplex with 1/3 bias
- Blinking is switched off
- Input and output bank selectors are reset (as defined in [Table 9](#))
- The I²C-bus interface is initialized
- The data pointer and the subaddress counter are cleared

Remark: Do not transfer data on the I²C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

The full-scale LCD voltage (V_{oper}) is obtained from V_{DD} – V_{LCD}. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin V_{LCD}.

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three series resistors connected between V_{DD} and V_{LCD}. The center resistor can be switched out of the circuit to provide a 1/2 bias voltage level for the 1:2 multiplex configuration.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in [Table 6](#).

Table 6. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for $\frac{1}{2}$ bias

a = 2 for $\frac{1}{3}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with [Equation 1](#):

$$V_{on(RMS)} = V_{LCD} \sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \tag{1}$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with [Equation 2](#):

$$V_{off(RMS)} = V_{LCD} \sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \tag{2}$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from [Equation 3](#):

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \tag{3}$$

Using [Equation 3](#), the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3} \right] = 2.309V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when $\frac{1}{3}$ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see [Figure 6](#). For a good contrast performance, the following rules should be followed:

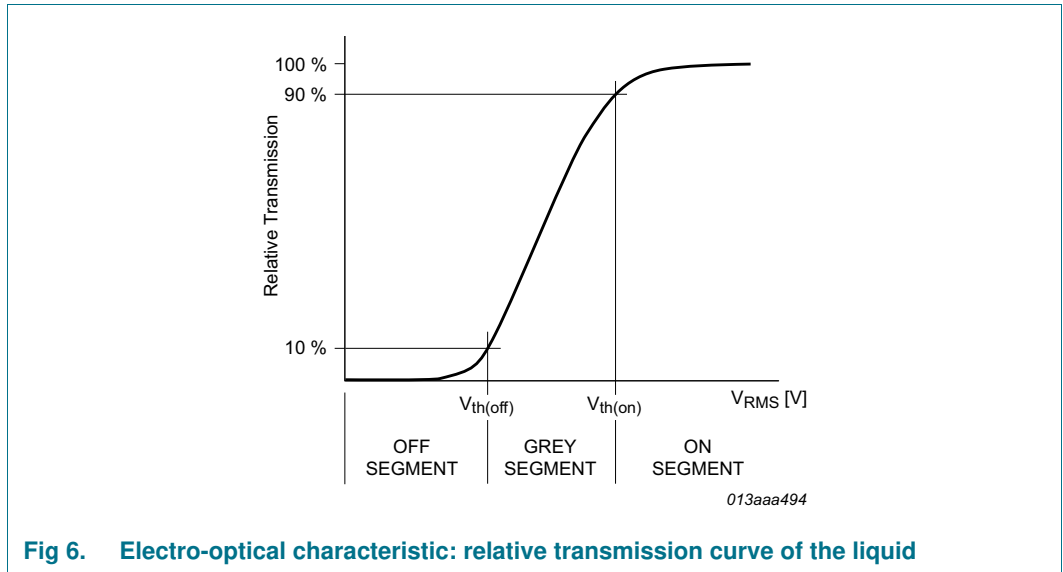
$$V_{on(RMS)} \geq V_{th(on)} \tag{4}$$

$$V_{off(RMS)} \leq V_{th(off)} \tag{5}$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a (see [Equation 1](#)), n (see [Equation 3](#)), and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th} . $V_{th(on)}$ is sometimes named saturation voltage V_{sat} .

It is important to match the module properties to those of the driver in order to achieve optimum performance.



7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in [Figure 7](#).

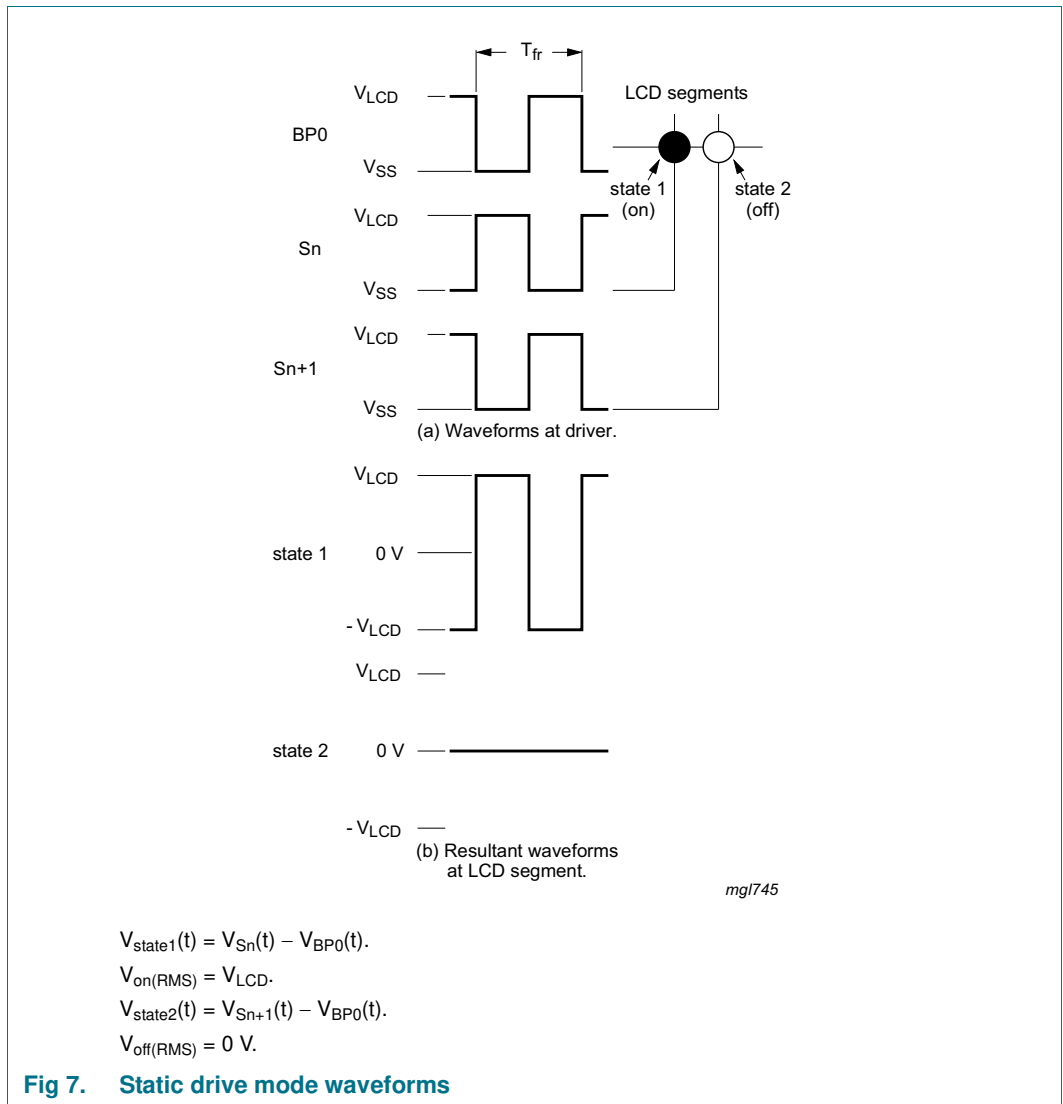
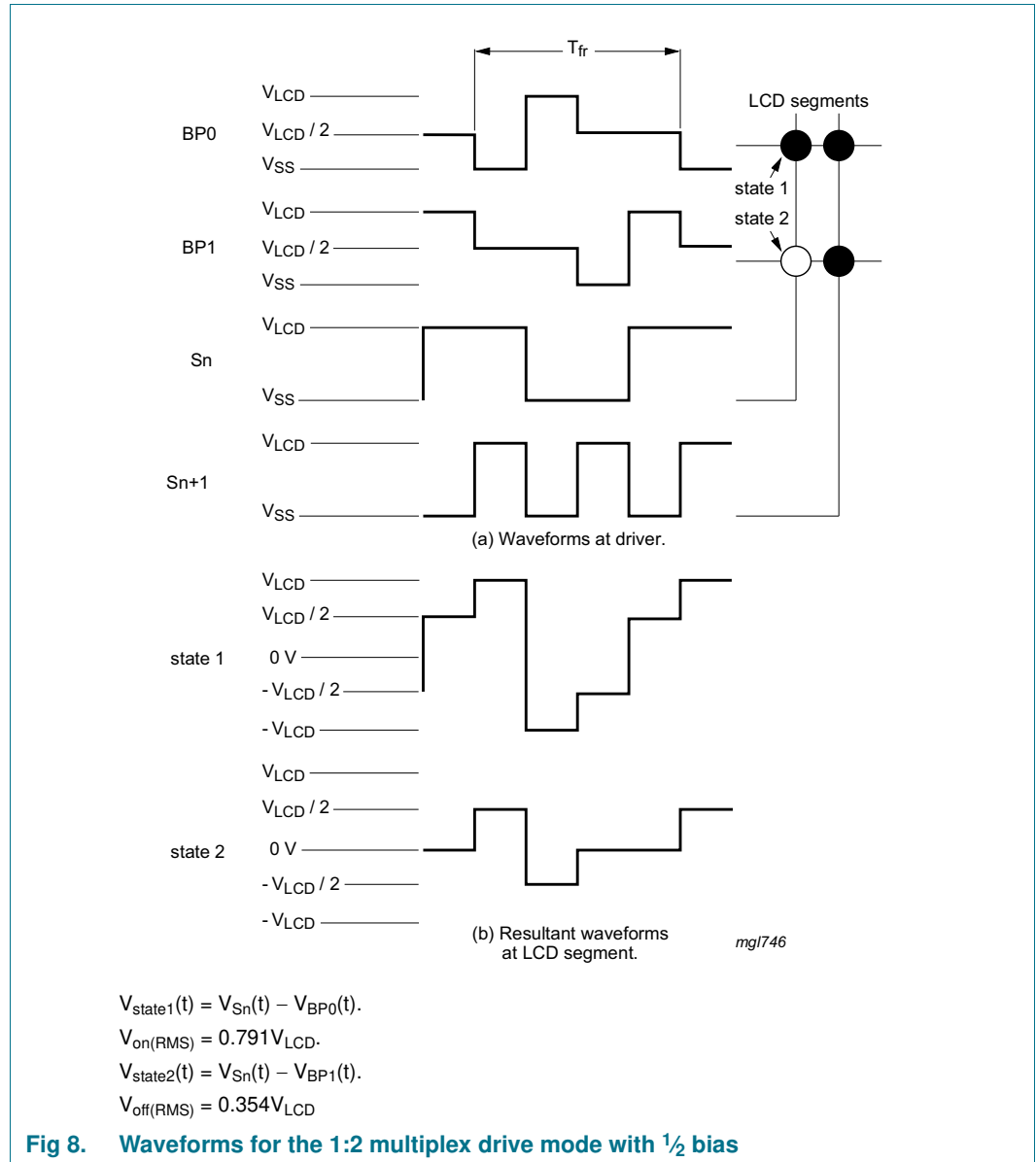
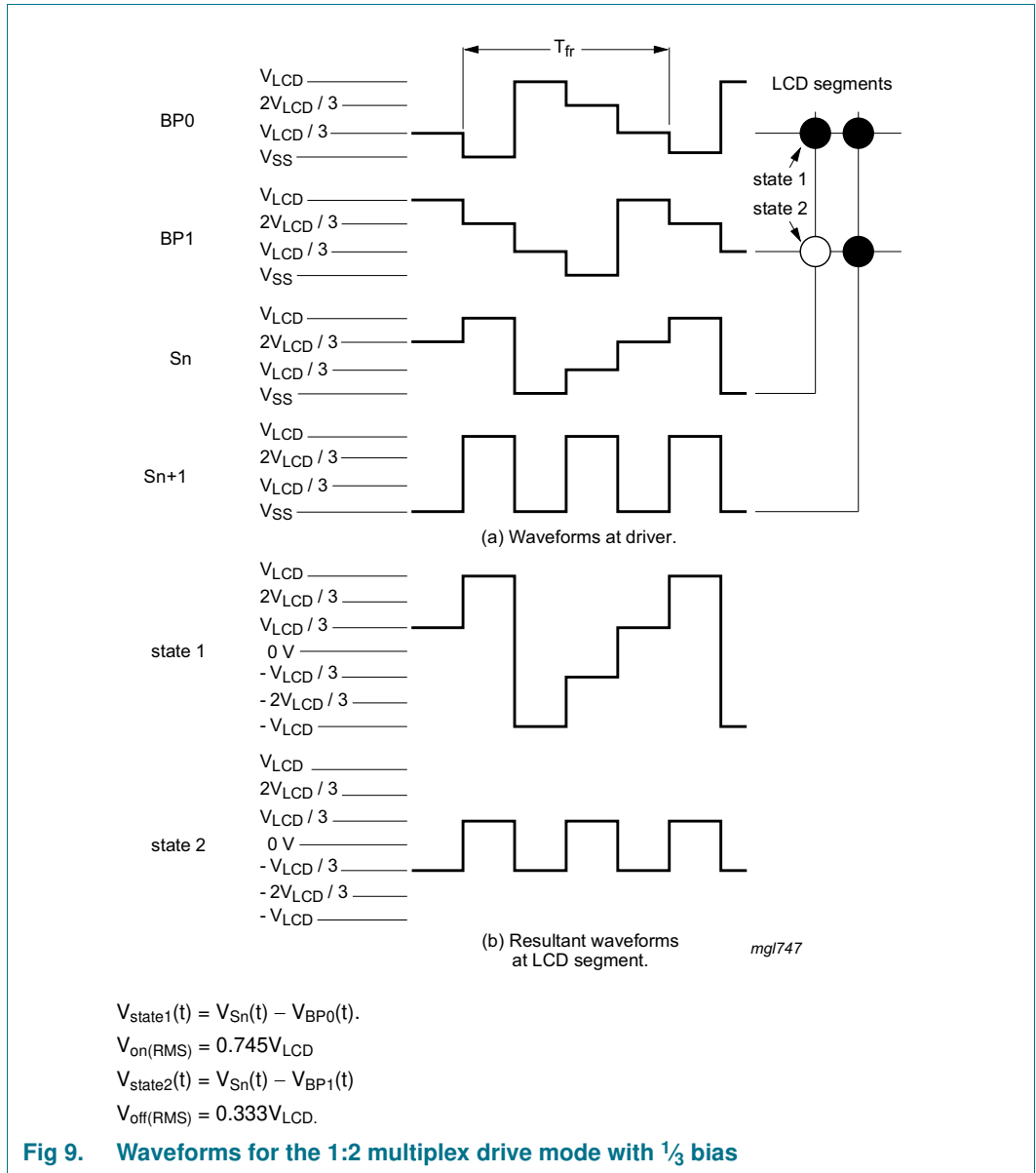


Fig 7. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

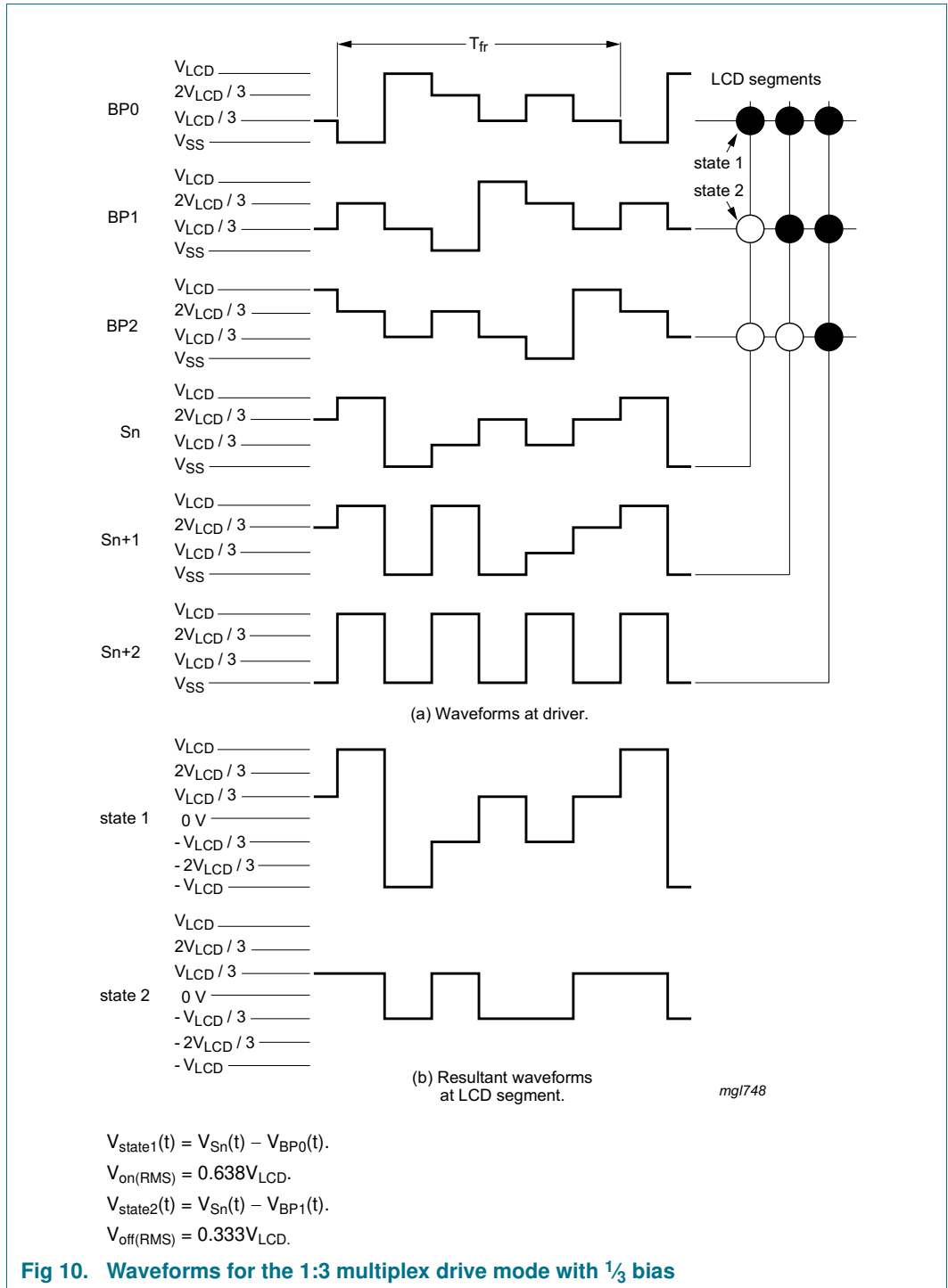
When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA8576C allows the use of 1/2 bias or 1/3 bias (see Figure 8 and Figure 9).





7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in [Figure 10](#).



7.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 11.

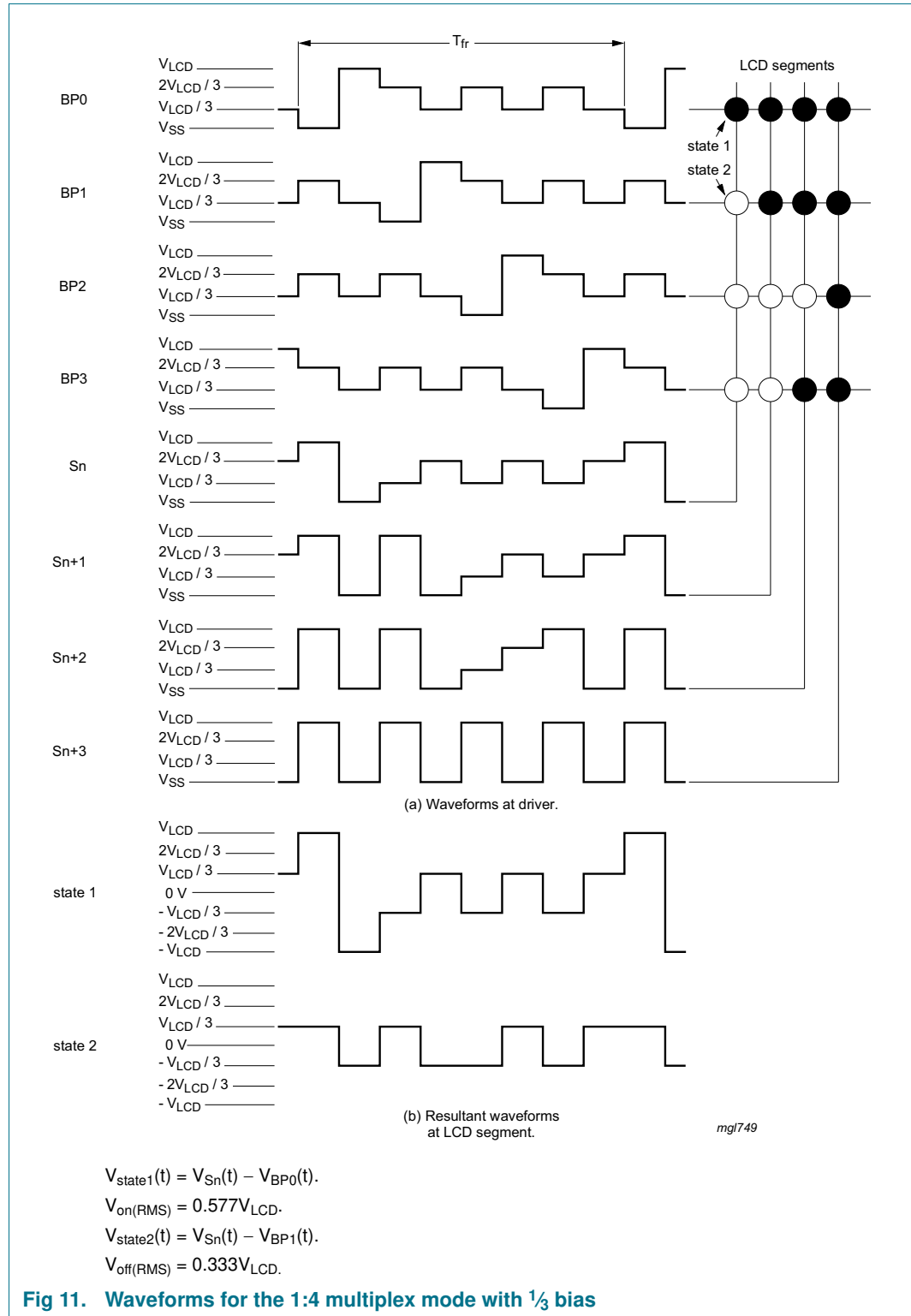


Fig 11. Waveforms for the 1:4 multiplex mode with 1/3 bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCA8576C are timed by the frequency f_{clk} , which equals either the built-in oscillator frequency f_{osc} or the external clock frequency $f_{clk(ext)}$.

The clock frequency (f_{clk}) determines the LCD frame frequency (f_{fr}) and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case, the output from pin CLK is the clock signal for any cascaded PCA8576C in the system.

7.5.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK then becomes the external clock input.

Remark: A clock signal must always be supplied to the device. Removing the clock, freezes the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing

The timing of the PCA8576C sequences the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal (SYNC) maintains the correct timing relationship between the PCA8576Cs in the system. The timing also generates the LCD frame frequency which is derived as an integer division of the clock frequency (see [Table 7](#)). The frame frequency is set by the mode-set command (see [Table 10](#)) when an internal clock is used or by the frequency applied to the pin CLK when an external clock is used.

Table 7. LCD frame frequencies [1]

PCA8576C mode	Frame frequency	Nominal frame frequency (Hz)
Normal-power mode	$f_{fr} = \frac{f_{clk}}{2880}$	69 [2]
Power-saving mode	$f_{fr} = \frac{f_{clk}}{480}$	65 [3]

[1] The possible values for f_{clk} see [Table 17](#).

[2] For $f_{clk} = 200$ kHz.

[3] For $f_{clk} = 31$ kHz.

The ratio between the clock frequency and the LCD frame frequency depends on the power mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power consumption.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus. When a device is unable to process a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.8 Shift register

The shift register transfers display information from the display RAM to the display register while previous data is displayed.

7.9 Segment outputs

The LCD drive section includes 40 segment outputs, S0 to S39, which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.10 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left as an open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.11 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte																																																									
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x = data bit unchanged.

Fig 13. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

7.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see [Table 11](#)). After this, the data byte is stored starting at the display RAM address indicated by the data pointer (see [Figure 13](#)). Once each byte is stored, the data pointer is automatically incremented based on the selected LCD configuration.

The contents of the data pointer are incremented as follows:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I²C-bus data access terminates early, the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

7.13 Sub-address counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter match with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device-select command (see [Table 12](#)). If the contents of the subaddress counter and the hardware subaddress do not match then data storage is blocked but the data pointer will be incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCA8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

7.14 Bank selector

7.14.1 Output bank selector

The output bank selector (see [Table 13](#)), selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode: all RAM addresses of row 0 are selected, followed sequentially by the contents of row 1, row 2, and then row 3.
- In 1:3 multiplex mode: rows 0, 1, and 2 are selected sequentially.
- In 1:2 multiplex mode: rows 0 and 1 are selected.
- In the static mode: row 0 is selected.

The PCA8576C includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In 1:2 multiplex drive mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This enables preparation of display information in an alternative bank and the ability to switch to it once it has been assembled.

7.14.2 Input bank selector

The input bank selector (see [Table 13](#)) loads display data into the display RAM based on the selected LCD drive configuration. Using the bank-select command, display data can be loaded in row 2 into static drive mode or in rows 2 and 3 into 1:2 multiplex drive mode. The input bank selector functions independently of the output bank selector.

7.15 Blinking

The display blinking capabilities of the PCA8576C are very versatile. The whole display can be blinked at frequencies selected by the blink-select command. The blinking frequencies are integer fractions of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating (see [Table 8](#)).

Table 8. Blink frequencies

Blinking mode	Normal-power mode ratio	Power-saving mode ratio	Blink frequency
off	-	-	blinking off
1	$f_{blink} = \frac{f_{clk}}{92160}$	$f_{blink} = \frac{f_{clk}}{15360}$	2 Hz
2	$f_{blink} = \frac{f_{clk}}{184320}$	$f_{blink} = \frac{f_{clk}}{30720}$	1 Hz
3	$f_{blink} = \frac{f_{clk}}{368640}$	$f_{blink} = \frac{f_{clk}}{61440}$	0.5 Hz

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. Using the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the blink-select command (see [Table 14](#)).

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

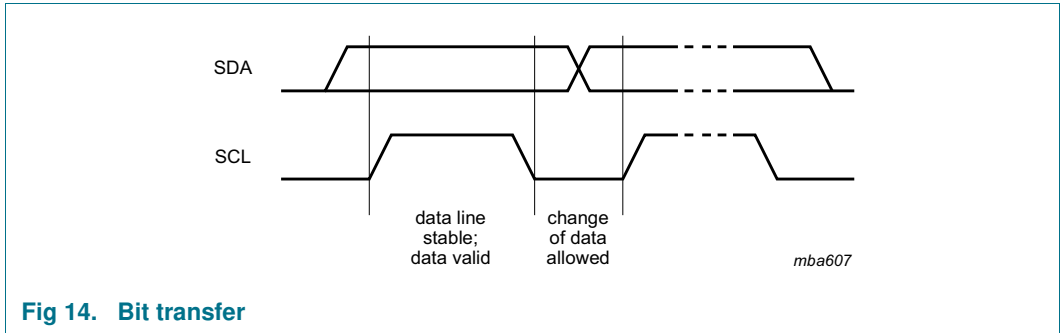
If the entire display needs to be blinked at a frequency other than the nominal blink frequency, this can be done using the mode-set command to set and reset the display enable bit E at the required rate (see [Table 10](#)).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DATA line (SDA) and a Serial CLOCK line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

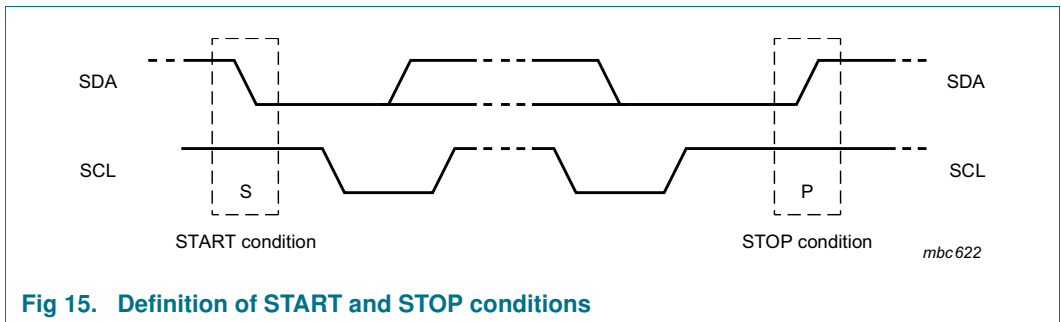
7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in [Figure 14](#).



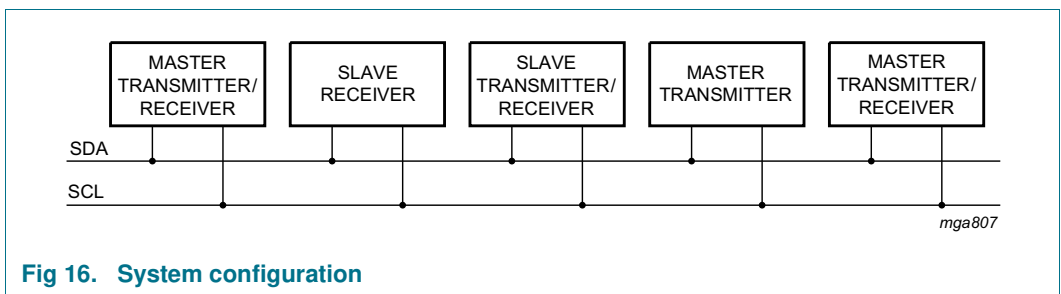
7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in [Figure 15](#).



7.16.3 System configuration

A device generating a message is a transmitter and a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is illustrated in [Figure 16](#).



7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is illustrated in [Figure 17](#).

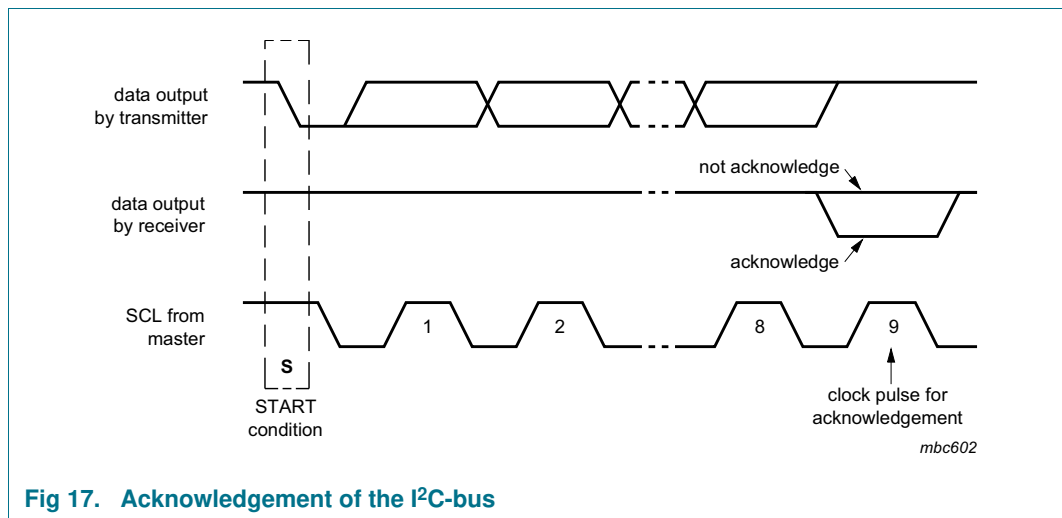


Fig 17. Acknowledgement of the I²C-bus

7.16.5 PCA8576C I²C-bus controller

The PCA8576C acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCA8576C are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, the transferred command data and the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCA8576C is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCA8576C forces the SCL line LOW until its internal operations are completed. This is known as the clock synchronization feature of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.16.6 Input filter

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.17 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCA8576C. The least significant bit of the slave address that a PCA8576C responds to is defined by the level tied at its input SA0. Therefore, two types of PCA8576C can be distinguished on the same I²C-bus which allows:

- Up to 16 PCA8576Cs on the same I²C-bus for very large LCD applications.
- The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in [Figure 18](#). The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCA8576C slave addresses available. All PCA8576Cs with the corresponding SA0 level acknowledge in parallel with the slave address but all PCA8576Cs with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes follow which define the status of the addressed PCA8576Cs.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCA8576Cs on the bus.

After the last command byte, a series of display data bytes may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCA8576C device. The acknowledgement after each byte is made only by the (A0, A1, and A2) addressed PCA8576C. After the last display byte, the I²C-bus master issues a STOP condition (P).

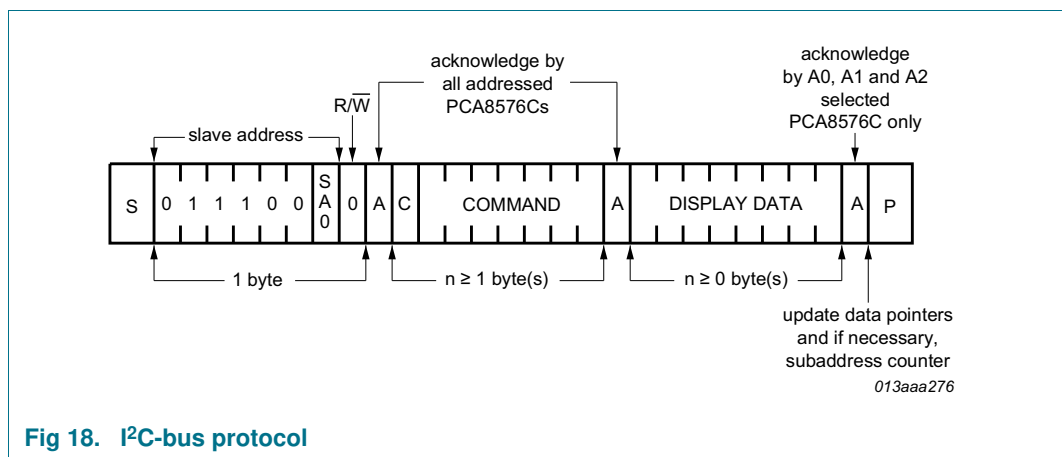


Fig 18. I²C-bus protocol