Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PCA8576D

Automotive 40 x 4 LCD segment driver for low multiplex rates up to 1:4

Rev. 2 — 6 June 2013 Product data sheet

1. General description

The PCA8576D is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCA8576D is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

2. Features and benefits

- AEC-Q100 compliant for automotive applications
- Single chip LCD controller and driver
- Selectable backplane drive configuration: static or 2, 3, 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - Up to 20 7-segment numeric characters
  - Up to 10 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 6.5 V for high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components required
- Compatible with chip-on-glass and chip-on-board technology
- Manufactured in silicon gate CMOS process

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8576DU	bare die	59 bumps	PCA8576DU/2DA

3.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA8576DU/2DA/Q2	935294883026	PCA8576DU/2DA/Q2,0	1	chips with bumps in tray

4. Marking

Table 3. Marking codes

Product type number	Marking code
PCA8576DU/2DA/Q2	PC8576D-2

5. Block diagram

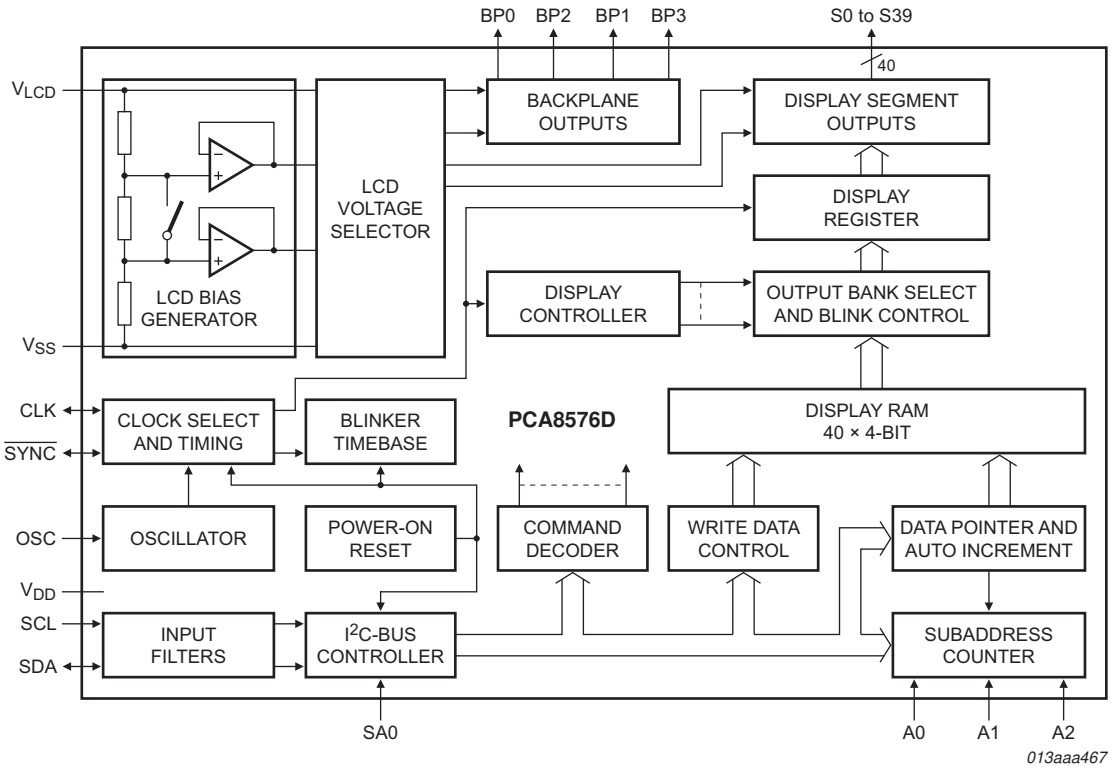
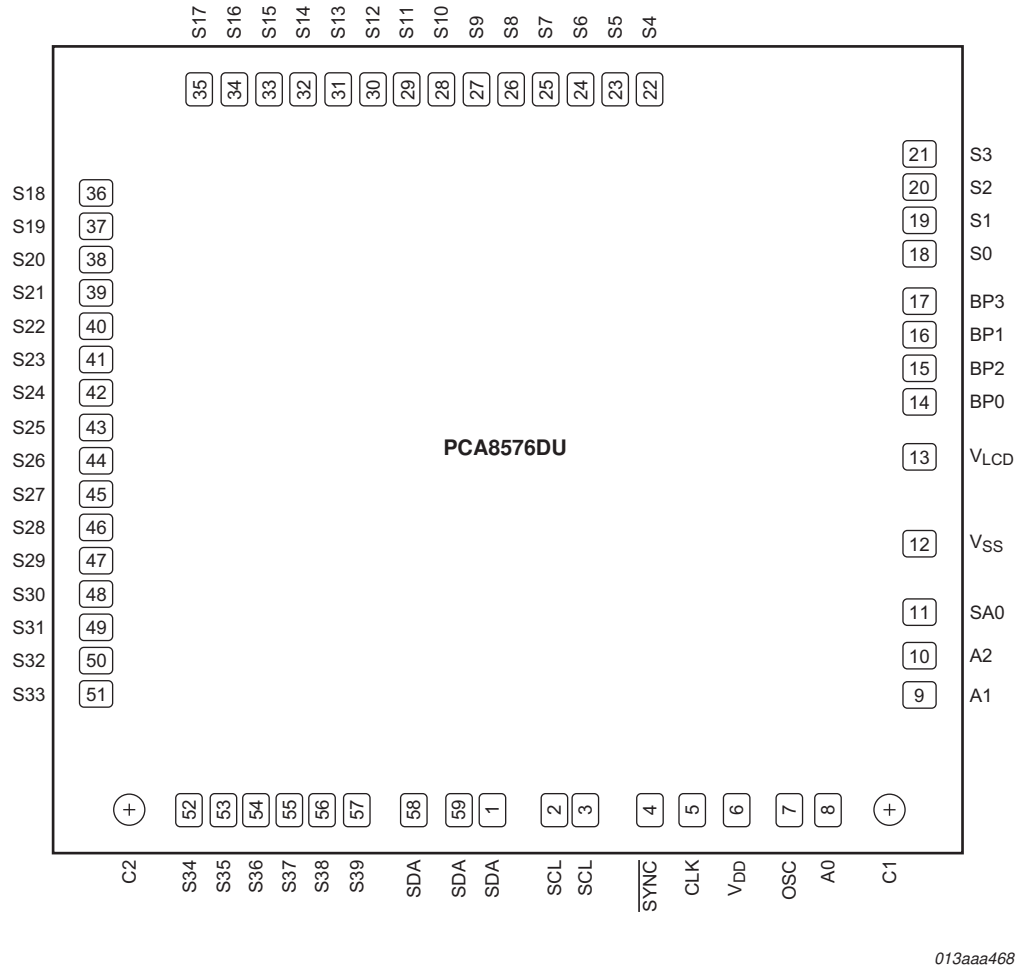


Fig 1. Block diagram of PCA8576D

6. Pinning information

6.1 Pinning



Viewed from active side. C1 and C2 are alignment marks. For mechanical details, see Figure 23.

Fig 2. Pinning diagram for PCA8576DU (bare die)

6.2 Pin description

Table 4. Pin description

Symbol	Pin PCA8576DU	Description
SDA	1, 58, 59	I^2C-bus serial data input and output
SCL	2, 3	I^2C-bus serial clock input
CLK	5	external clock input or output
V_{DD}	6	supply voltage
$\overline{SYNC}$	4	cascade synchronization input or output
OSC	7	internal oscillator enable input
A0 to A2	8 to 10	subaddress inputs
SA0	11	I^2C-bus address input; bit 0
V_{SS}	12[1]	ground supply voltage
V_{LCD}	13	LCD supply voltage
BP0, BP2, BP1, BP3	14 to 17	LCD backplane outputs
S0 to S39	18 to 57	LCD segment outputs

[1] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

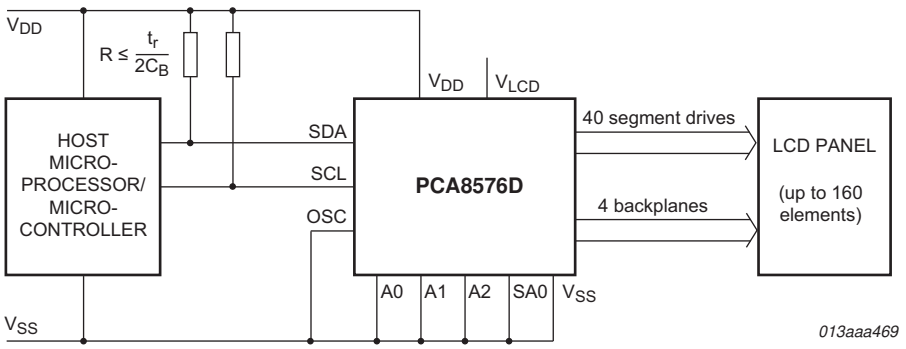
7. Functional description

The PCA8576D is a versatile peripheral device designed to interface any microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

The possible display configurations of the PCA8576D depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 5. All of these configurations can be implemented in the typical system shown in Figure 3.

Table 5. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment	**14-segment**	
4	160	20	10	160 (4 × 40)
3	120	15	7	120 (3 × 40)
2	80	10	5	80 (2 × 40)
1	40	5	2	40 (1 × 40)



The resistance of the power lines must be kept to a minimum.

For chip-on-glass applications, due to the Indium Tin Oxide (ITO) track resistance, each supply line must be routed separately between the chip and the connector.

Fig 3. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I^2C-bus communication channel with the PCA8576D. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

7.1 Power-on reset

At power-on the PCA8576D resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled (bit E = 0, see Table 11)

Data transfers on the I^2C-bus must be avoided for 1 ms following power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between V_{LCD} and V_{SS}. The middle resistor can be bypassed to provide a $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration. The LCD voltage can be temperature compensated externally using the supply to pin V_{LCD}.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command (see Table 11) from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 6.

Table 6. Discrimination ratios

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for $\frac{1}{2}$ bias

a = 2 for 1⁄3 bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (1)$$

where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 3 for 1:3 multiplex

n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with 1⁄2 bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with 1⁄2 bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (1⁄2 bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (1⁄2 bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3 V_{off(RMS)}$ when 1⁄3 bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at V_{low}) and the other at 90 % relative transmission (at V_{high}), see Figure 4. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{high} \quad (4)$$

$$V_{off(RMS)} \leq V_{low} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes just named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

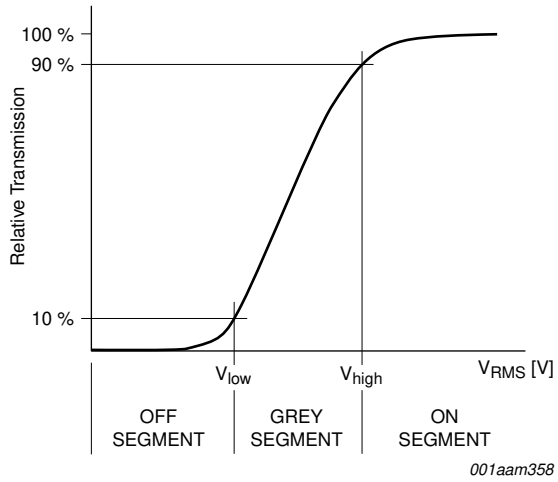
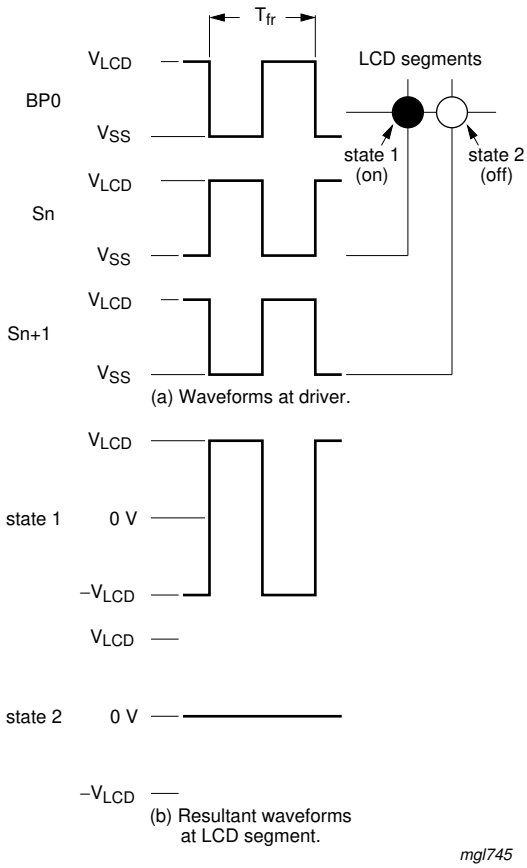


Fig 4. Electro-optical characteristic: relative transmission curve of the liquid

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (Sn) waveforms for this mode are shown in Figure 5.



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = V_{LCD}$.

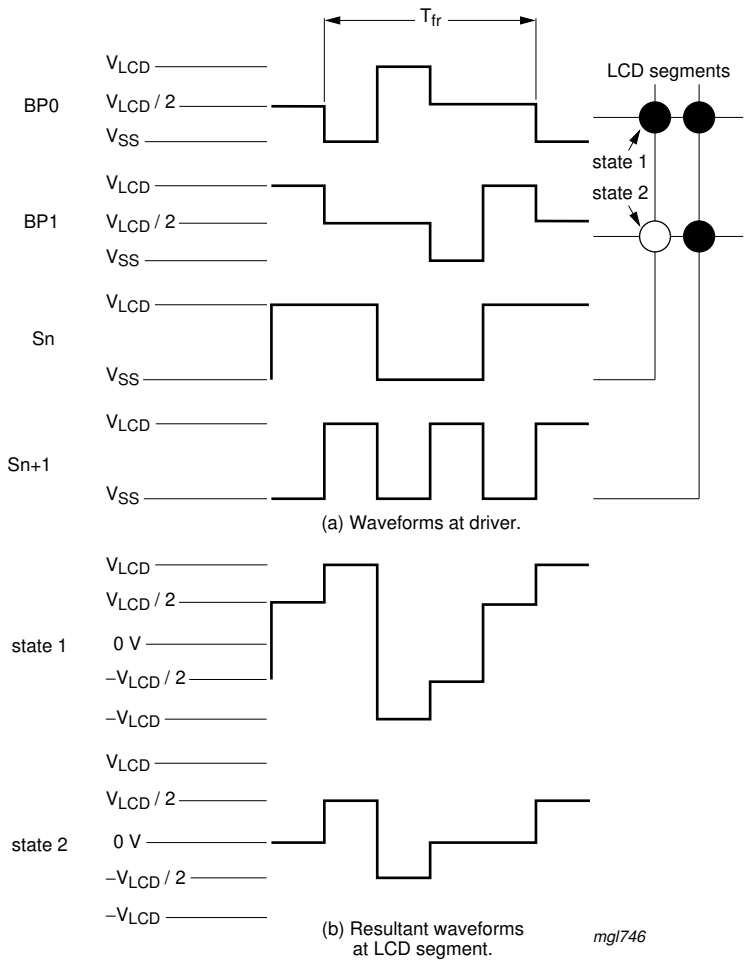
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

(4) $V_{off(RMS)} = 0$ V.

Fig 5. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

The 1:2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½ bias or ⅓ bias as shown in Figure 6 and Figure 7.



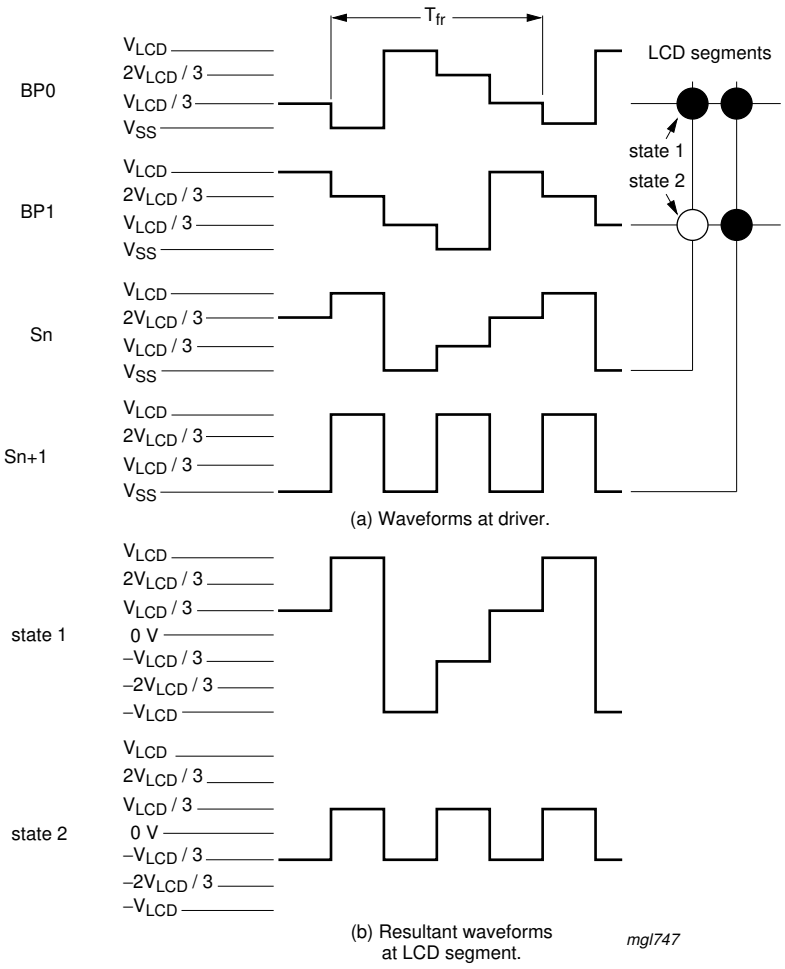
(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.791V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.354V_{LCD}$.

Fig 6. Waveforms for the 1:2 multiplex drive mode with ½ bias



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.745V_{LCD}$.

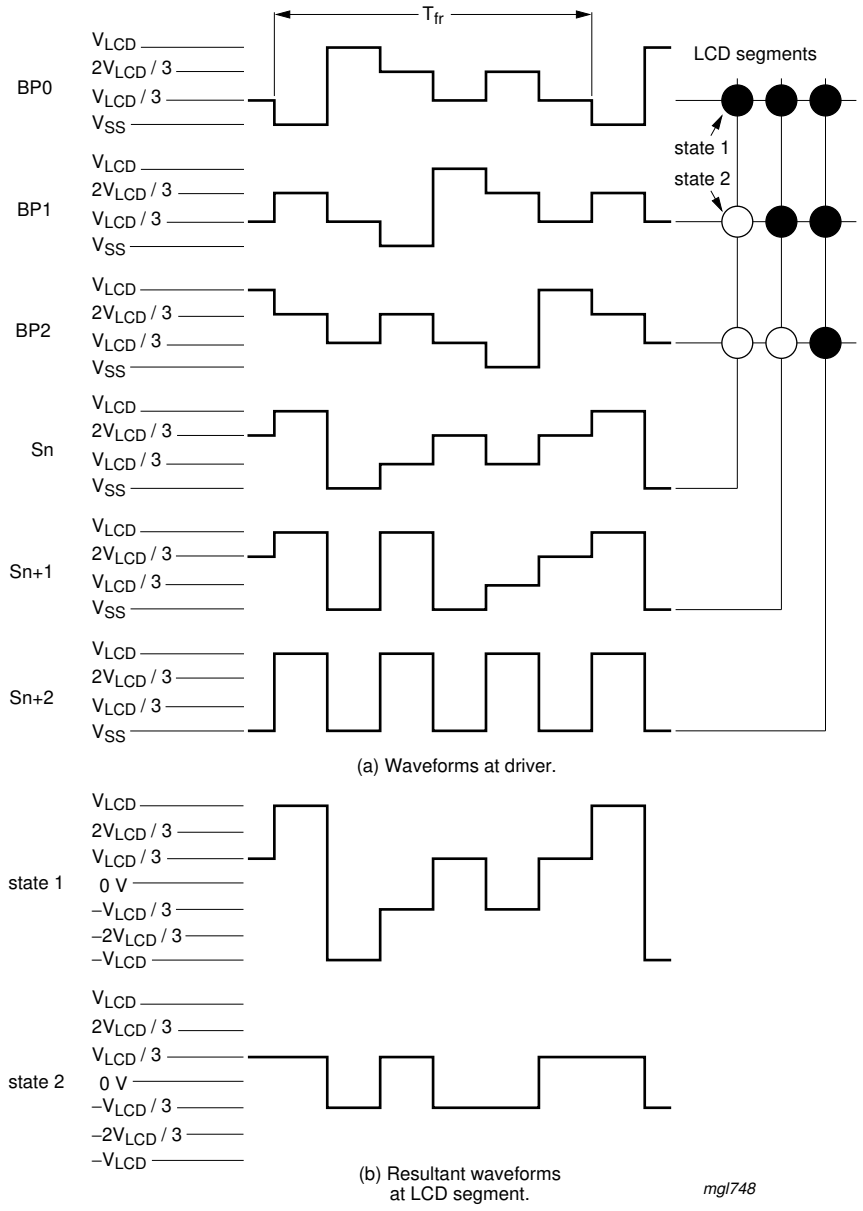
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies (see Figure 8).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.638V_{LCD}$.

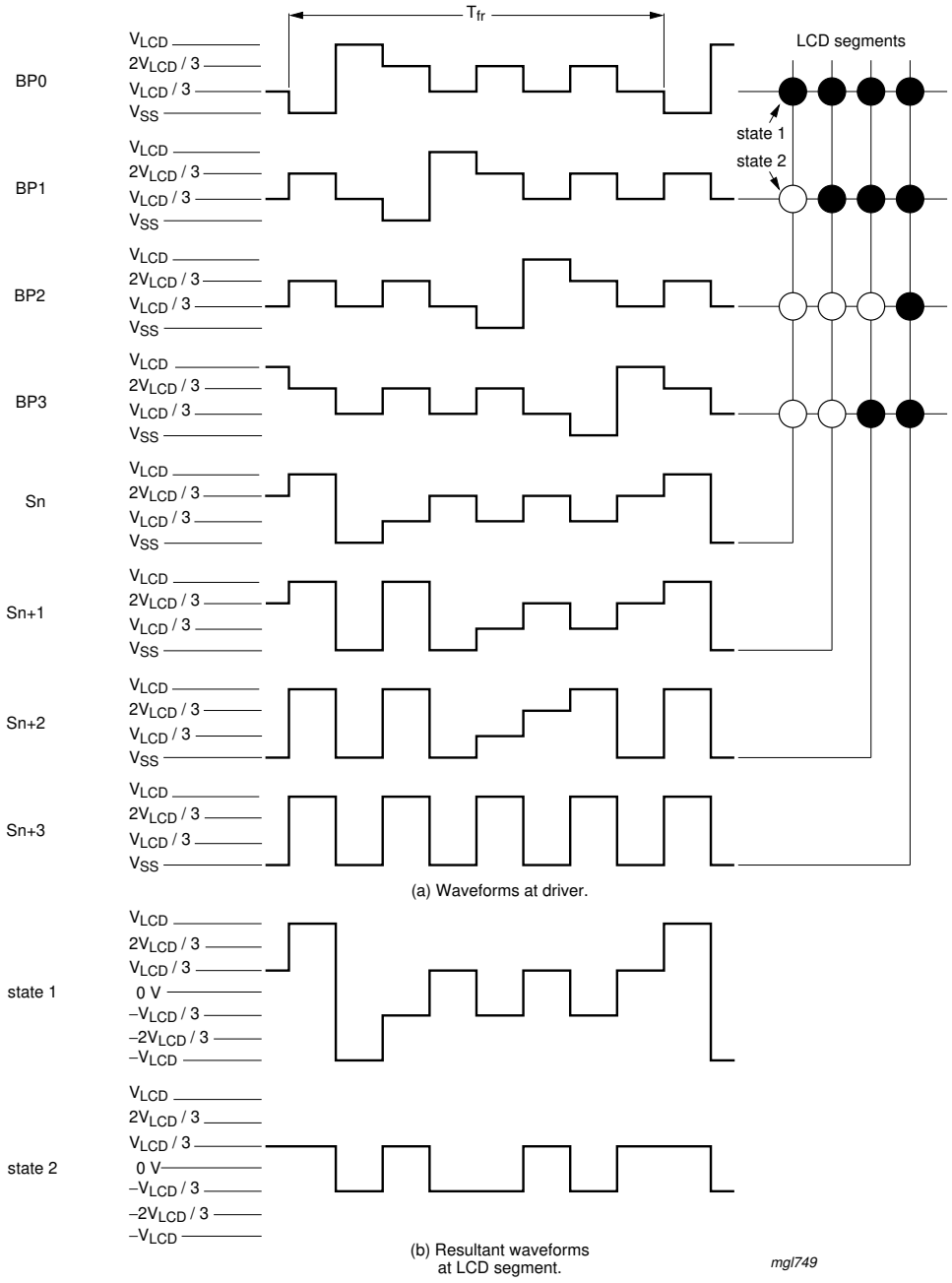
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies (see Figure 9).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.577V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:4 multiplex drive mode with 1/3 bias

7.5 Oscillator

7.5.1 Internal clock

The internal logic of the PCA8576D and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCA8576D in the system that are connected in cascade.

7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

The LCD frame signal frequency is determined by the clock frequency (f_{clk}).

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing

The PCA8576D timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCA8576D in the system is maintained by the synchronization signal at pin $\overline{SYNC}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$.

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs, and one column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

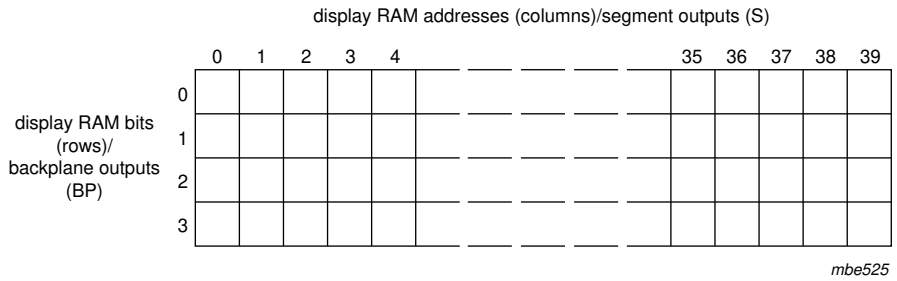
In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.

In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.

In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

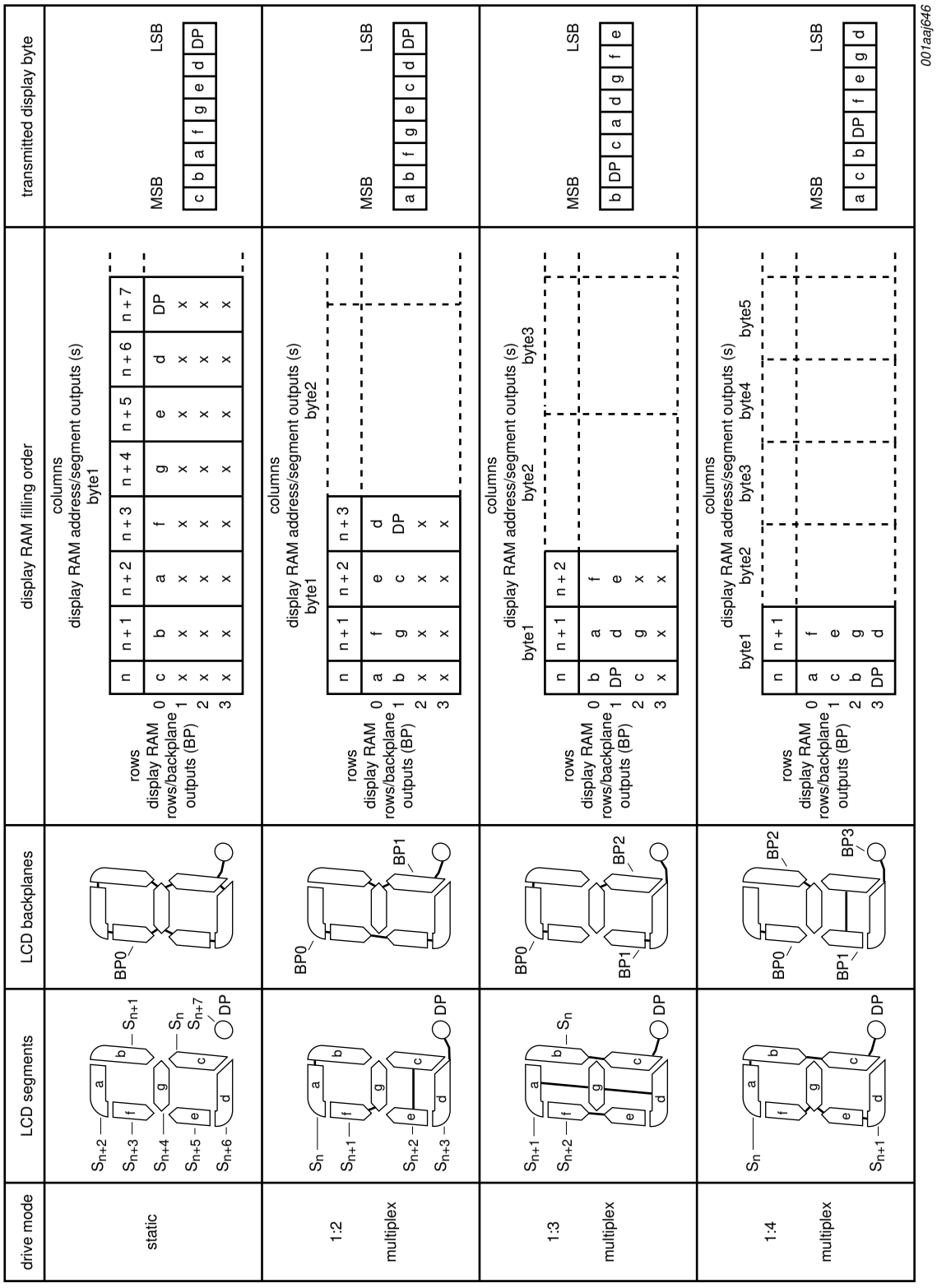
The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map Figure 10 shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2 and BP3 respectively.



Display RAM bit map showing direct relationship between RAM addresses and segment outputs; also between bits in a RAM word and the backplane outputs.

Fig 10. Display RAM bit map

When display data is transmitted to the PCA8576D, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 11; the RAM filling organization depicted applies equally to other LCD types.



x = data bit unchanged.

Fig 11. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

The following applies to Figure 11:

- In static drive mode the eight transmitted data bits are placed in row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer.

This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Section 7.17).

Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 11.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

After each byte is stored, the contents of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I²C-bus data access is terminated early then the state of the data pointer is unknown. The data pointer should be re-written prior to further RAM accesses.

7.12 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter match with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device-select command (see Section 7.17). If the contents of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCA8576D occurs when the last RAM address is exceeded.

Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1:3 multiplex mode).

The hardware subaddress must not be changed while the device is being accessed on the I^2C-bus interface.

7.13 Output bank selector

The output bank selector (see Table 14) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The $\overline{SYNC}$ signal resets these sequences to the following starting points: row 3 for 1:4 multiplex, row 2 for 1:3 multiplex, row 1 for 1:2 multiplex and row 0 for static mode.

The PCA8576D includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it, once it is assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

7.15 Blinking

The PCA8576D has a very versatile display blinking capability. The whole display can blink at a frequency selected by the blink-select command (see Table 15). Each blink frequency is a fraction of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected (see Table 7).

An additional feature allows an arbitrary selection of LCD segments to blink in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the blink-select command (see Table 15).

In the 1:3 and 1:4 drive modes, where no alternative RAM bank is available, groups of LCD segments can blink selectively by changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 11).

Table 7. Blinking frequencies[1]

Blink mode	Normal operating mode ratio	Nominal blink frequency
off	-	blinking off
1	$\frac{f_{clk}}{768}$	2 Hz
2	$\frac{f_{clk}}{1536}$	1 Hz
3	$\frac{f_{clk}}{3072}$	0.5 Hz

[1] Blink modes 1, 2 and 3 and the nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency (f_{clk}) of 1536 Hz (see Section 11).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 12).

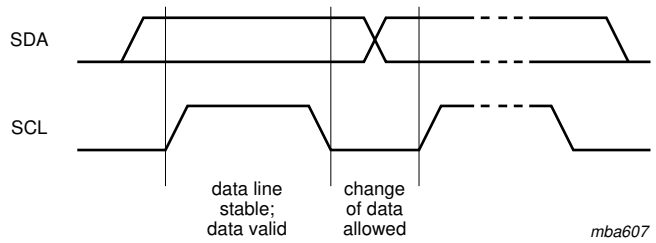


Fig 12. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 13).

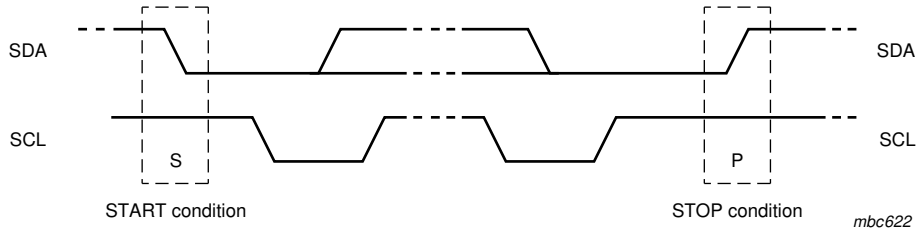


Fig 13. Definition of START and STOP conditions

7.16.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 14).

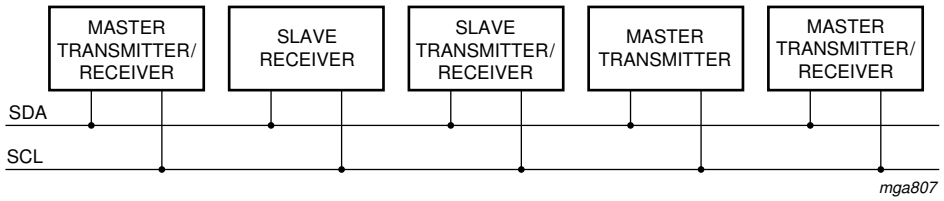


Fig 14. System configuration

7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is shown in Figure 15.

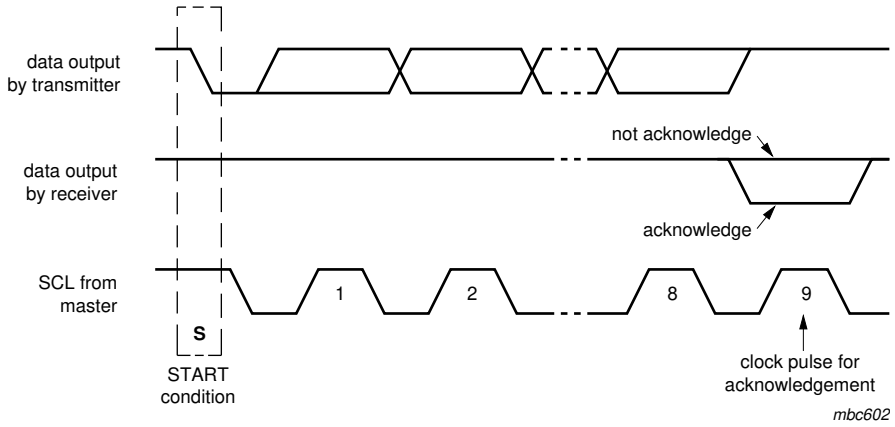


Fig 15. Acknowledgement of the I²C-bus

7.16.5 I²C-bus controller

The PCA8576D acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCA8576D are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCA8576D.

The PCA8576D slave address is illustrated in Table 8.

Table 8. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
	0	1	1	1	0	0	SA0	R/$\overline{W}$

The least significant bit of the slave address that a PCA8576D will respond to is defined by the level tied to its SA0 input. The PCA8576D is a write-only device and will not respond to a read access. Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 16 PCA8576D for very large LCD applications
- The use of two types of LCD multiplex drive modes.

The I²C-bus protocol is shown in Figure 16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCA8576D slave addresses available. All PCA8576D whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCA8576D whose SA0 inputs are set to the alternative level.

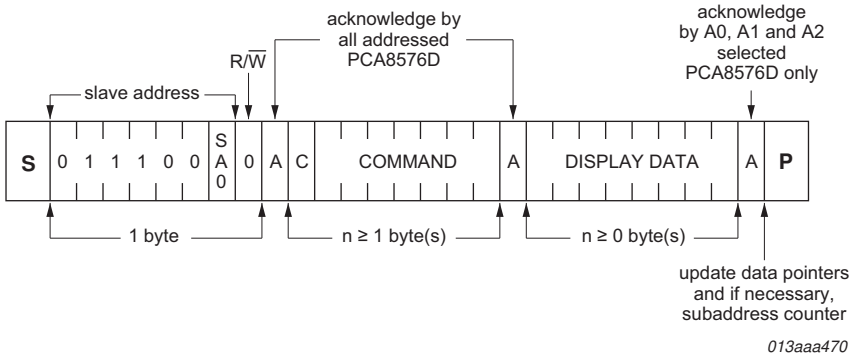


Fig 16. I²C-bus protocol

After an acknowledgement, one or more command bytes follow, that define the status of each addressed PCA8576D.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see Figure 17). The command bytes are also acknowledged by all addressed PCA8576D on the bus.

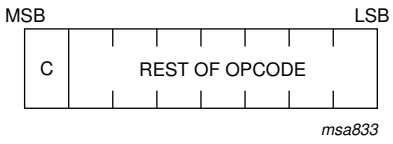


Fig 17. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCA8576D device.

An acknowledgement after each byte is asserted only by the PCA8576D that are addressed via address lines A0, A1 and A2. After the last display byte, the I²C-bus master asserts a STOP condition (P). Alternately a START may be asserted to restart an I²C-bus access.

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The commands available to the PCA8576D are defined in Table 9.

Table 9. Definition of PCA8576D commands

Command	Operation Code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	C	1	0	[1]	E	B	M[1:0]		Table 11
load-data-pointer	C	0	P[5:0]						Table 12
device-select	C	1	1	0	0	A[2:0]			Table 13
bank-select	C	1	1	1	1	0	I	O	Table 14
blink-select	C	1	1	1	0	AB	BF[1:0]		Table 15

[1] Not used.

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 17. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see Table 10).

Table 10. C bit description

Bit	Symbol	Value	Description
7	C		**continue bit**
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

Table 11. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 10
6 to 5	-	10	fixed value
4	-	-	unused
3	E		**display status**[1]
		0[2]	disabled (blank)[3]
		1	enabled
2	B		**LCD bias configuration**[4]
		0[2]	1/3 bias
		1	1/2 bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00[2]	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[4] Not applicable for static drive mode.

Table 12. Load-data-pointer command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 10
6	-	0	fixed value
5 to 0	P[5:0]	000000[1] to 100111	6 bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses

[1] Default value.

Table 13. Device-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 10
6 to 3	-	1100	fixed value
2 to 0	A[2:0]	000[1] to 111	3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

[1] Default value.

Table 14. Bank-select command bit description

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7	C	0, 1	see Table 10	
6 to 2	-	11110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0[2]	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0[2]	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

[2] Default value.

Table 15. Blink-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 10
6 to 3	-	1110	fixed value
2	AB		**blink mode selection**
		0[1]	normal blinking[2]
		1	alternate RAM bank blinking[3]
1 to 0	BF[1:0]		**blink frequency selection**
		00[1]	off
		01	1
		10	2
		11	3

[1] Default value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.