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PCA9539; PCA9539R

16-bit I²C-bus and SMBus low power I/O port with interrupt and reset

Rev. 9 — 8 November 2017 Product data sheet

1. General description

The PCA9539; PCA9539R is a 24-pin CMOS device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion with interrupt and reset for I²C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9539; PCA9539R consists of two 8-bit configuration (input or output selection), input, output and polarity inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity inversion register. All registers can be read by the system master.

The PCA9539; PCA9539R is identical to the PCA9555 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW, replacement of A2 with $\overline{\text{RESET}}$ and a different address range.

The PCA9539; PCA9539R open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed.

The power-on reset sets the registers to their default values and initializes the device state machine. In the PCA9539, the $\overline{\text{RESET}}$ pin causes the same reset/default I/O input configuration to occur without de-powering the device, holding the registers and I²C-bus state machine in their default state until the $\overline{\text{RESET}}$ input is once again HIGH. This input requires a pull-up to V_{DD}. In the PCA9539R however, only the device state machine is initialized by the $\overline{\text{RESET}}$ pin and the internal general-purpose registers remain unchanged. Using the PCA9539R $\overline{\text{RESET}}$ pin will only reset the I²C-bus interface should it be stuck LOW to regain access to the I²C-bus. This allows the I/O pins to retain their last configured state so that they can keep any lines in their previously defined state and not cause system errors while the I²C-bus is being restored.

Two hardware pins (A0, A1) vary the fixed I²C-bus address and allow up to four devices to share the same I²C-bus/SMBus.

2. Features and benefits

- 16-bit I²C-bus GPIO with interrupt and reset
- Operating power supply voltage range of 2.3 V to 5.5 V (3.0 V to 5.5 V for PCA9539PW/Q900 and PCA9539RPW/Q900)
- 5 V tolerant I/Os

- Polarity inversion register
- Active LOW interrupt output
- Active LOW reset input
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in three different packages: SO24, TSSOP24, and HVQFN24

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9539BS	9539	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1
PCA9539RBS	539R	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1
PCA9539D	PCA9539D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA9539PW	PCA9539PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9539PW/Q900[1]	PCA9539PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9539RPW	PA9539RPW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9539RPW/Q900[1]	PA9539RPW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

[1] PCA9539PW/Q900 and PCA9539RPW/Q900 are AEC-Q100 compliant. Contact **I2C.support@nxp.com** for PPAP.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9539BS	PCA9539BS,115	HVQFN24	Reel 7” Q1/T1 *standard mark SMD[1]	1500	T_{amb} = −40 °C to +85 °C
	PCA9539BS,118	HVQFN24	Reel 13” Q1/T1 *standard mark SMD[1]	6000	T_{amb} = −40 °C to +85 °C
	PCA9539BSHP	HVQFN24	Reel 13” Q2/T3 *standard mark SMD[2]	6000	T_{amb} = −40 °C to +85 °C

Table 2. Ordering options *…continued*

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9539RBS	PCA9539RBS,118	HVQFN24	Reel 13” Q1/T1 *standard mark SMD[1]	6000	T_{amb} = −40 °C to +85 °C
PCA9539D	PCA9539D,112	SO24	Standard marking * IC’s tube - DSC bulk pack	1200	T_{amb} = −40 °C to +85 °C
	PCA9539D,118	SO24	Reel 13” Q1/T1 *standard mark SMD[1]	1000	T_{amb} = −40 °C to +85 °C
PCA9539PW	PCA9539PW,112	TSSOP24	Standard marking * IC’s tube - DSC bulk pack	1575	T_{amb} = −40 °C to +85 °C
	PCA9539PW,118	TSSOP24	Reel 13” Q1/T1 *standard mark SMD[1]	2500	T_{amb} = −40 °C to +85 °C
PCA9539PW/Q900	PCA9539PW/Q900,118	TSSOP24	Reel 13” Q1/T1 *standard mark SMD[1]	2500	T_{amb} = −40 °C to +125 °C
PCA9539RPW	PCA9539RPW,118	TSSOP24	Reel 13” Q1/T1 *standard mark SMD[1]	2500	T_{amb} = −40 °C to +85 °C
PCA9539RPW/Q900	PCA9539RPWJ	TSSOP24	Reel 13” Q1/T1 *standard mark SMD[1]	2500	T_{amb} = −40 °C to +125 °C

[1] Pin 1 in Quadrant 1; see Figure 2.

[2] Pin 1 in Quadrant 2; see Figure 3.

3.1.1 Pin 1 quadrant indication

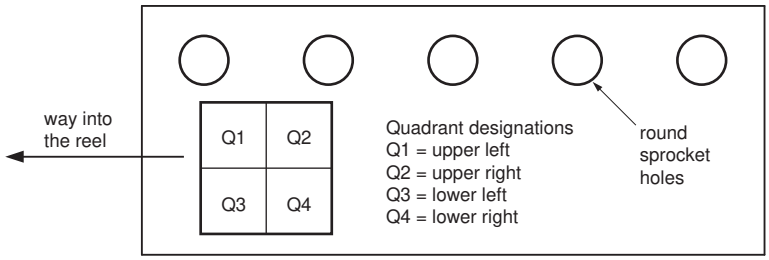


Fig 1. Carrier tape pin 1 quadrant designations

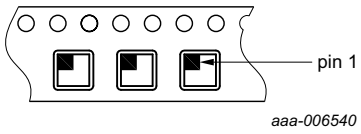


Fig 2. Pin 1 in Q1

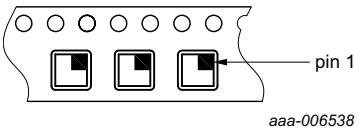
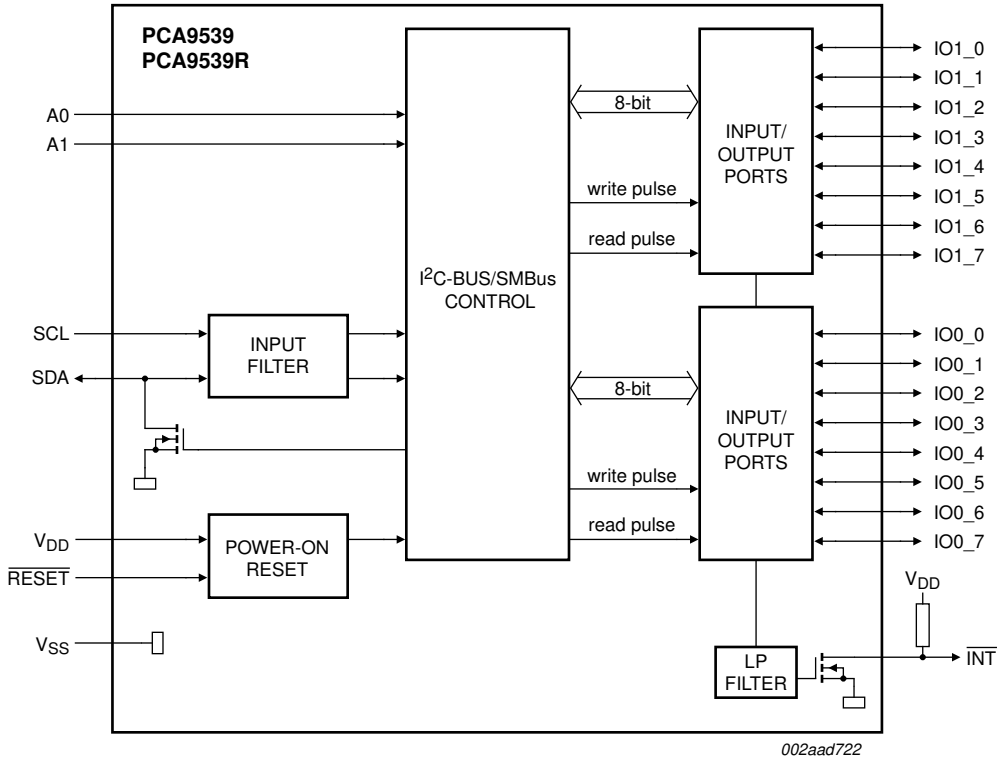


Fig 3. Pin 1 in Q2

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig 4. Block diagram of PCA9539; PCA9539R

5. Pinning information

5.1 Pinning

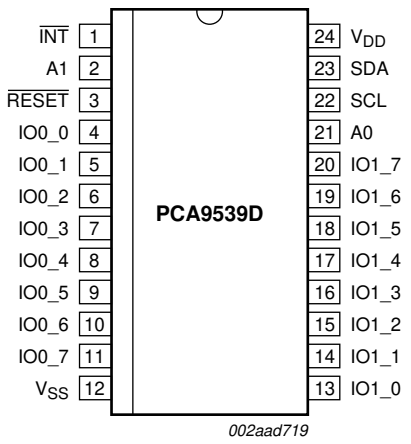


Fig 5. Pin configuration for SO24

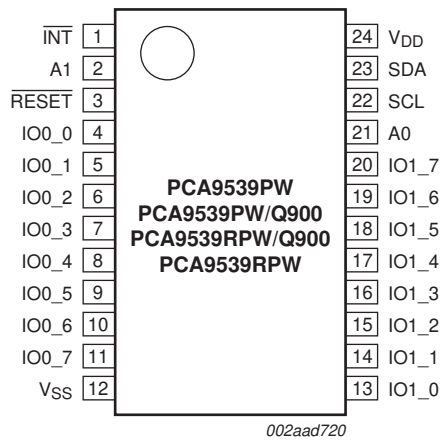


Fig 6. Pin configuration for TSSOP24

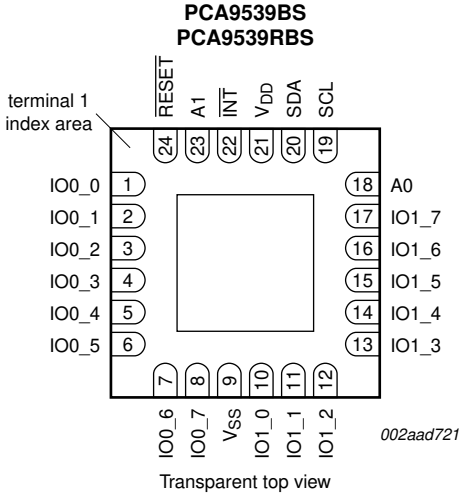


Fig 7. Pin configuration for HVQFN24

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO24, TSSOP24	HVQFN24	
$\overline{INT}$	1	22	interrupt output (open-drain)
A1	2	23	address input 1
$\overline{RESET}$	3	24	active LOW reset input. Driving this pin LOW causes: • PCA9539 to reset its state machine and registers • PCA9539R to reset its state machine, but has no effect on its registers
IO0_0	4	1	port 0 input/output 0
IO0_1	5	2	port 0 input/output 1
IO0_2	6	3	port 0 input/output 2
IO0_3	7	4	port 0 input/output 3
IO0_4	8	5	port 0 input/output 4
IO0_5	9	6	port 0 input/output 5
IO0_6	10	7	port 0 input/output 6
IO0_7	11	8	port 0 input/output 7
V_{SS}	12	9[1]	supply ground
IO1_0	13	10	port 1 input/output 0
IO1_1	14	11	port 1 input/output 1
IO1_2	15	12	port 1 input/output 2
IO1_3	16	13	port 1 input/output 3
IO1_4	17	14	port 1 input/output 4
IO1_5	18	15	port 1 input/output 5
IO1_6	19	16	port 1 input/output 6
IO1_7	20	17	port 1 input/output 7
A0	21	18	address input 0
SCL	22	19	serial clock line input
SDA	23	20	serial data line open-drain input/output
V_{DD}	24	21	supply voltage

[1] HVQFN24 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

Refer to Figure 4 “Block diagram of PCA9539; PCA9539R”.

6.1 Device address

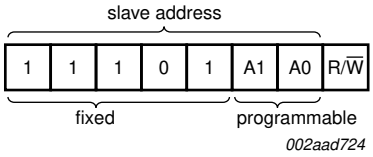


Fig 8. PCA9539; PCA9539R device address

6.2 Registers

6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 4. Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity inversion port 0
5	Polarity inversion port 1
6	Configuration port 0
7	Configuration port 1

6.2.2 Registers 0 and 1: Input port registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5. Input port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6. Input port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

6.2.3 Registers 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 7. Output port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8. Output port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

6.2.4 Registers 4 and 5: Polarity inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 9. Polarity inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10. Polarity inversion port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

6.2.5 Registers 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. At reset, the device's ports are inputs.

Table 11. Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12. Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

6.3 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9539; PCA9539R in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9539; PCA9539R registers and SMBus state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

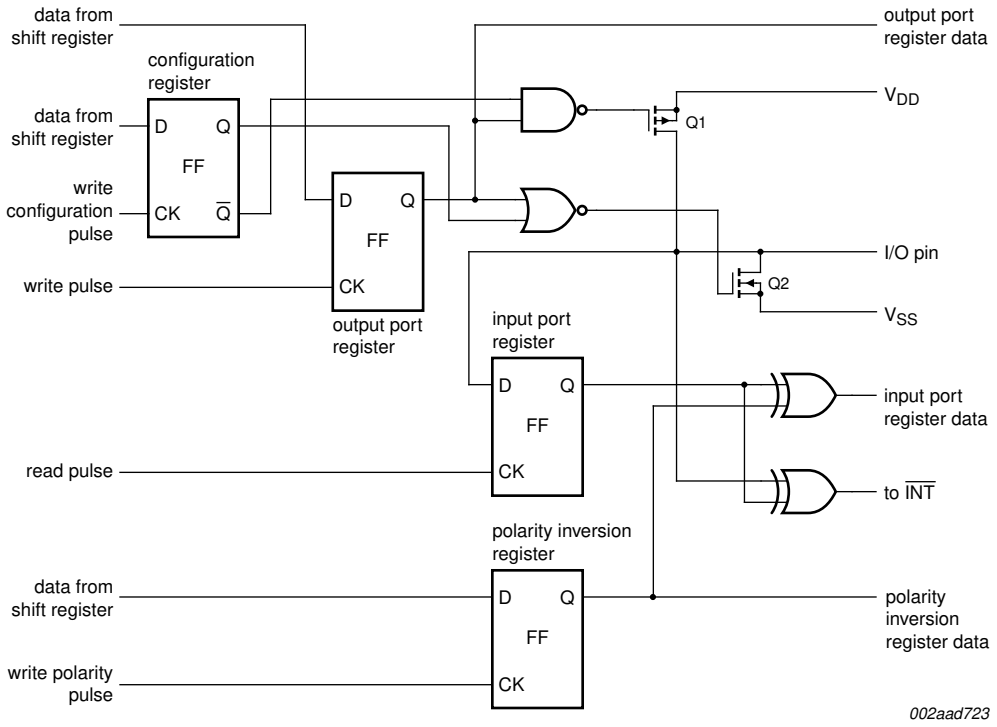
6.4 $\overline{\text{RESET}}$ input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. In the PCA9539 the registers and SMBus/I²C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH. This input typically requires a pull-up to V_{DD}. In the PCA9539R, only the device state machine is initialized. The internal general-purpose registers remain unchanged. Using the PCA9539R hardware reset pin will only reset the I²C-bus interface should it be stuck LOW to regain access to the I²C-bus. This allows the I/O pins to retain their last configured state so that they can keep any lines in their previously defined state and not cause system errors while the I²C-bus is being restored.

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either V_{DD} or V_{SS}.



At power-on reset, all registers return to default values.

Fig 9. Simplified schematic of I/Os

6.6 Bus transactions

6.6.1 Writing to the port registers

Data is transmitted to the PCA9539; PCA9539R by sending the device address and setting the least significant bit to a logic 0 (see Figure 8 “PCA9539; PCA9539R device address”). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the PCA9539; PCA9539R are configured to operate as four register pairs. The four pairs are Input ports, Output ports, Polarity inversion ports, and Configuration ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 10 and Figure 11). For example, if the first byte is sent to Output port 1 (register 3), then the next byte will be stored in Output port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

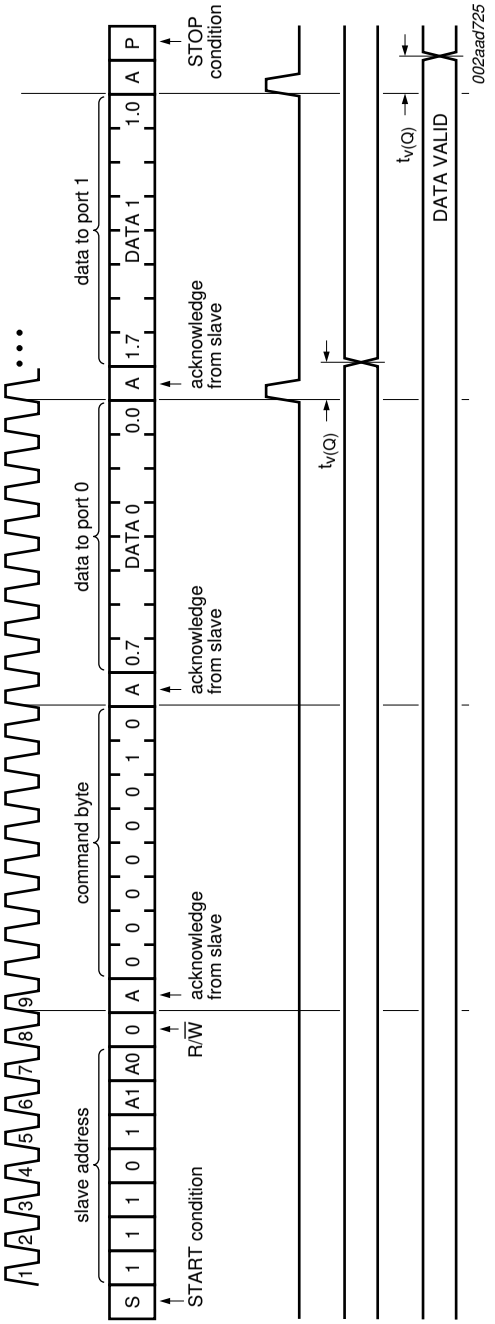


Fig 10. Write to output port registers

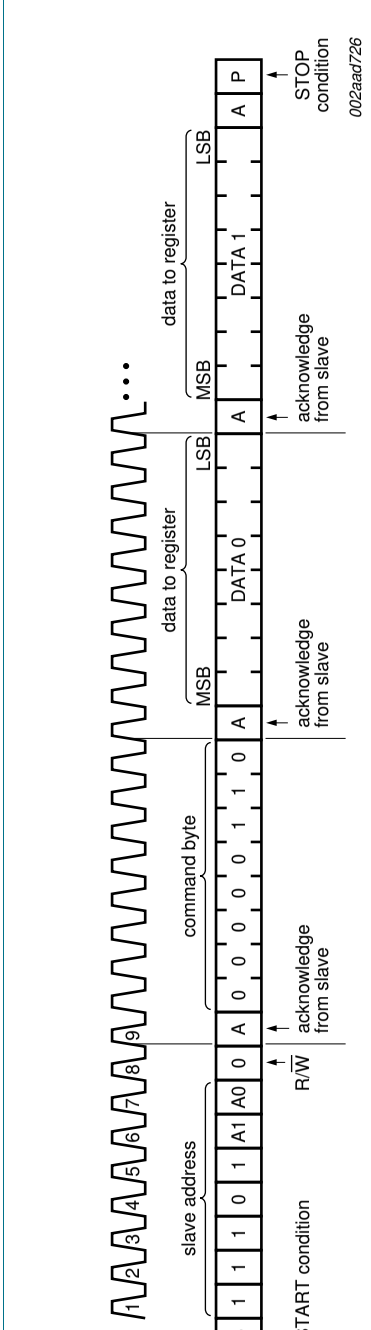
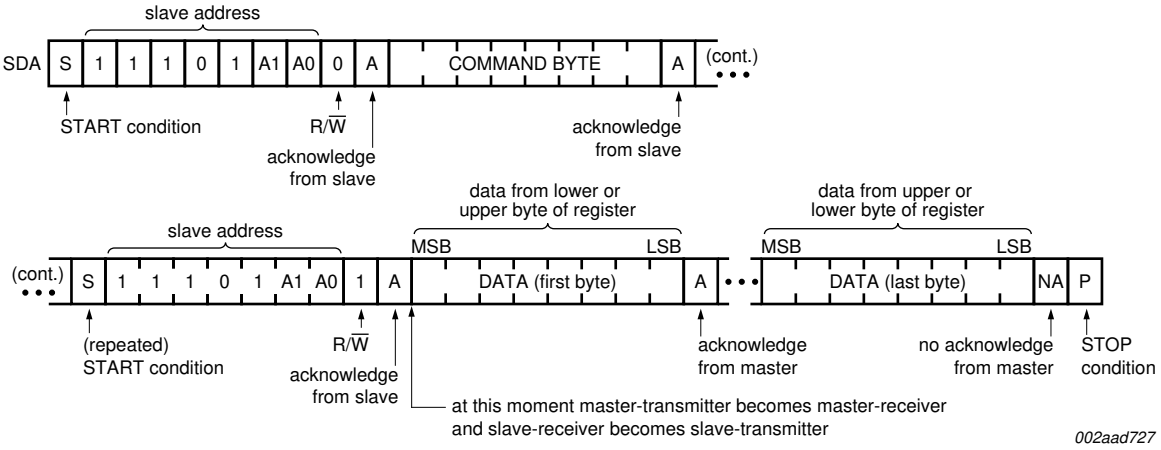


Fig 11. Write to configuration registers

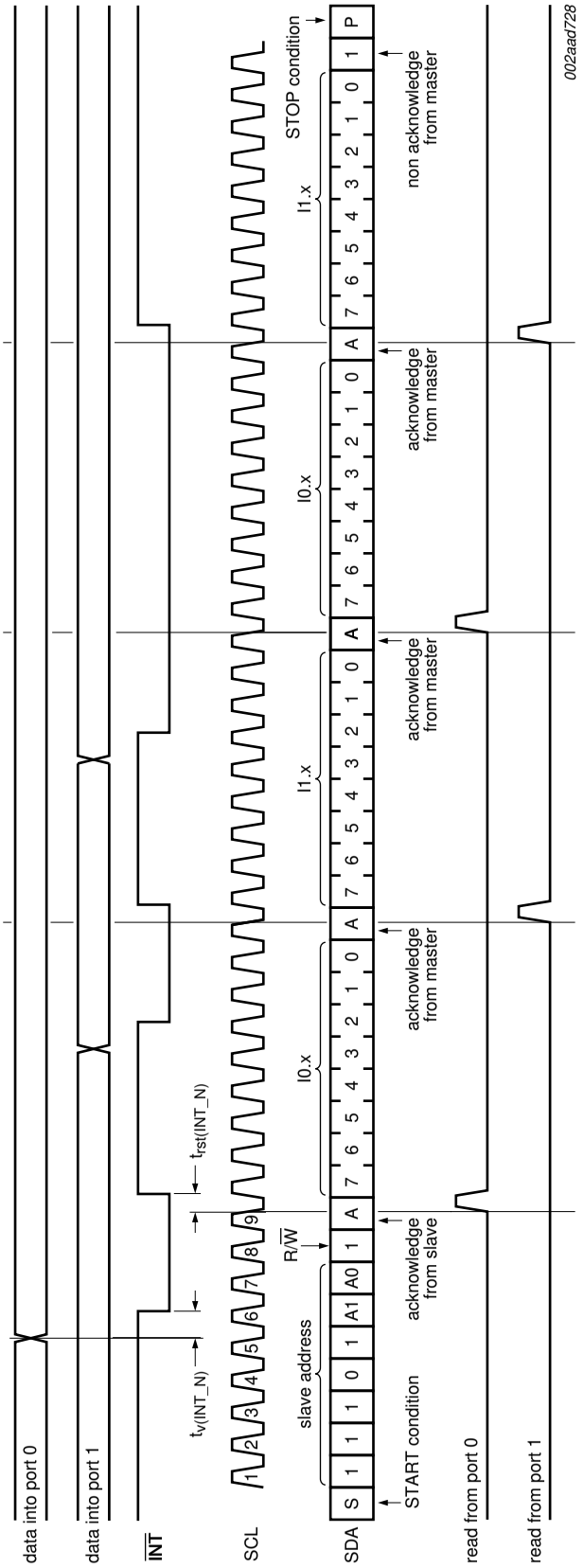
6.6.2 Reading the port registers

In order to read data from the PCA9539; PCA9539R, the bus master must first send the PCA9539; PCA9539R address with the least significant bit set to a logic 0 (see Figure 8 "PCA9539; PCA9539R device address"). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PCA9539; PCA9539R (see Figure 12, Figure 13 and Figure 14). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input port 1, then the next byte read would be Input port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.



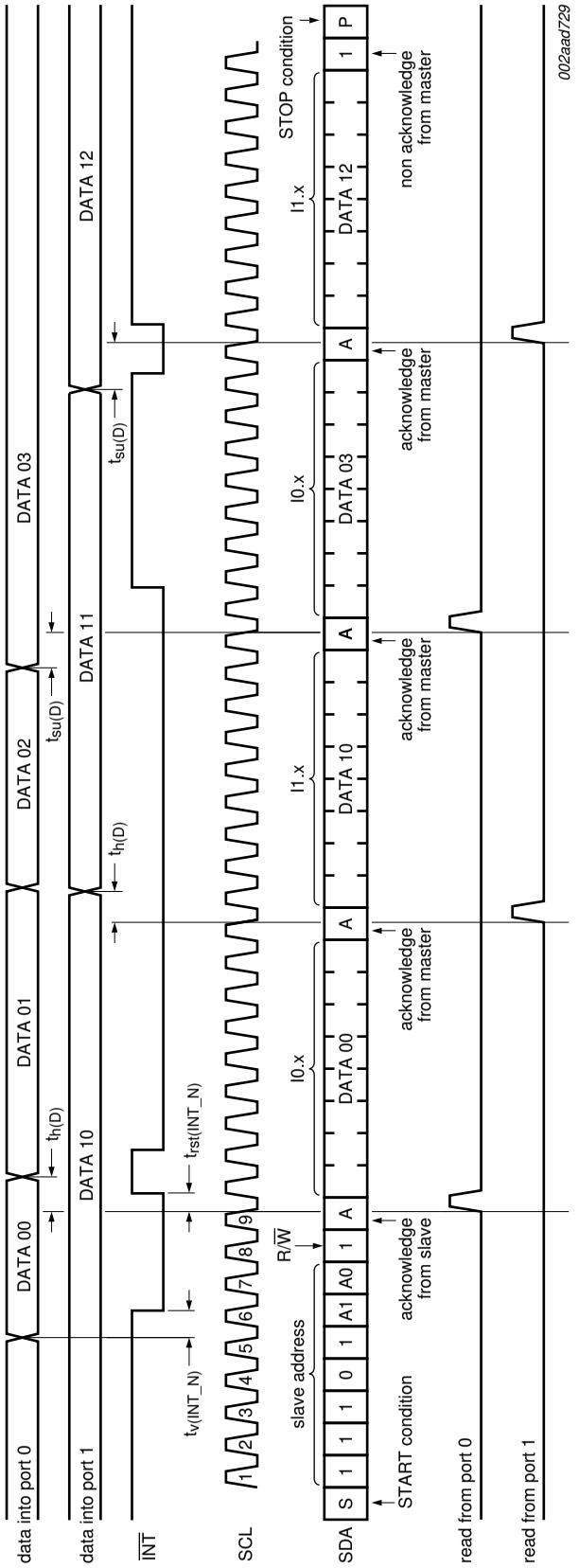
Remark: Transfer can be stopped at any time by a STOP condition.

Fig 12. Read from register



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

Fig 13. Read input port register, scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

Fig 14. Read input port register, scenario 2

6.6.3 Interrupt output

The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input port register is read (see Figure 13). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input port register.

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 15).

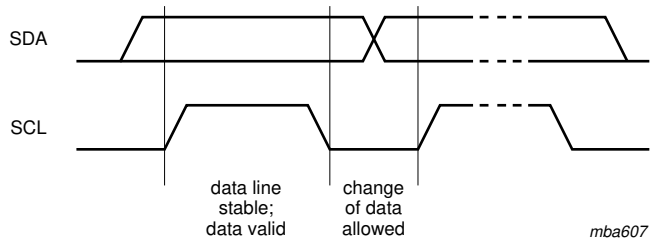


Fig 15. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 16).

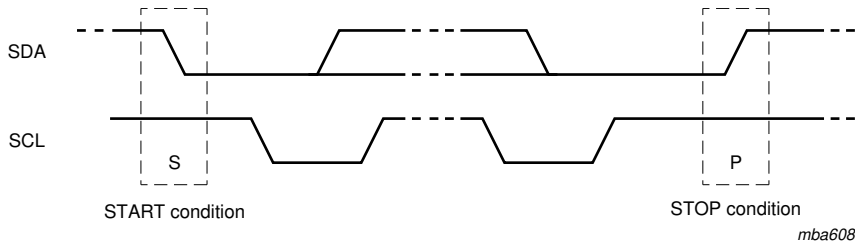


Fig 16. Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 17).

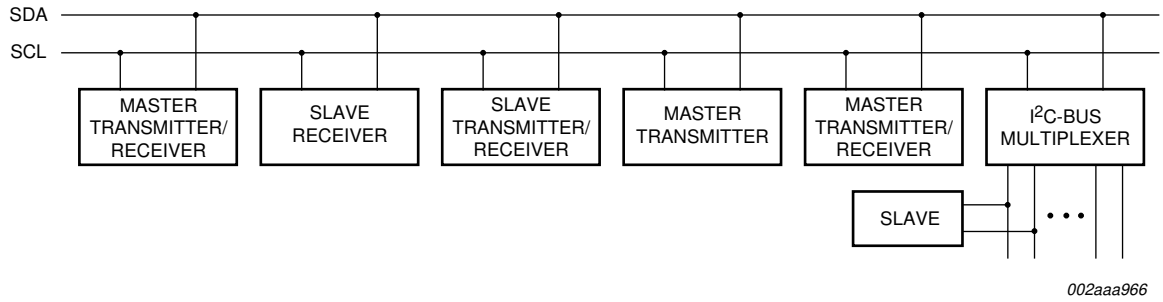


Fig 17. System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

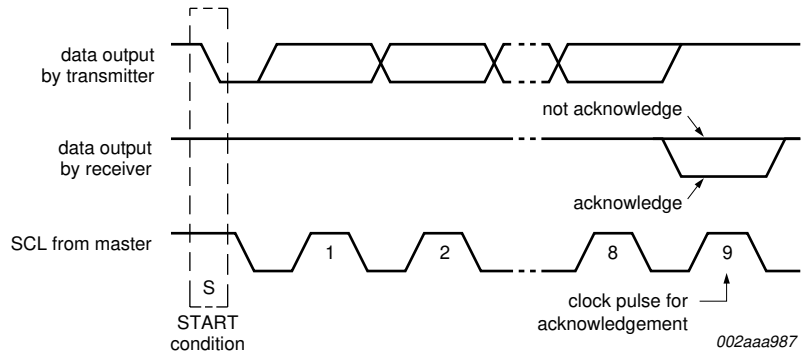
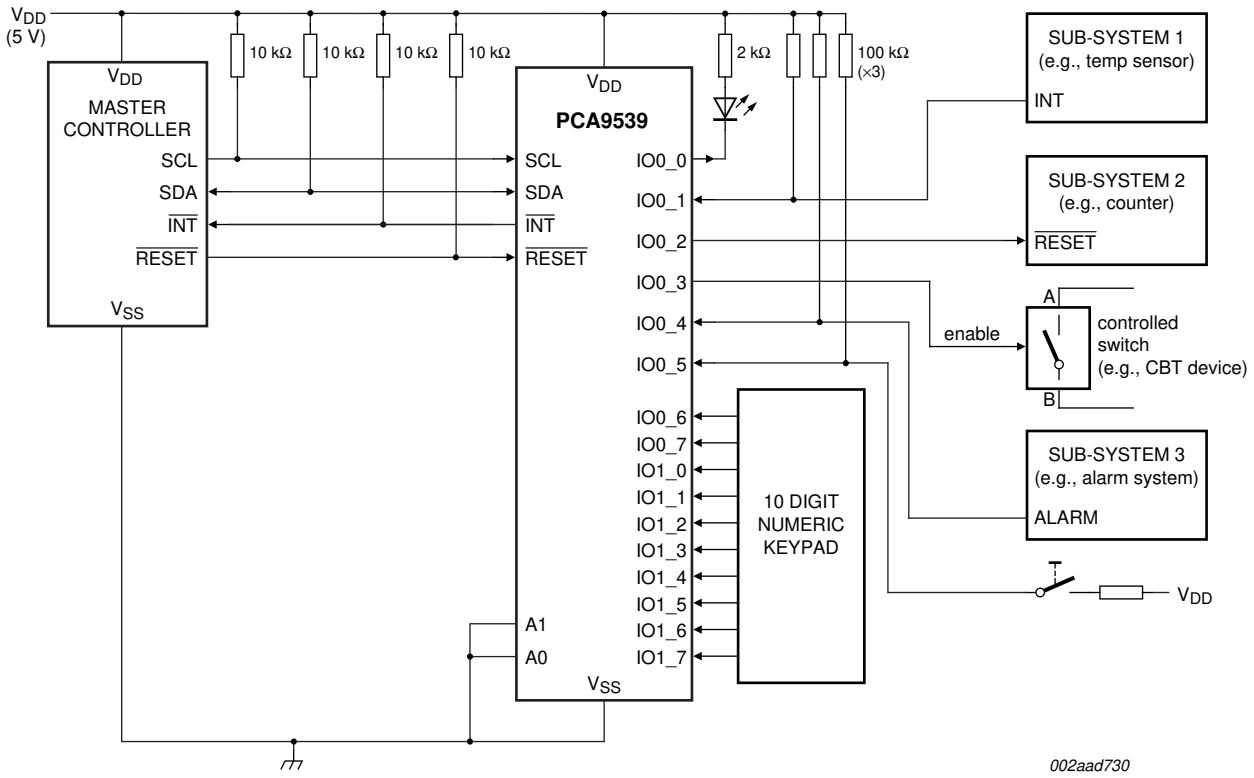


Fig 18. Acknowledgement on the I²C-bus

8. Application design-in information



Device address configured as 1110 100X for this example.

IO0_0, IO0_2, IO0_3 configured as outputs.

IO0_1, IO0_4, IO0_5 configured as inputs.

IO0_6, IO0_7 and (IO1_0 to IO1_7) configured as inputs.

Fig 19. Typical application

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 19. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 20 shows a high value resistor in parallel with the LED. Figure 21 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

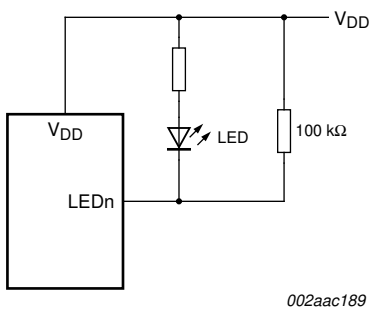


Fig 20. High value resistor in parallel with the LED

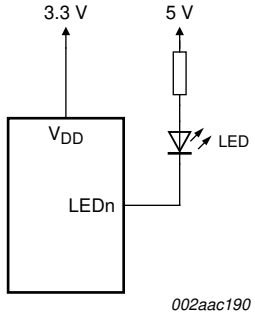


Fig 21. Device supplied by a lower voltage

9. Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		V_{SS} − 0.5	6	V
I_O	output current	on an I/O pin	-	±50	mA
I_I	input current		-	±20	mA
I_{DD}	supply current		-	160	mA
I_{SS}	ground supply current		-	200	mA
P_{tot}	total power dissipation		-	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating			
		all devices except PCA9539PW/Q900 and PCA9539RPW/Q900	−40	+85	°C
		PCA9539PW/Q900 and PCA9539RPW/Q900	−40	+125	°C
$T_{j(max)}$	maximum junction temperature		-	125	°C

10. Static characteristics

Table 14. Static characteristics for all devices except PCA9539PW/Q900 and PCA9539RPW/Q900

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz; I/O = inputs	-	135	200	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs	-	0.25	1	µA
		Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs	-	0.25	1	µA
V_{POR}	power-on reset voltage[1]	no load; V_I = V_{DD} or V_{SS}	-	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
I_L	leakage current	V_I = V_{DD} = V_{SS}	−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}	-	6	10	pF
I/Os						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.5 V [2]	8	9	-	mA
		V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.7 V [2]	10	11	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; V_{DD} = 2.3 V [3]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V [3]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V [3]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V [3]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V [3]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V [3]	4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 5.5 V; V_I = V_{DD}	-	-	1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; V_I = V_{SS}	-	-	−1	µA
C_i	input capacitance		-	3.7	5	pF
C_o	output capacitance		-	3.7	5	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
Select inputs A0, A1 and $\overline{RESET}$						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA

[1] V_{DD} must be lowered to 0.2 V for at least 5 µs in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.

[3] The total current sourced by all I/Os must be limited to 160 mA (80 mA for IO0_0 through IO0_7 and 80 mA for IO1_0 through IO1_7).

Table 15. Static characteristics for PCA9539PW/Q900 and PCA9539RPW/Q900

V_{DD} = 3.0 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		3.0	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz; I/O = inputs	-	135	200	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	-	0.25	1	µA
		Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	-	0.25	1	µA
V_{POR}	power-on reset voltage[1]	no load; $V_I = V_{DD}$ or V_{SS}	-	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current, SDA	V_{OL} = 0.4 V				
		V_{DD} = 5.5 V	3	-	-	mA
		V_{DD} = 3.0 V	2.5	-	-	mA
I_L	leakage current	$V_I = V_{DD} = V_{SS}$	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	6	10	pF
I/Os						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V				
		V_{DD} = 4.5 V [2]	8	9	-	mA
		V_{DD} = 3.0 V [2]	7.5	-	-	mA
		V_{OL} = 0.7 V				
		V_{DD} = 4.5 V [2]	10	11	-	mA
		V_{DD} = 3.0 V [2]	9.5	-	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA				
		V_{DD} = 4.5 V [3]	4.1	-	-	V
		V_{DD} = 3.0 V [3]	2.5	-	-	V
		I_{OH} = −10 mA				
		V_{DD} = 4.5 V [3]	4.0	-	-	V
		V_{DD} = 3.0 V [3]	2.4	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 5.5 V; $V_I = V_{DD}$	-	-	1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$	-	-	−1	µA
C_i	input capacitance		-	3.7	5	pF
C_o	output capacitance		-	3.7	5	pF
Interrupt INT						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA

Table 15. Static characteristics for PCA9539PW/Q900 and PCA9539RPW/Q900 *...continued*

V_{DD} = 3.0 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Select inputs A0, A1 and $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA

[1] V_{DD} must be lowered to 0.2 V for at least 5 µs in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.

[3] The total current sourced by all I/Os must be limited to 160 mA (80 mA for IO0_0 through IO0_7 and 80 mA for IO1_0 through IO1_7).

11. Dynamic characteristics

Table 16. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals	[3]	-	300	$20 + 0.1C_b$	300	ns
t_r	rise time of both SDA and SCL signals	[3]	-	1000	$20 + 0.1C_b$	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{v(Q)}$	data output valid time	[4]	-	200	-	200	ns
$t_{su(D)}$	data input set-up time		150	-	150	-	ns
$t_{h(D)}$	data input hold time		1	-	1	-	µs

Table 16. Dynamic characteristics *…continued*

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
Interrupt timing							
$t_{v(INT\_N)}$	valid time on pin $\overline{INT}$		-	4	-	4	µs
$t_{rst(INT\_N)}$	reset time on pin $\overline{INT}$		-	4	-	4	µs
$\overline{RESET}$ timing							
$t_{w(rst)}$	reset pulse width	all devices except PCA9539RPW/Q900	4	-	4	-	ns
		PCA9539RPW/Q900	6	-	6	-	ns
$t_{rec(rst)}$	reset recovery time		0	-	0	-	ns
t_{rst}	reset time	[5][6]	400	-	400	-	ns

[1] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

[4] $t_{v(Q)}$ measured from $0.7V_{DD}$ on SCL to 50 % I/O output.

[5] Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.

[6] Upon reset, the full delay will be the sum of t_{rst} and the RC time constant of the SDA bus.

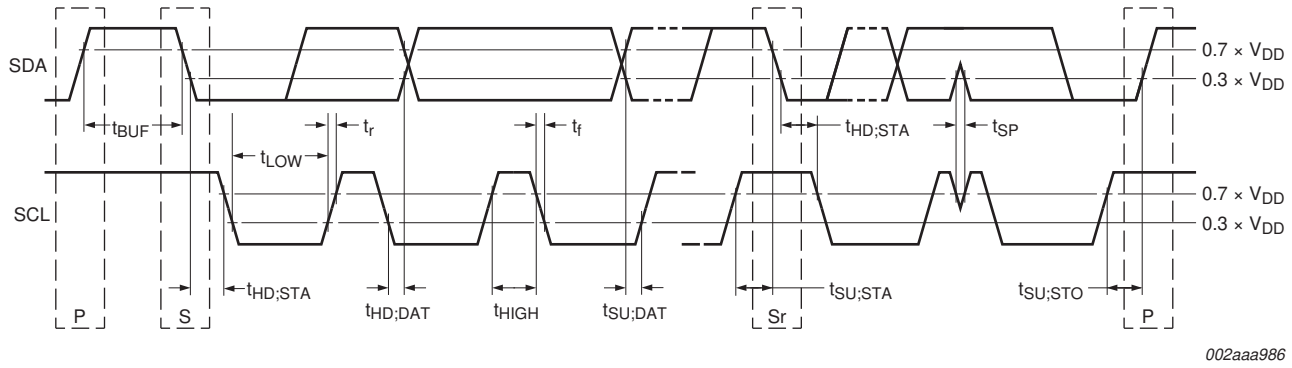


Fig 22. Definition of timing on the I²C-bus

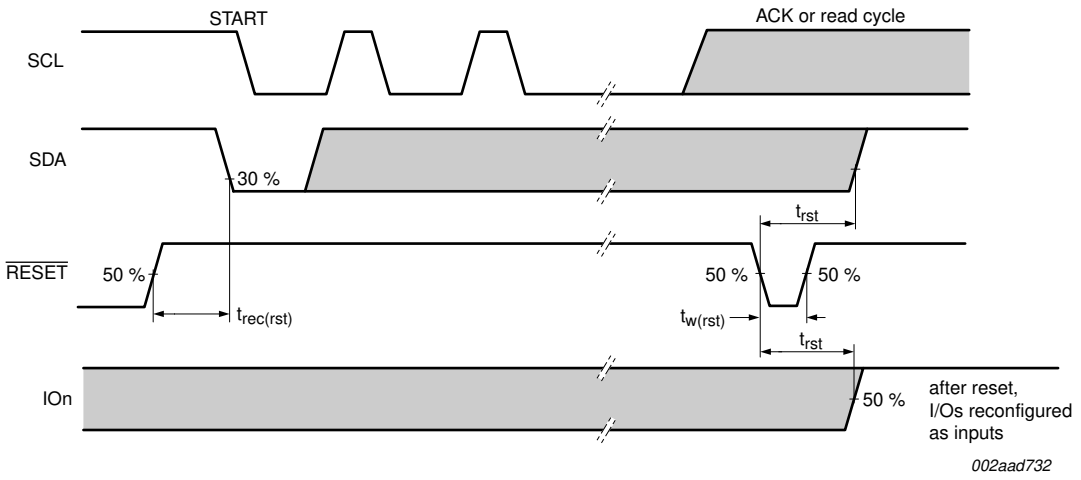


Fig 23. Definition of $\overline{\text{RESET}}$ timing in PCA9539

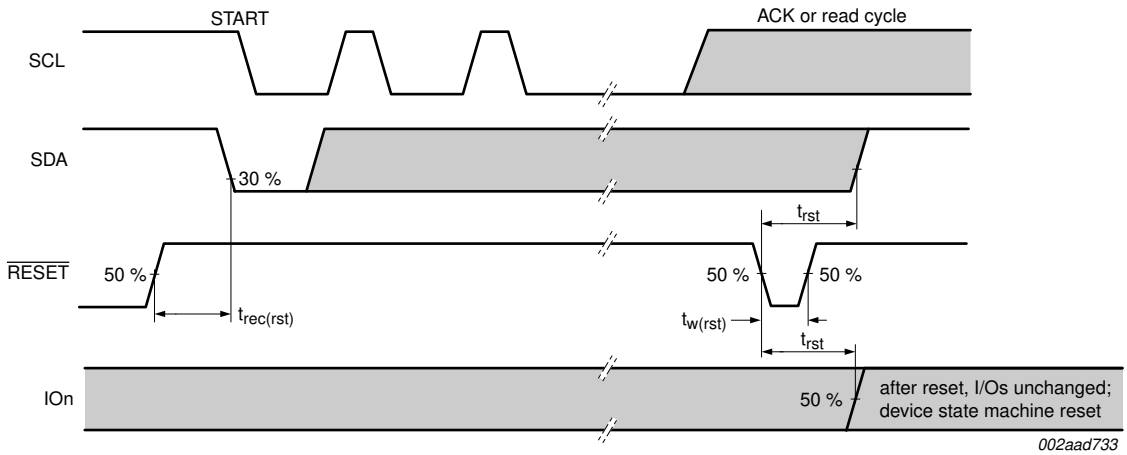


Fig 24. Definition of $\overline{\text{RESET}}$ timing in PCA9539R

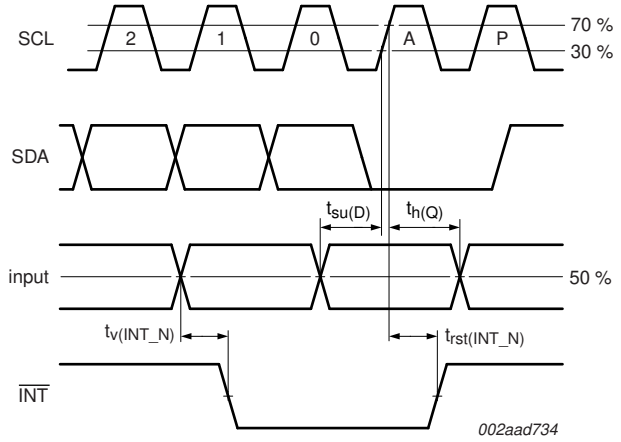


Fig 25. Expanded view of read input port register

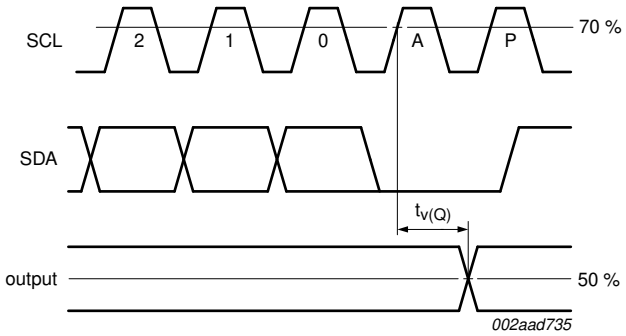
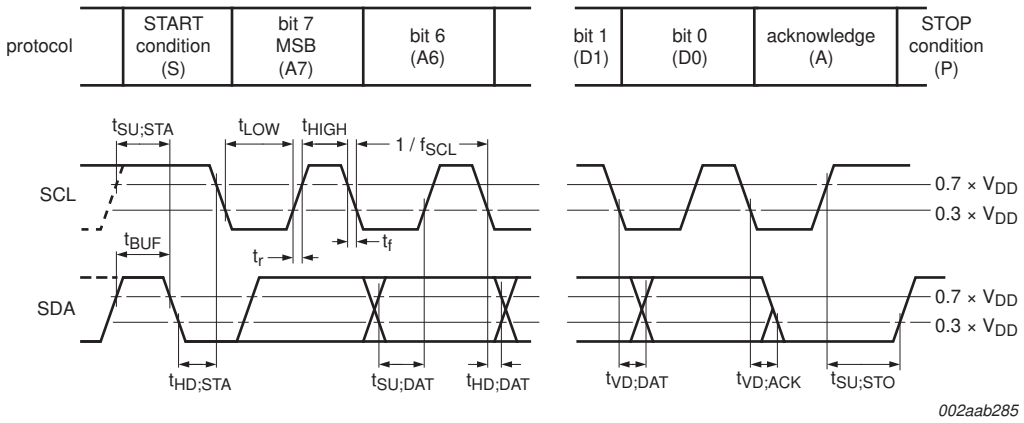


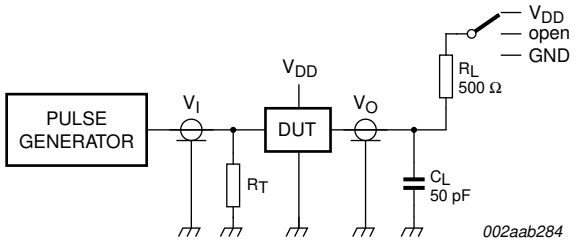
Fig 26. Expanded view of write to output port register



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 27. I²C-bus timing diagram

12. Test information



R_L = load resistor.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance of Z_o of the pulse generators.

Fig 28. Test circuitry for switching times

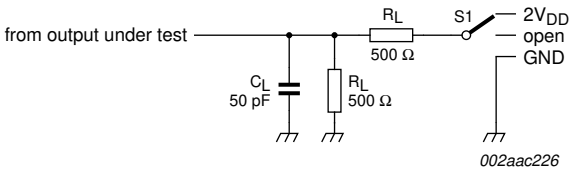


Fig 29. Load circuit

Table 17. Test data

Test	Load		Switch
	C_L	R_L	
$t_{v(Q)}$	50 pF	500 Ω	2 × V_{DD}