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PCA9554B; PCA9554C

Low-voltage 8-bit I²C-bus and SMBus low power I/O port with interrupt, weak pull-up

Rev. 2 — 4 August 2015 Product data sheet

1. General description

The PCA9554B and PCA9554C are low-voltage 8-bit General Purpose Input/Output (GPIO) expanders with interrupt and weak pull-up resistors for I²C-bus/SMBus applications. The only difference between the PCA9554B and PCA9554C is their I²C fixed address allowing a larger number of the same device on the I²C-bus with no chance of address conflict. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs, fan control, etc.

In addition to providing a flexible set of GPIOs, the wide V_{DD} range of 1.65 V to 5.5 V allow the PCA9554B/PCA9554C to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCA9554B/PCA9554C contain a register set of 8-bit Configuration, Input, Output, and Polarity Inversion registers.

The PCA9554B is a pin-to-pin replacement for the PCA9554, while the PCA9554C replaces the PCA9554A. Both of these devices replace other industry-standard part numbers. More fully-featured parts PCAL9554B and PCAL9554C are also available with Agile I/O features. See the respective data sheet for more details.

The PCA9554B/PCA9554C open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCA9554B/PCA9554C can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins have weak pull-up resistors connected to them to eliminate external components.

Three hardware pins (A0, A1, A2) select the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus. The PCA9554B and PCA9554C differ only in their base I²C-bus addresses permitting a total of 16 devices on the I²C-bus, minimizing the chance for address conflict, even in the most complex system.

2. Features and benefits

- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 1.5 μA (typical at 5 V V_{DD})
  - 1.0 μA (typical at 3.3 V V_{DD})
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - $V_{hys} = 0.10 \times V_{DD}$ (typical)
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output ($\overline{INT}$)
- 400 kHz Fast-mode I²C-bus
- Input/output configuration register
- Polarity inversion register
- Internal power-on reset
- Power-up with all channels configured as inputs with weak pull-up resistors
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection exceeds JESD22
  - 2000 V Human Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP16 and HVQFN16

3. Ordering information

Table 1. Ordering information

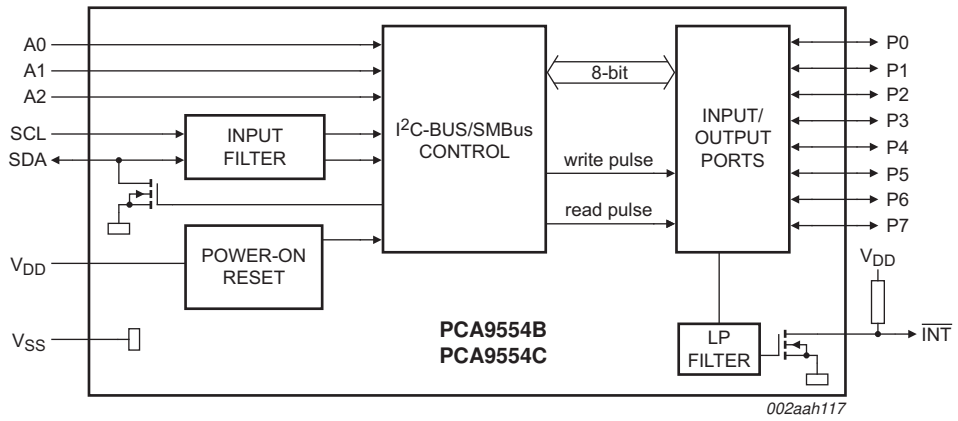
Type number	Topside mark	Package		
		Name	Description	Version
PCA9554BBS	P4B	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9554BPW	PA9554B	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9554CBS	P4C	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9554CPW	PA9554C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9554BBS	PCA9554BBSHP	HVQFN16	Reel pack, SMD, 13-inch, Turned	6000	T_{amb} = −40 °C to +85 °C
PCA9554BPW	PCA9554BPWJ	TSSOP16	Reel pack, SMD, 13-inch	2500	T_{amb} = −40 °C to +85 °C
PCA9554CBS	PCA9554CBSHP	HVQFN16	Reel pack, SMD, 13-inch, Turned	6000	T_{amb} = −40 °C to +85 °C
PCA9554CPW	PCA9554CPWJ	TSSOP16	Reel pack, SMD, 13-inch	2500	T_{amb} = −40 °C to +85 °C

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCA9554B; PCA9554C

5. Pinning information

5.1 Pinning

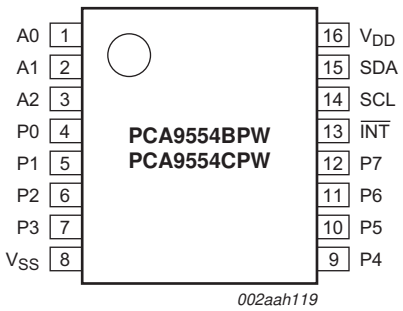


Fig 2. Pin configuration for TSSOP16

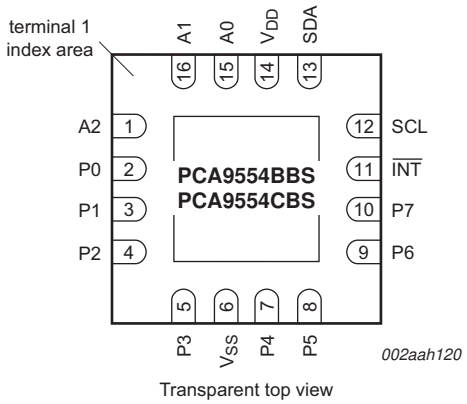


Fig 3. Pin configuration for HVQFN16

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP16	HVQFN16	
A0	1	15	address input 0
A1	2	16	address input 1
A2	3	1	address input 2
P0[1]	4	2	Port P input/output 0
P1[1]	5	3	Port P input/output 1
P2[1]	6	4	Port P input/output 2
P3[1]	7	5	Port P input/output 3
V_{SS}	8	6[2]	supply ground
P4[1]	9	7	Port P input/output 4
P5[1]	10	8	Port P input/output 5
P6[1]	11	9	Port P input/output 6
P7[1]	12	10	Port P input/output 7
$\overline{INT}$	13	11	interrupt output (open-drain)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V_{DD}	16	14	supply voltage

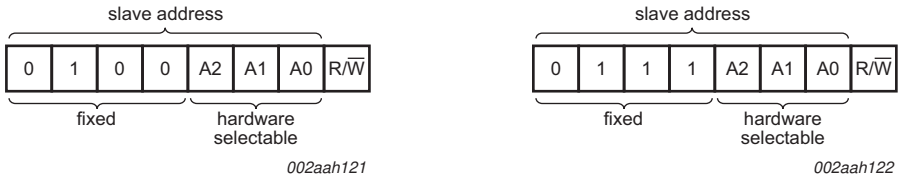
[1] All I/O are configured as input at power-on.

[2] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6. Functional description

Refer to Figure 1 “Block diagram of PCA9554B; PCA9554C”.

6.1 Device address



a. PCA9554B address

b. PCA9554C address

Fig 4. Device address

A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

6.2 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCA9554B/PCA9554C. The lower two bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

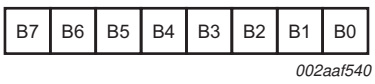


Fig 5. Pointer register bits

Table 4. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Output port	read/write byte	1111 1111
0	0	0	0	0	0	1	0	02h	Polarity Inversion	read/write byte	0000 0000
0	0	0	0	0	0	1	1	03h	Configuration	read/write byte	1111 1111

[1] Undefined.

6.3 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
PCA9554B I²C-bus slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
PCA9554C I²C-bus slave address	L	H	H	H	A2	A1	A0	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

6.4 Register descriptions

6.4.1 Input port register (00h)

The Input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port register is read only; writes to this register have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 7.2 "Read commands".

Table 6. Input port register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

6.4.2 Output port register (01h)

The Output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from this register reflect the value that was written to this register, **not** the actual pin value.

Table 7. Output port register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

6.4.3 Polarity inversion register (02h)

The Polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Table 8. Polarity inversion register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

6.4.4 Configuration register (03h)

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

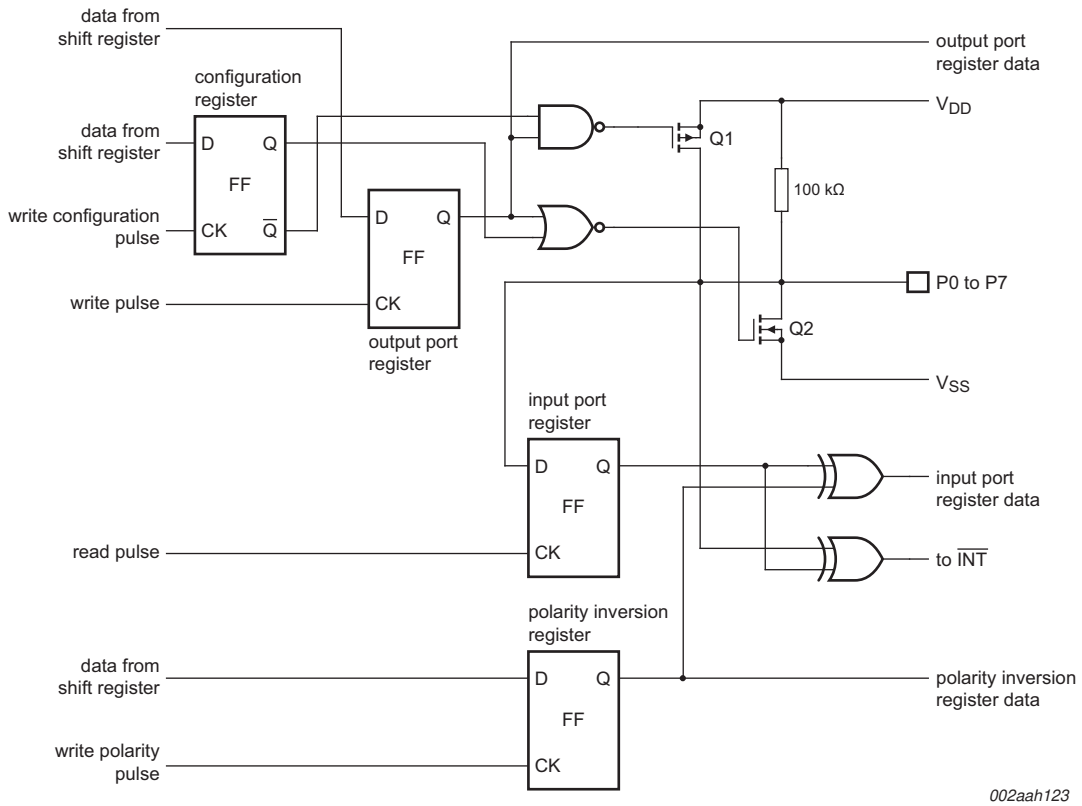
Table 9. Configuration register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{DD} or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig 6. Simplified schematic of the I/Os (P0 to P7)

6.6 Power-on reset

When power (from 0 V) is applied to V_{DD}, an internal power-on reset holds the PCA9554B/PCA9554C in a reset condition until V_{DD} has reached V_{POR}. At that time, the reset condition is released and the PCA9554B/PCA9554C registers and I²C-bus/SMBus state machine initialize to their default states. After that, V_{DD} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle. See Section 8.2 "Power-on reset requirements".

6.7 Interrupt output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt (see Figure 10). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the reset of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input port register.

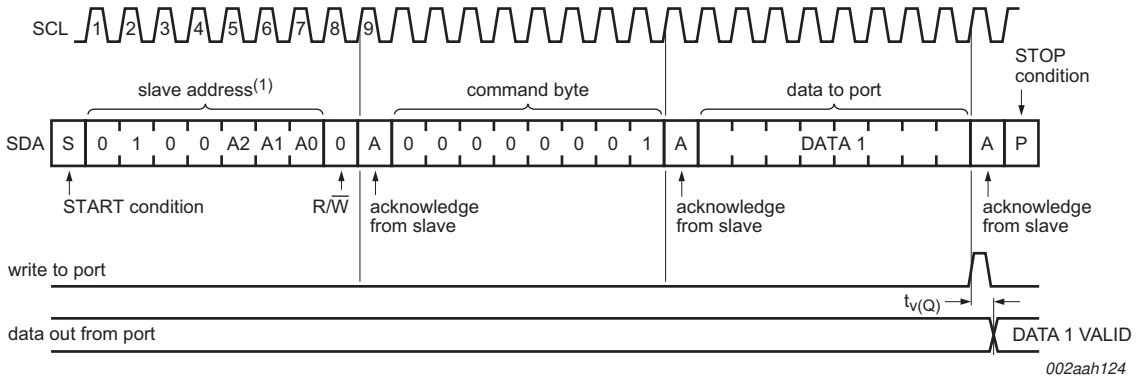
The $\overline{INT}$ output has an open-drain structure and requires a pull-up resistor to V_{DD}. $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information. When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

7. Bus transactions

The PCA9554B/PCA9554C is an I²C-bus slave device. Data is exchanged between the master and PCA9554B/PCA9554C through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

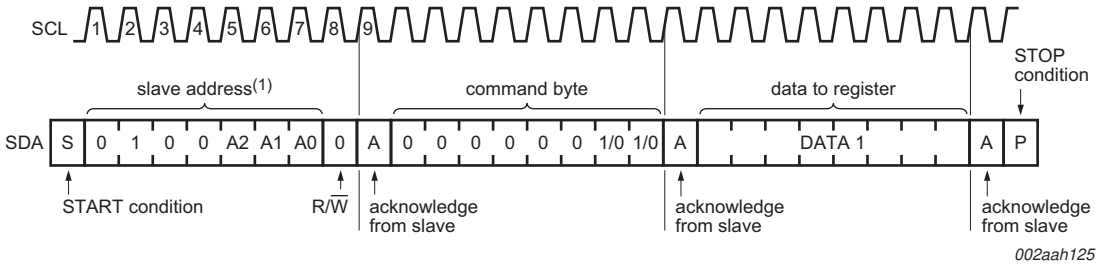
7.1 Write commands

Data is transmitted to the PCA9554B/PCA9554C by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.



(1) PCA9554B address shown. Address for PCA9554C is 0111,A2,A1,A0.

Fig 7. Write to Output port register



(1) PCA9554B address shown. Address for PCA9554C is 0111,A2,A1,A0.

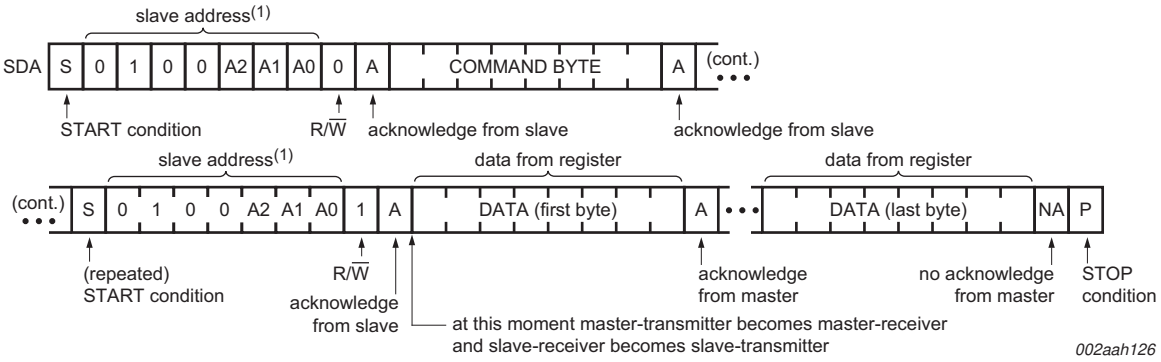
Fig 8. Write to Configuration or Polarity inversion registers

7.2 Read commands

To read data from the PCA9554B/PCA9554C, the bus master must first send the PCA9554B/PCA9554C address with the least significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is to be accessed.

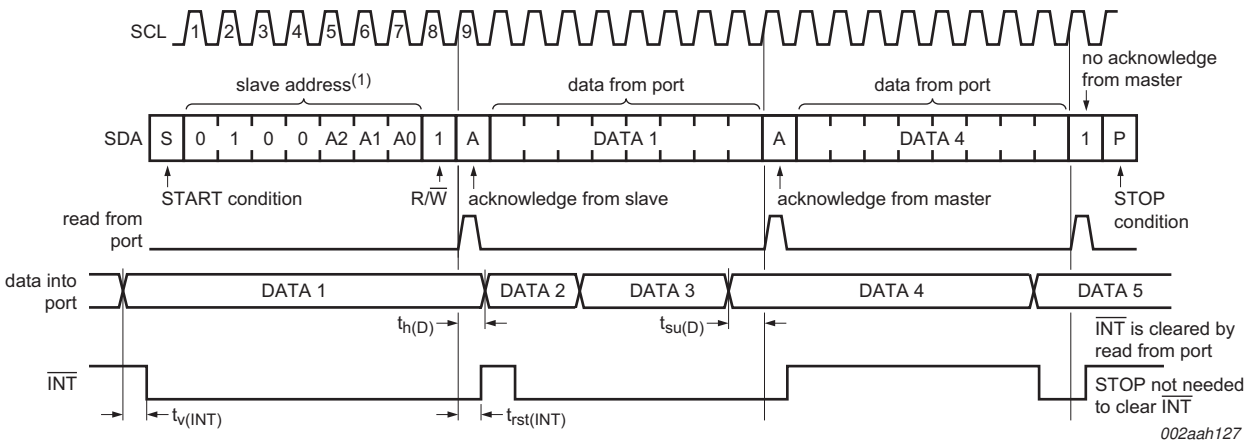
After a restart the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9554B/PCA9554C (see Figure 9 and Figure 10).

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.



(1) PCA9554B address shown. Address for PCA9554C is 0111,A2,A1,A0.

Fig 9. Read from register



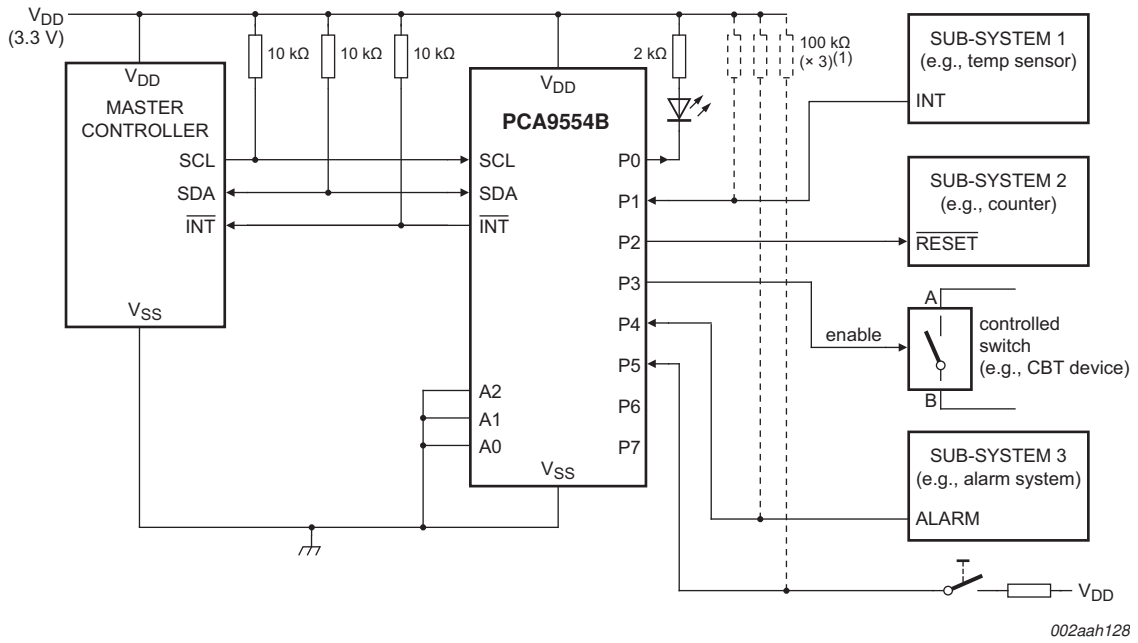
Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 9).

(1) PCA9554B address shown. Address for PCA9554C is 0111,A2,A1,A0.

Fig 10. Read Input port register

8. Application design-in information



Device address is 0100 000x for this example (PCA9554B).

P0, P2, P3 configured as outputs.

P1, P4, P5 configured as inputs.

(1) External resistors are not needed due to the internal weak pull-up resistors.

Fig 11. Typical application

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 12 and Figure 13 show typical solutions to minimizing current consumption. Figure 12 shows a high value resistor in parallel with the LED. Figure 13 shows V_{DD} less than the LED supply voltage by at least 1.2 V. However, the PCA9554B/PCA9554C needs no external resistors due to the integrated 100 kΩ pull-up resistors.

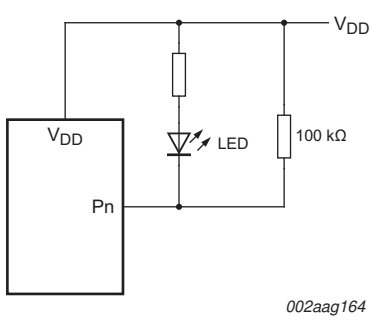


Fig 12. High value resistor in parallel with the LED

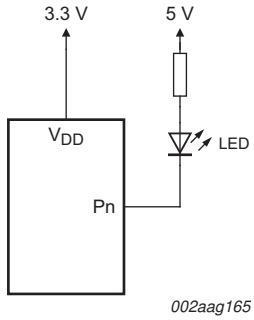


Fig 13. Device supplied by a lower voltage

8.2 Power-on reset requirements

In the event of a glitch or data corruption, PCA9554B/PCA9554C can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 14 and Figure 15.

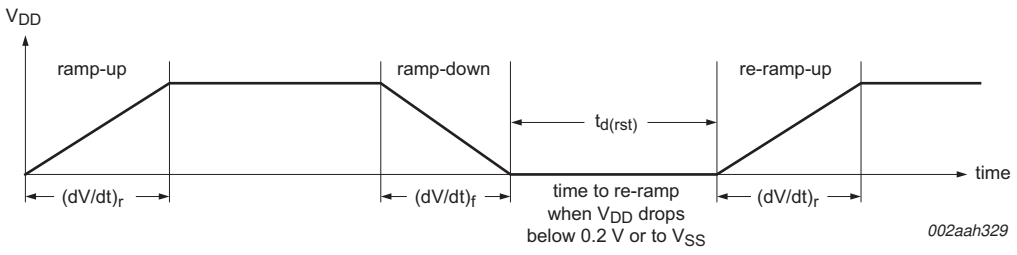


Fig 14. V_{DD} is lowered below 0.2 V or 0 V and then ramped up to V_{DD}

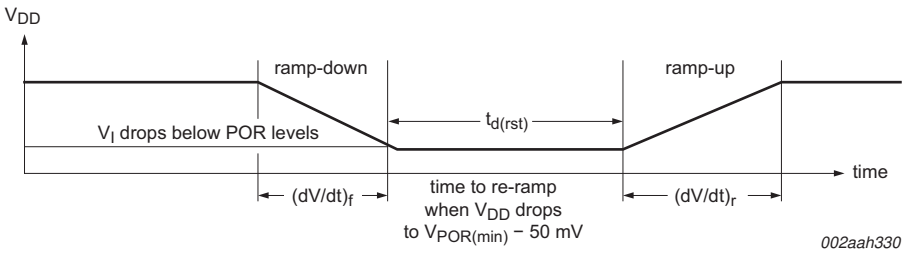


Fig 15. V_{DD} is lowered below the POR threshold, then ramped back up to V_{DD}

Table 10 specifies the performance of the power-on reset feature for PCA9554B/PCA9554C for both types of power-on reset.

Table 10. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 14		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 14		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 14; re-ramp time when V_{DD} drops to V_{SS}		1	-	-	µs
		Figure 15; re-ramp time when V_{DD} drops to $V_{POR(min)}$ − 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 16	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 16	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling V_{DD}		0.7	-	-	V
		rising V_{DD}		-	-	1.4	V

[1] Level that V_{DD} can glitch down to with a ramp rate of 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 16 and Table 10 provide more information on how to measure these specifications.

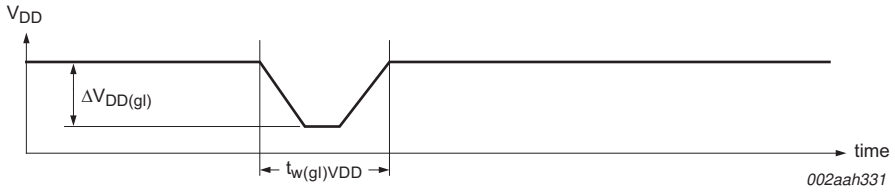


Fig 16. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 17 and Table 10 provide more details on this specification.

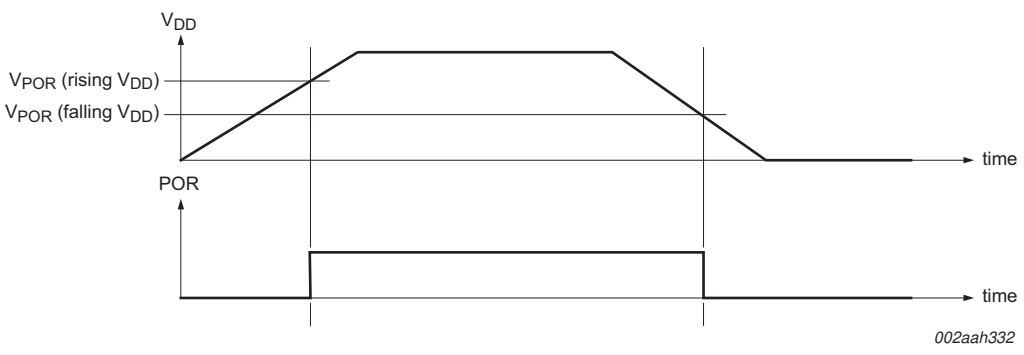


Fig 17. Power-on reset voltage (V_{POR})

8.3 Device current consumption with internal pull-up resistors

The PCA9554B/PCA9554C integrates pull-up resistors to eliminate external components when pins are configured as inputs and pull-up resistors are required (for example, nothing is driving the inputs to the power supply rails). Since these pull-up resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The internal pull-up resistor is connected to V_{DD}, a current will flow from the V_{DD} pin through the resistor to ground when the pin is held LOW. This current will appear as additional I_{DD} upsetting any current consumption measurements.

The pull-up resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flow through these resistors is additive by the number of pins held LOW and the current can be calculated by Ohm's law. See Figure 21 for a graph of supply current versus the number of pull-up resistors.

9. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.5	V
V_I	input voltage		[1]	−0.5	+6.5	V
V_O	output voltage		[1]	−0.5	+6.5	V
I_{IK}	input clamping current	A0, A1, A2, SCL; $V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD}$		-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD}$		-	±20	mA
I_{OL}	LOW-level output current	continuous; I/O port		-	50	mA
		continuous; SDA, $\overline{INT}$		-	25	mA
I_{OH}	HIGH-level output current	continuous; P port		-	25	mA
I_{DD}	supply current			-	160	mA
I_{SS}	ground supply current			-	200	mA
P_{tot}	total power dissipation			-	200	mW
T_{stg}	storage temperature			−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

10. Recommended operating conditions

Table 12. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA		$0.7 \times V_{DD}$	5.5	V
		A0, A1, A2, P port		$0.7 \times V_{DD}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA		−0.5	$0.3 \times V_{DD}$	V
		A0, A1, A2, P port		−0.5	$0.3 \times V_{DD}$	V
I_{OH}	HIGH-level output current	P port		-	10	mA
I_{OL}	LOW-level output current	P port		-	25	mA
T_{amb}	ambient temperature	operating in free air		−40	+85	°C

11. Thermal characteristics

Table 13. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	HVQFN16 package	[1]	53	K/W
		TSSOP16 package	[1]	108	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

12. Static characteristics

Table 14. Static characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA		−1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD}$ or V_{SS}; I_O = 0 mA		-	1.1	1.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 1.65 V to 5.5 V					
		SDA		3	-	-	mA
		$\overline{INT}$		3	15[2]	-	mA
		P port					
		V_{OL} = 0.5 V; V_{DD} = 1.65 V	[3]	8	10	-	mA
		V_{OL} = 0.7 V; V_{DD} = 1.65 V	[3]	10	13	-	mA
		V_{OL} = 0.5 V; V_{DD} = 2.3 V	[3]	8	10	-	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V	[3]	10	13	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[3]	8	14	-	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V	[3]	10	19	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[3]	8	17	-	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V	[3]	10	24	-	mA
V_{OH}	HIGH-level output voltage	P port					
		I_{OH} = −8 mA; V_{DD} = 1.65 V	[4]	1.2	-	-	V
		I_{OH} = −10 mA; V_{DD} = 1.65 V	[4]	1.1	-	-	V
		I_{OH} = −8 mA; V_{DD} = 2.3 V	[4]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V	[4]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V	[4]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V	[4]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V	[4]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V	[4]	4.0	-	-	V
I_I	input current	V_{DD} = 1.65 V to 5.5 V					
		SCL, SDA; $V_I = V_{DD}$ or V_{SS}		-	-	0.1	µA
		A0, A1, A2; $V_I = V_{DD}$ or V_{SS}		-	-	±1	µA
I_{IH}	HIGH-level input current	P port; $V_I = V_{DD}$; V_{DD} = 1.65 V to 5.5 V		-	-	1	µA
I_{IL}	LOW-level input current	P port; $V_I = V_{SS}$; V_{DD} = 1.65 V to 5.5 V		-	-	−100	µA

Table 14. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	SDA, P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz					
		V_{DD} = 3.6 V to 5.5 V		-	10	25	µA
		V_{DD} = 2.3 V to 3.6 V		-	6.5	15	µA
		V_{DD} = 1.65 V to 2.3 V		-	4	9	µA
		SCL, SDA, P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz					
		V_{DD} = 3.6 V to 5.5 V		-	1.5	7	µA
		V_{DD} = 2.3 V to 3.6 V		-	1	3.2	µA
		V_{DD} = 1.65 V to 2.3 V		-	0.5	1.7	µA
		Active mode; P port, A0, A1, A2; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz, continuous register read					
		V_{DD} = 3.6 V to 5.5 V		-	60	125	µA
		V_{DD} = 2.3 V to 3.6 V		-	40	75	µA
		V_{DD} = 1.65 V to 2.3 V		-	20	45	µA
		with pull-ups; P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port = V_{SS}; V_I on A0, A1, A2 = V_{DD} or V_{SS}; I_O = 0 mA; I/O = inputs with pull-up; f_{SCL} = 0 kHz					
		V_{DD} = 1.65 V to 5.5 V		-	0.55	0.75	mA
ΔI_{DD}	additional quiescent supply current	SCL, SDA; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V		-	-	25	µA
		P port, A0, A1, A2; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V		-	-	80	µA
C_i	input capacitance	V_I = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V		-	6	7	pF
C_{io}	input/output capacitance	$V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V		-	7	8	pF
		$V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V		-	7.5	8.5	pF
$R_{pu(int)}$	internal pull-up resistance	input/output		50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at V_{DD} = 3.3 V and T_{amb} = 25 °C.

[2] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{DD} = 3.3 V. Typical value for V_{DD} < 2.5 V, V_{OL} = 0.6 V.

[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[4] The total current sourced by all I/Os must be limited to 85 mA.

12.1 Typical characteristics

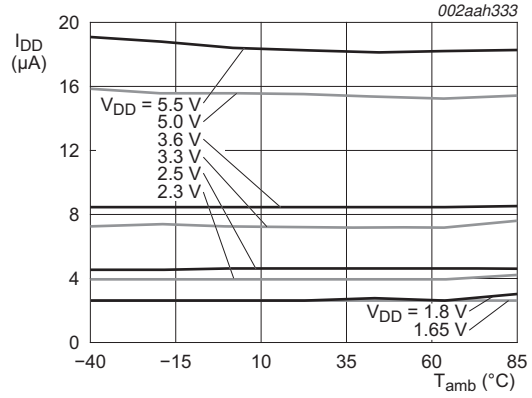


Fig 18. Supply current versus ambient temperature

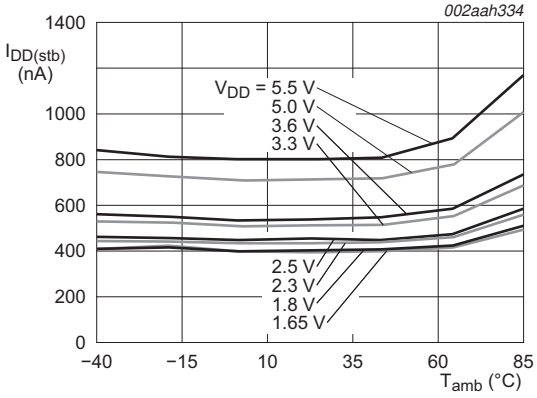


Fig 19. Standby supply current versus ambient temperature

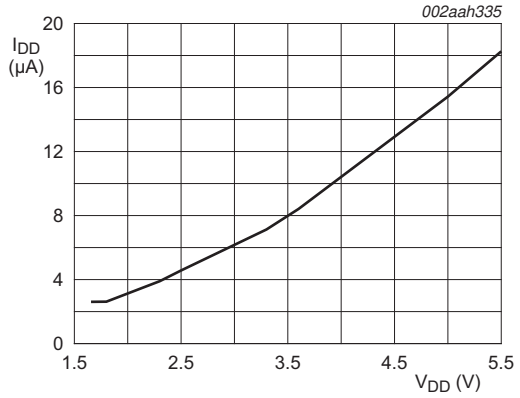


Fig 20. Supply current versus supply voltage

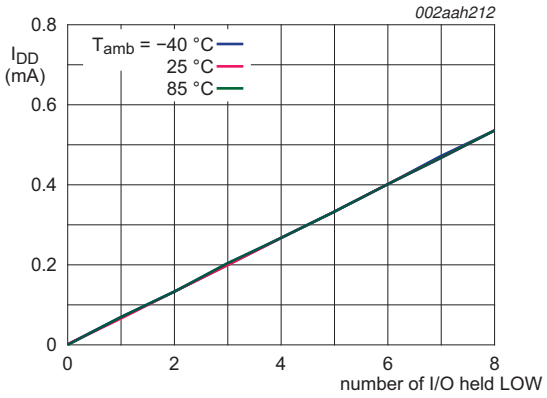
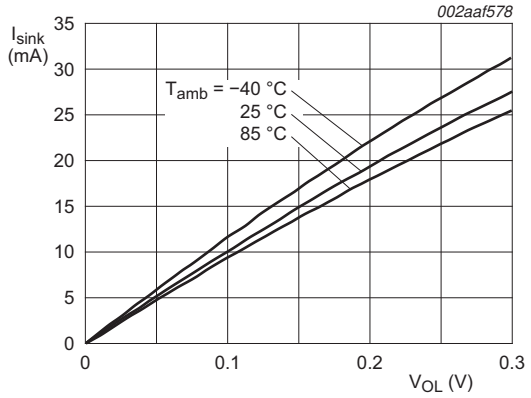
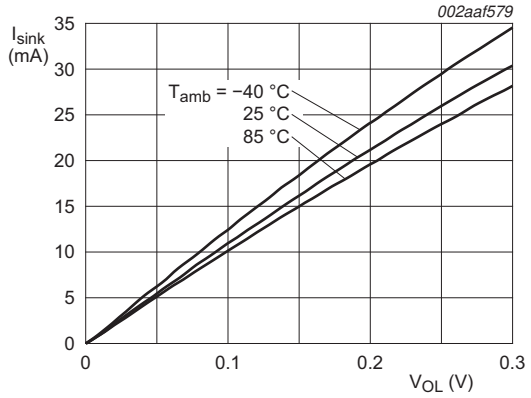


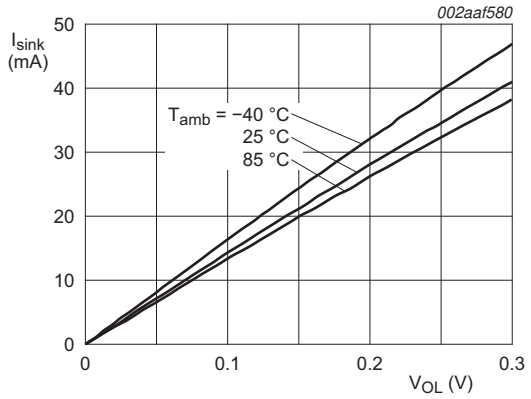
Fig 21. Supply current versus number of I/O held LOW



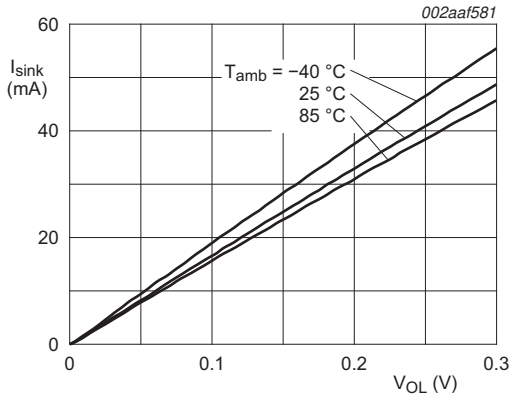
a. V_{DD} = 1.65 V



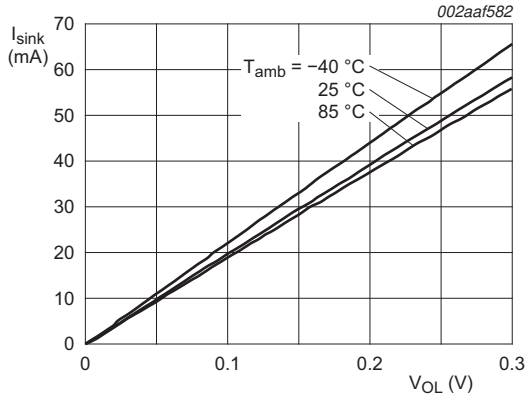
b. V_{DD} = 1.8 V



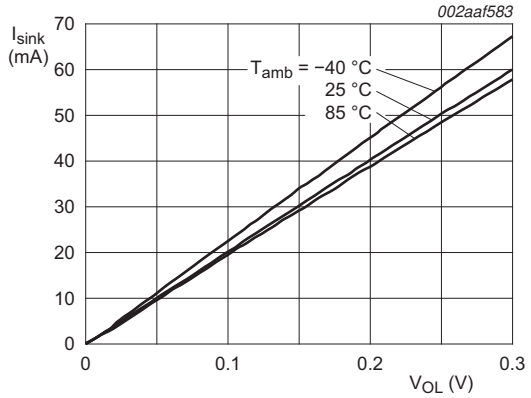
c. V_{DD} = 2.5 V



d. V_{DD} = 3.3 V

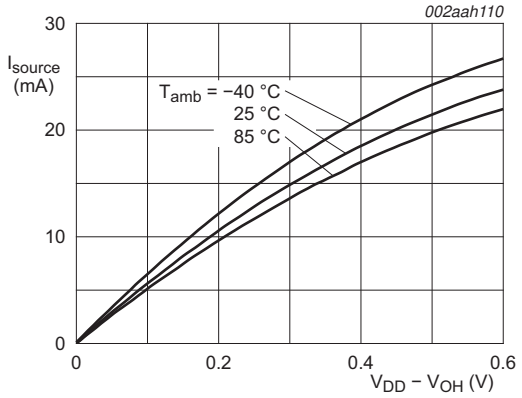


e. V_{DD} = 5.0 V

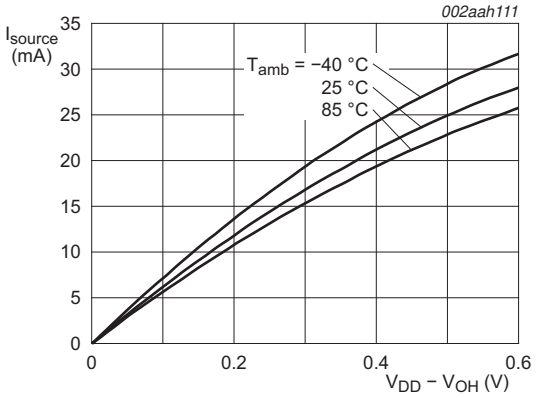


f. V_{DD} = 5.5 V

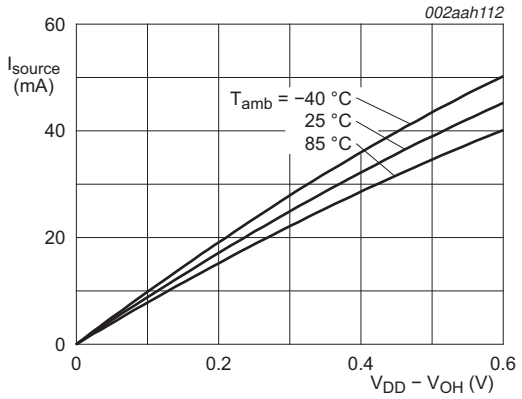
Fig 22. I/O sink current versus LOW-level output voltage



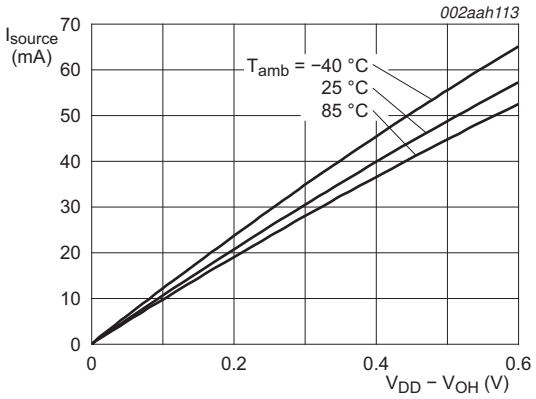
a. V_{DD} = 1.65 V



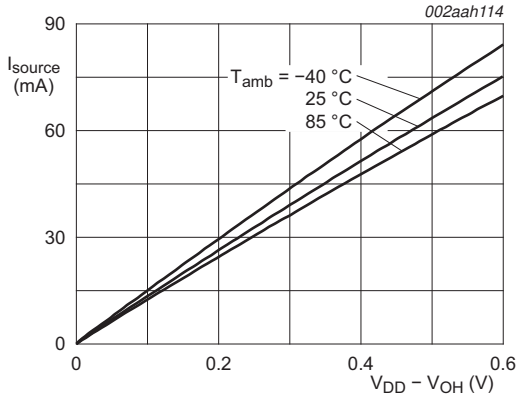
b. V_{DD} = 1.8 V



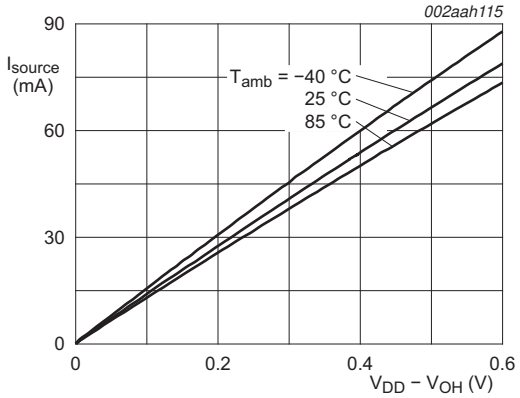
c. V_{DD} = 2.5 V



d. V_{DD} = 3.3 V

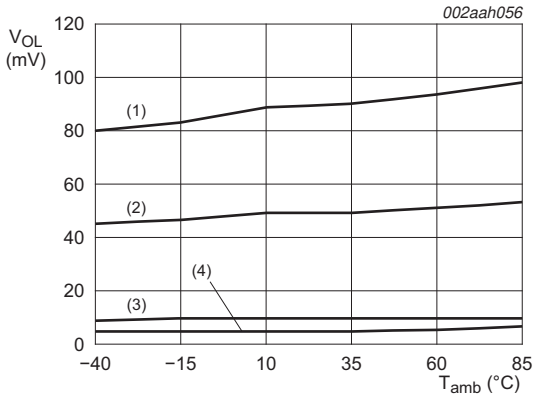


e. V_{DD} = 5.0 V



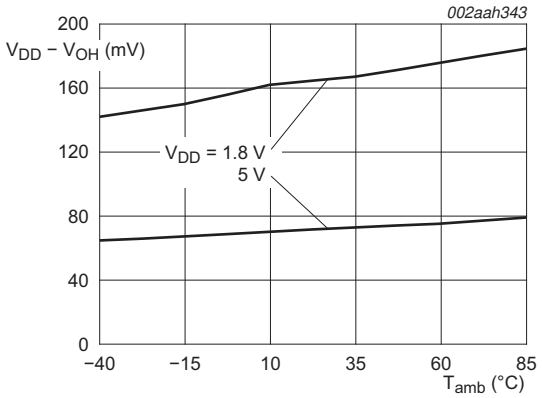
f. V_{DD} = 5.5 V

Fig 23. I/O source current versus HIGH-level output voltage



(1) V_{DD} = 1.8 V; I_{sink} = 10 mA
(2) V_{DD} = 5 V; I_{sink} = 10 mA
(3) V_{DD} = 1.8 V; I_{sink} = 1 mA
(4) V_{DD} = 5 V; I_{sink} = 1 mA

Fig 24. LOW-level output voltage versus temperature



I_{source} = −10 mA

Fig 25. I/O high voltage versus temperature

13. Dynamic characteristics

Table 15. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 26.

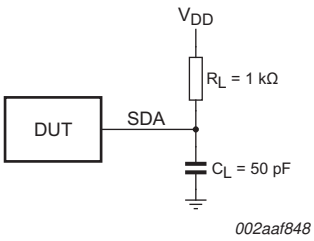
Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock			4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter			0	50	0	50	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
t_r	rise time of both SDA and SCL signals			-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals			-	300	$20 \times (V_{DD} / 5.5\ V)$	300	ns
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4	-	0.6	-	µs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid		-	3.45	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW		-	3.45	-	0.9	µs

Table 16. Switching characteristics

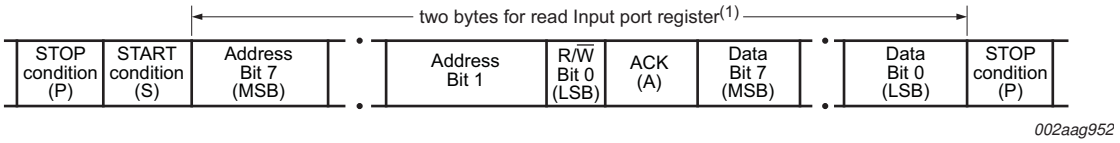
Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 26.

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$		-	1	-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$		-	1	-	1	µs
$t_{v(Q)}$	data output valid time	from SCL to P port		-	400	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCL		0	-	0	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL		300	-	300	-	ns

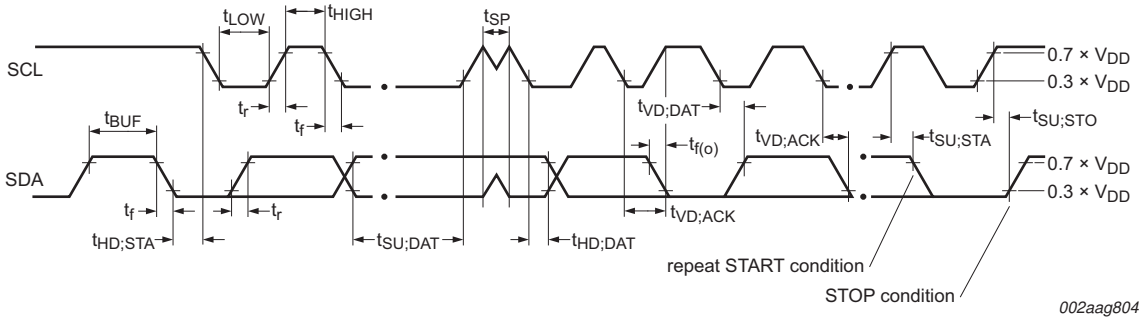
14. Parameter measurement information



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

C_L includes probe and jig capacitance.

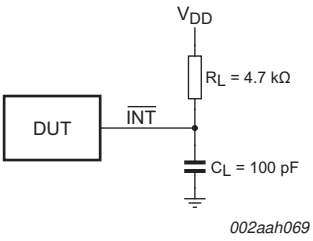
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

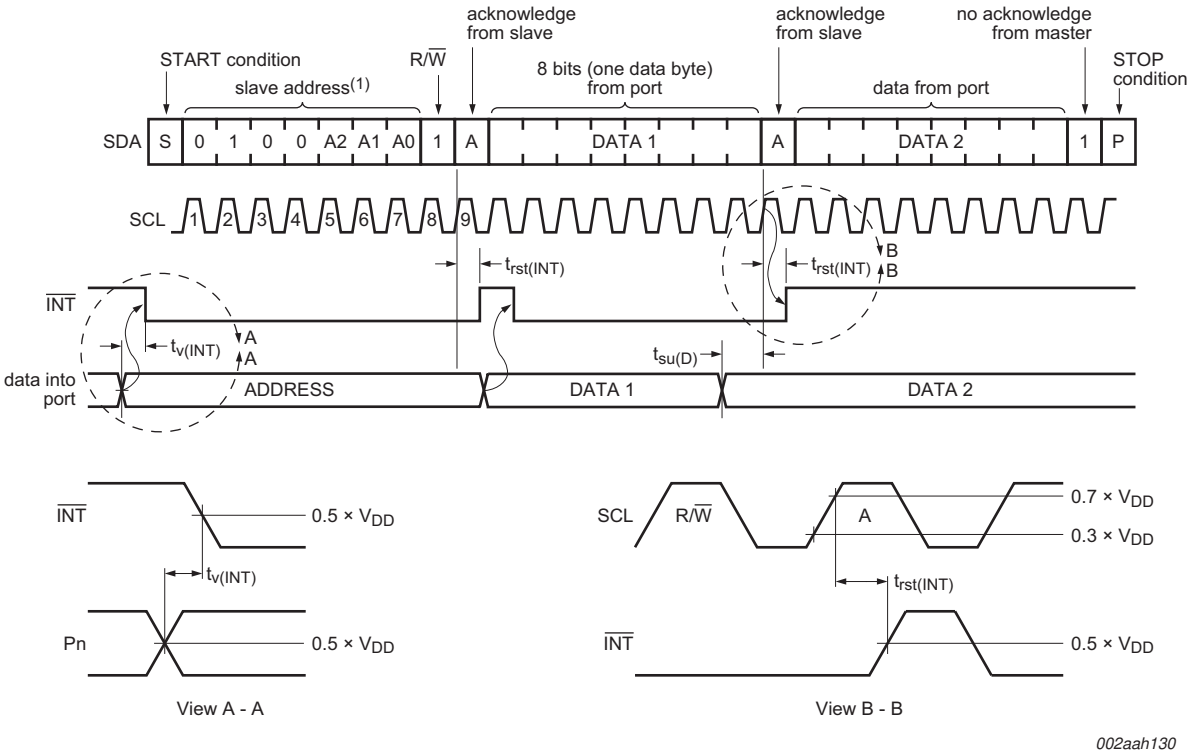
Byte 1 = I²C-bus address; Byte 2, byte 3 = P port data.

(1) See Figure 9.

Fig 26. I²C-bus interface load circuit and voltage waveforms



a. Interrupt load configuration



b. Voltage waveforms

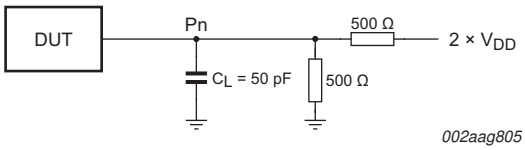
C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

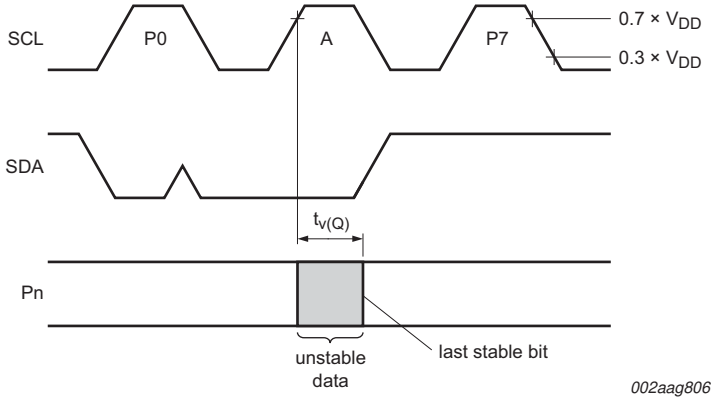
All parameters and waveforms are not applicable to all devices.

(1) PCA9554B address shown. Address for PCA9554C is 0111,A2,A1,A0.

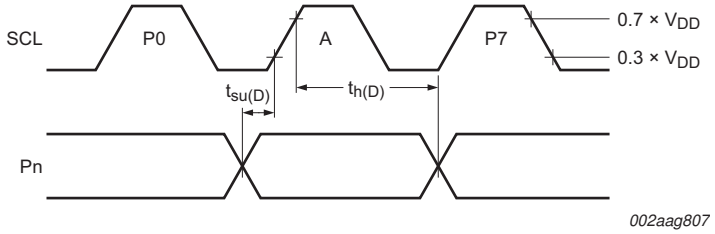
Fig 27. Interrupt load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

$t_{v(Q)}$ is measured from 0.7 × V_{DD} on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 28. P port load circuit and voltage waveforms