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PCA9555

16-bit I²C-bus and SMBus I/O port with interrupt

Product data sheet

1. General description

The PCA9555 is a 24-pin CMOS device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9555 consists of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master. Although pin-to-pin and I²C-bus address compatible with the PCF8575, software changes are required due to the enhancements, and are discussed in *Application Note AN469*.

The PCA9555 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus. The fixed I²C-bus address of the PCA9555 is the same as the PCA9554, allowing up to eight of these devices in any combination to share the same I²C-bus/SMBus.

2. Features

■ Operating power supply voltage range of 2.3 V to 5.5 V
■ 5 V tolerant I/Os
■ Polarity Inversion register
■ Active LOW interrupt output
■ Low standby current
■ Noise filter on SCL/SDA inputs
■ No glitch on power-up
■ Internal power-on reset
■ 16 I/O pins which default to 16 inputs
■ 0 Hz to 400 kHz clock frequency
■ ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101

■ Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
■ Six packages offered: DIP24, SO24, SSOP24, TSSOP24, HVQFN24 and HWQFN24

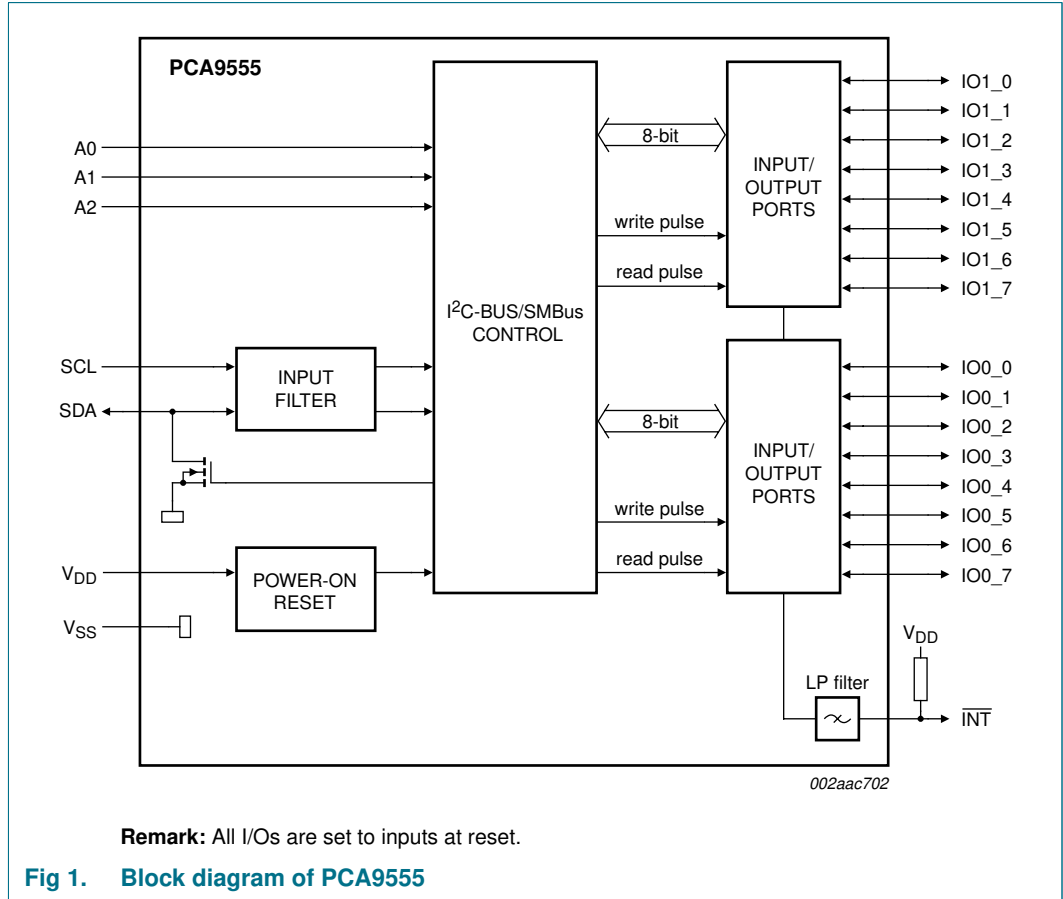## 3. Ordering information

Table 1.   Ordering information

Type number	Package			Version
	Name	**Description**		
PCA9555N	DIP24	plastic dual in-line package; 24 leads (600 mil)		SOT101-1
PCA9555D	SO24	plastic small outline package; 24 leads; body width 7.5 mm		SOT137-1
PCA9555DB	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm		SOT340-1
PCA9555PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm		SOT355-1
PCA9555BS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body $4 \times 4 \times 0.85$ mm		SOT616-1
PCA9555HF	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body $4 \times 4 \times 0.75$ mm		SOT994-1

3.1 Ordering options

Table 2.   Ordering options

Type number	Topside mark	Temperature range
PCA9555N	PCA9555	−40 °C to +85 °C
PCA9555D	PCA9555D	−40 °C to +85 °C
PCA9555DB	PCA9555	−40 °C to +85 °C
PCA9555PW	PCA9555	−40 °C to +85 °C
PCA9555BS	9555	−40 °C to +85 °C
PCA9555HF	P55H	−40 °C to +85 °C

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4. Block diagram

Remark: All I/Os are set to inputs at reset.

Fig 1. **Block diagram of PCA9555**

5. Pinning information

5.1 Pinning

Fig 2. **Pin configuration for DIP24**

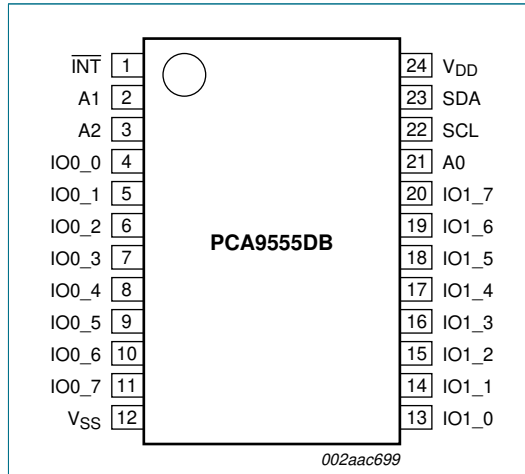**Fig 3.** **Pin configuration for SO24**
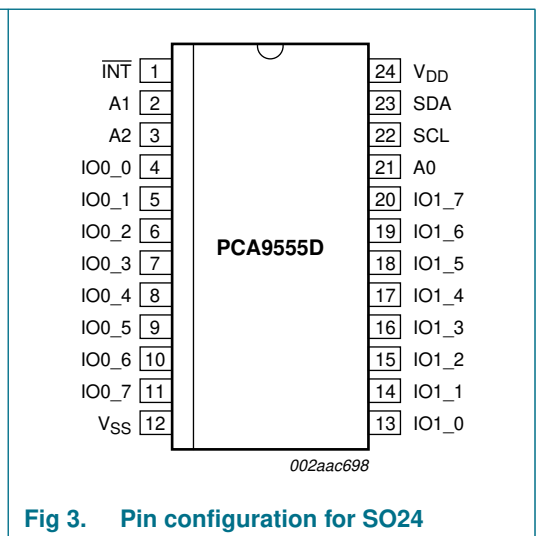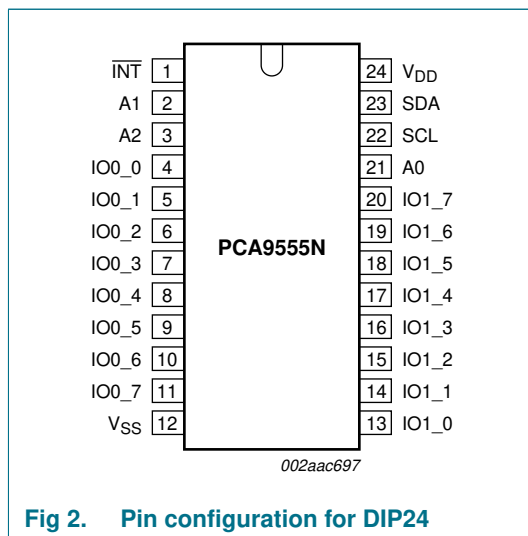
Fig 4.   Pin configuration for SSOP24
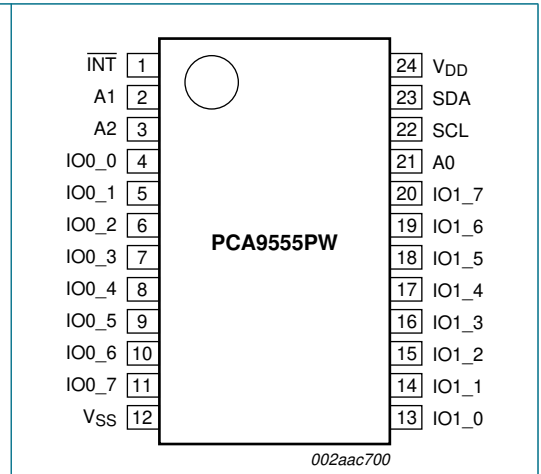

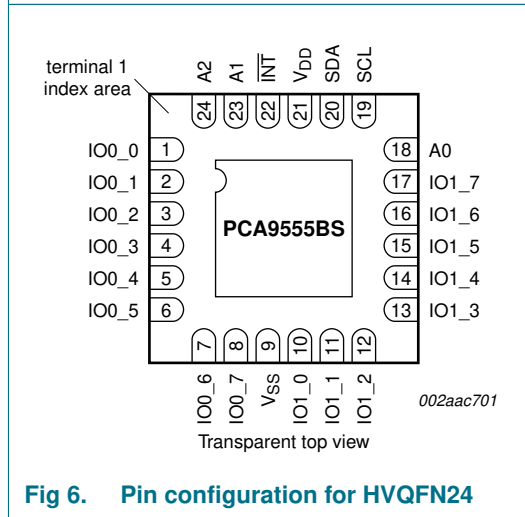**Fig 5.   Pin configuration for TSSOP24**

Fig 6.   Pin configuration for HVQFN24
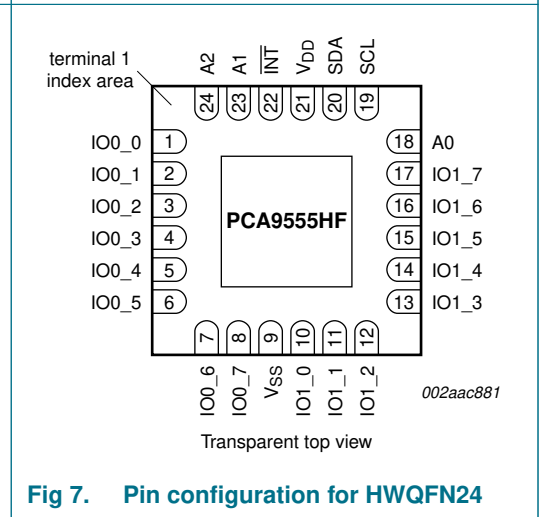
Fig 7.   Pin configuration for HWQFN24

5.2 Pin description

Table 3.   Pin description

Symbol	Pin		Description
	DIP24, SO24, SSOP24, TSSOP24	**HVQFN24, HWQFN24**	
$\overline{INT}$	1	22	interrupt output (open-drain)
A1	2	23	address input 1
A2	3	24	address input 2
IO0_0	4	1	port 0 input/output
IO0_1	5	2	
IO0_2	6	3	
IO0_3	7	4	
IO0_4	8	5	
IO0_5	9	6	
IO0_6	10	7	
IO0_7	11	8	
V_{SS}	12	9[1]	supply ground
IO1_0	13	10	port 1 input/output
IO1_1	14	11	
IO1_2	15	12	
IO1_3	16	13	
IO1_4	17	14	
IO1_5	18	15	
IO1_6	19	16	
IO1_7	20	17	
A0	21	18	address input 0
SCL	22	19	serial clock line
SDA	23	20	serial data line
V_{DD}	24	21	supply voltage

[1]   HVQFN and HWQFN package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

Refer to Figure 1 "Block diagram of PCA9555".

6.1 Device address

Fig 8.   PCA9555 device address
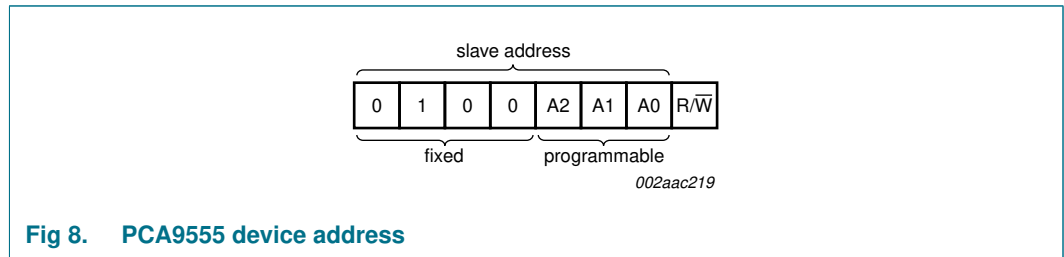
6.2 Registers

6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 4.   Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity Inversion port 0
5	Polarity Inversion port 1
6	Configuration port 0
7	Configuration port 1

6.2.2 Registers 0 and 1: Input port registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5. **Input port 0 Register**

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6. **Input port 1 register**

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

6.2.3 Registers 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 7. **Output port 0 register**

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8. **Output port 1 register**

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

6.2.4 Registers 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 9. **Polarity Inversion port 0 register**

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10. **Polarity Inversion port 1 register**

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

6.2.5 Registers 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to V_{DD} at each pin. At reset, the device's ports are inputs with a pull-up to V_{DD}.

Table 11. Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12. Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

6.3 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9555 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9555 registers and SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

6.4 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either V_{DD} or V_{SS}.

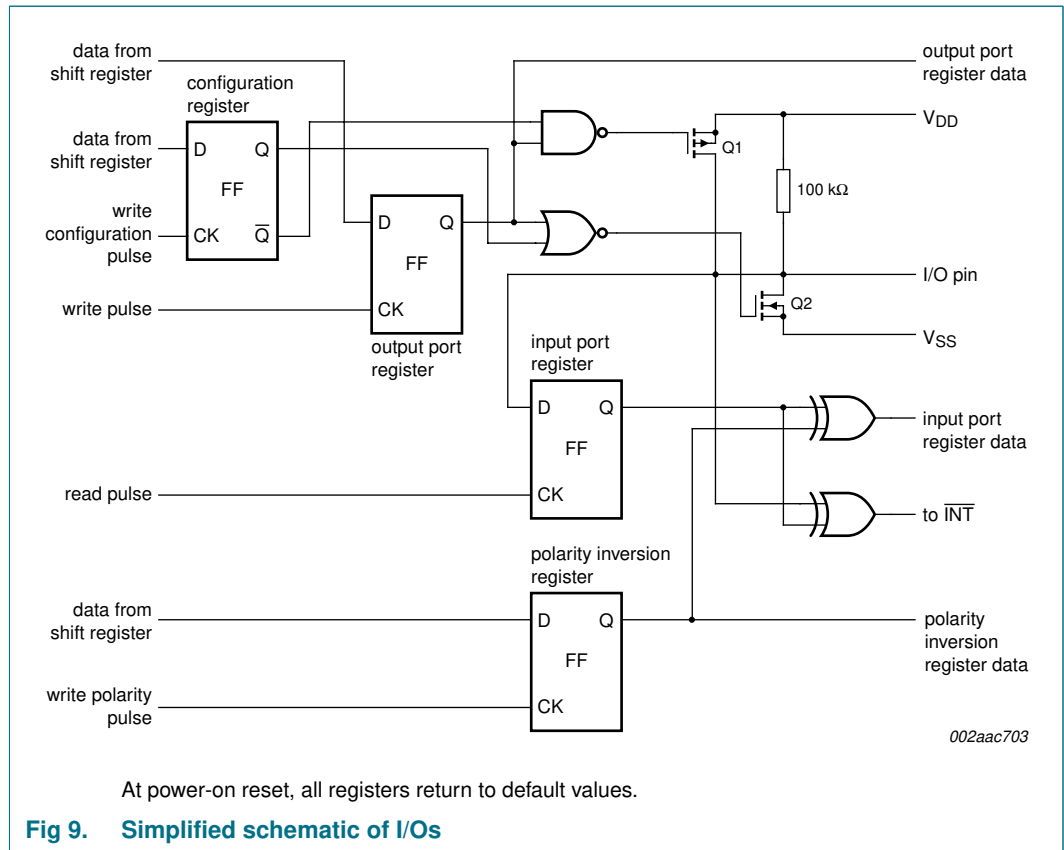At power-on reset, all registers return to default values.

Fig 9. **Simplified schematic of I/Os**

## 6.5 Bus transactions

6.5.1 Writing to the port registers

Data is transmitted to the PCA9555 by sending the device address and setting the least significant bit to a logic 0 (see Figure 8 "PCA9555 device address"). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the PCA9555 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 10 and Figure 11). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

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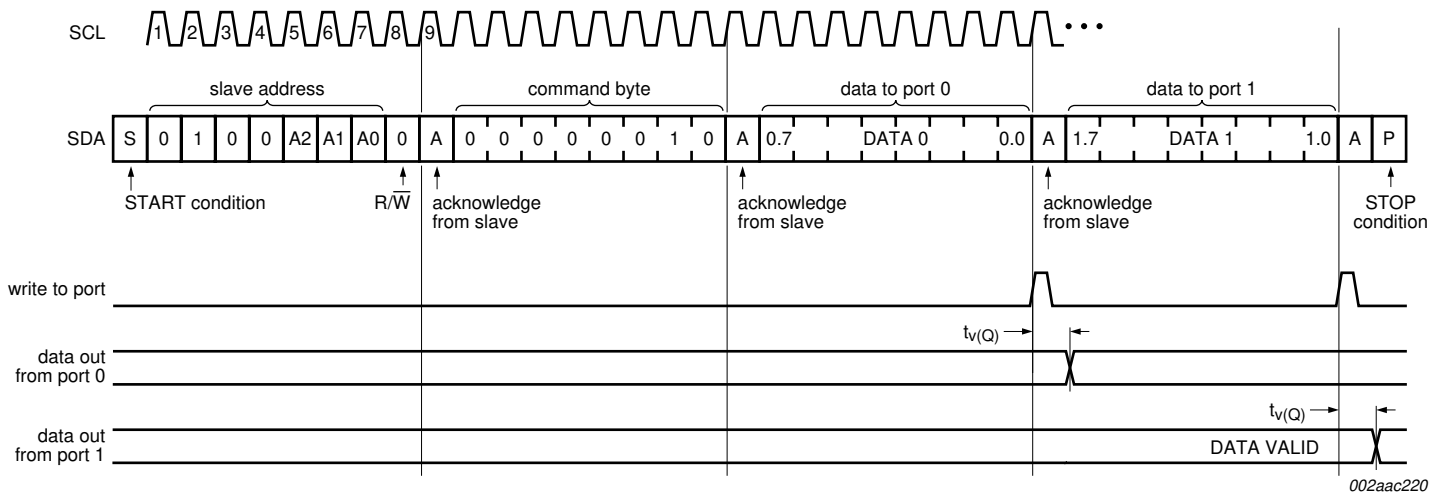
Fig 10.   Write to Output port registers
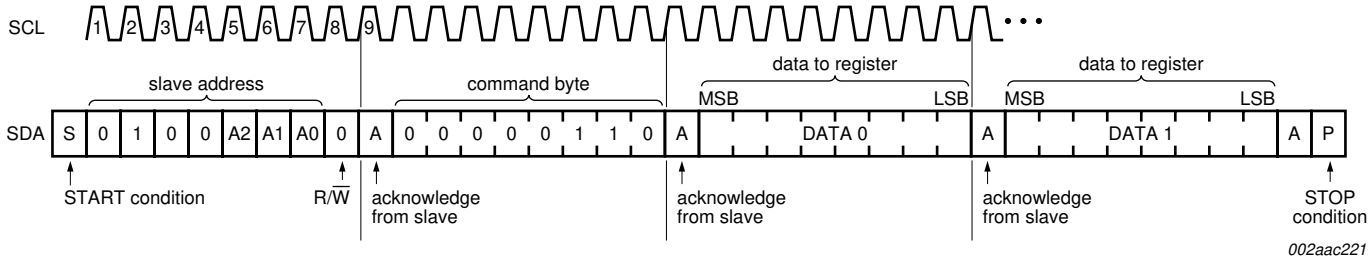
**Fig 11.   Write to Configuration registers**

6.5.2 Reading the port registers

In order to read data from the PCA9555, the bus master must first send the PCA9555 address with the least significant bit set to a logic 0 (see Figure 8 "PCA9555 device address"). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PCA9555 (see Figure 12, Figure 13 and Figure 14). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.
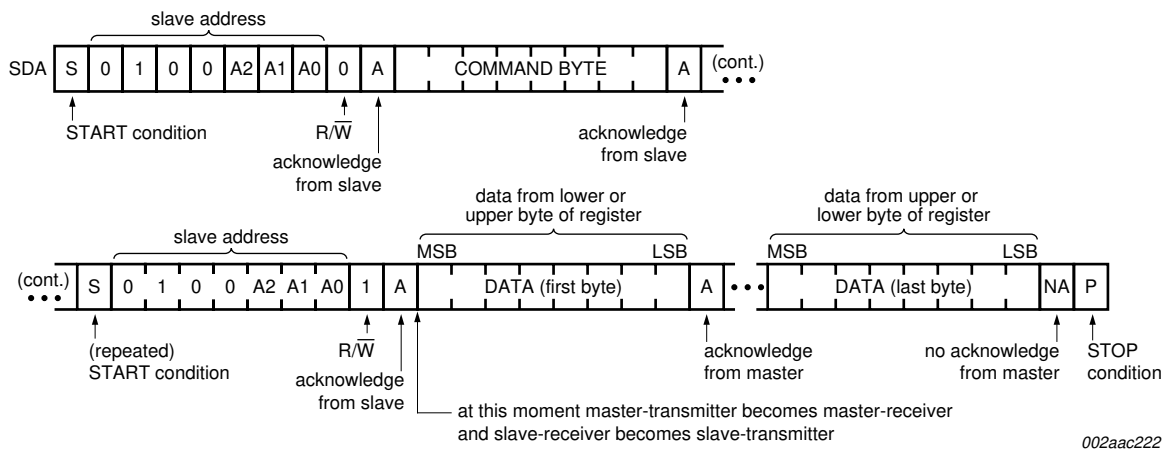
Remark: Transfer can be stopped at any time by a STOP condition.

Fig 12. Read from register
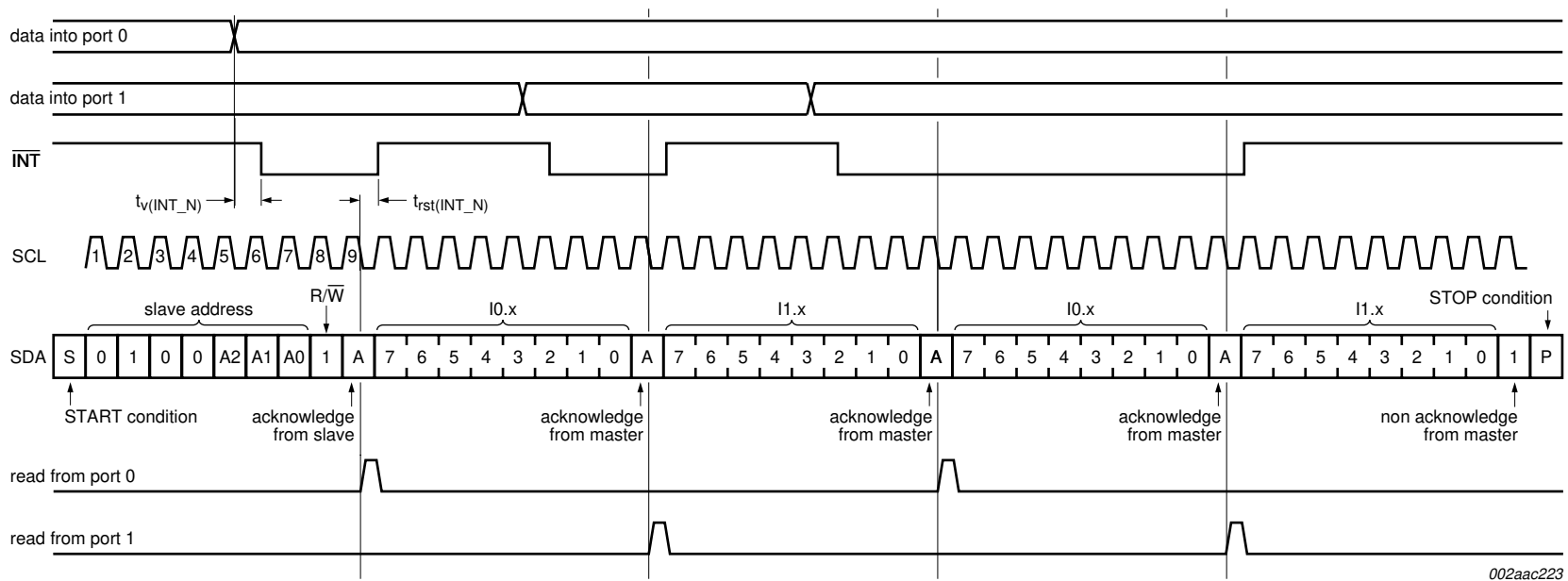
Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Fig 13. Read Input port register, scenario 1
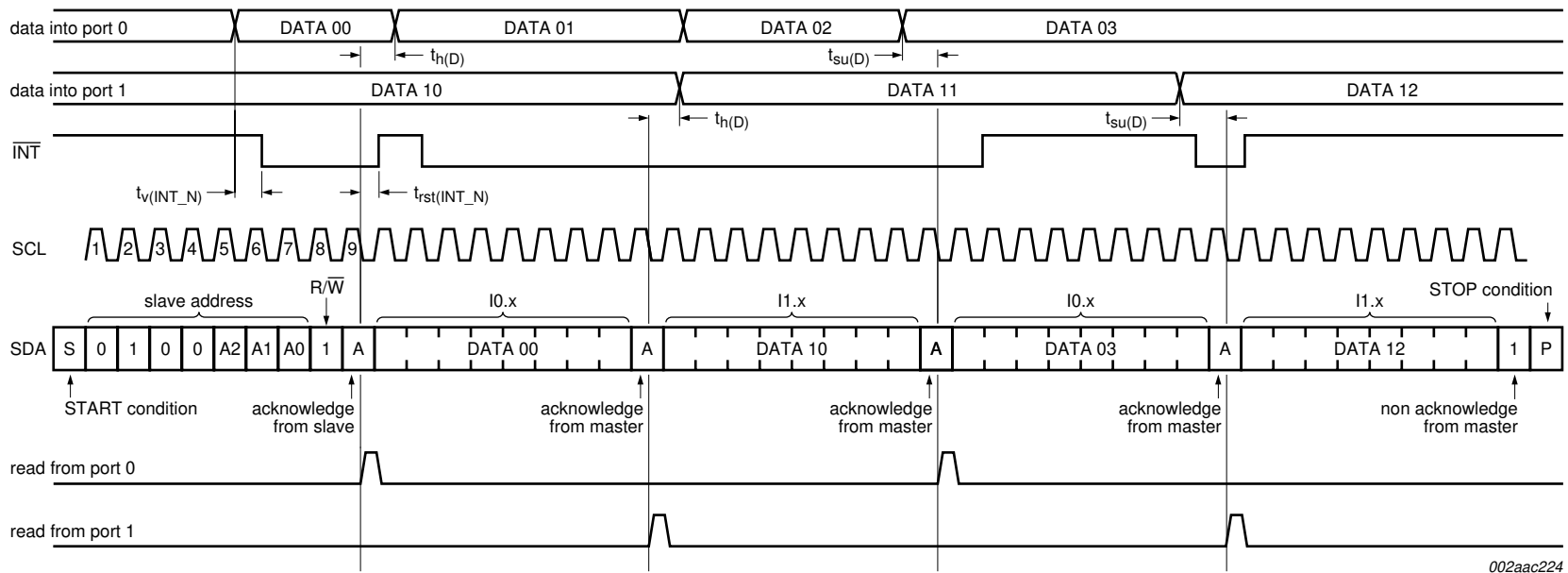
Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Fig 14.   Read Input port register, scenario 2

6.5.3 Interrupt output

The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read (see Figure 13). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

7. Characteristics of the I2C-bus

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 15).

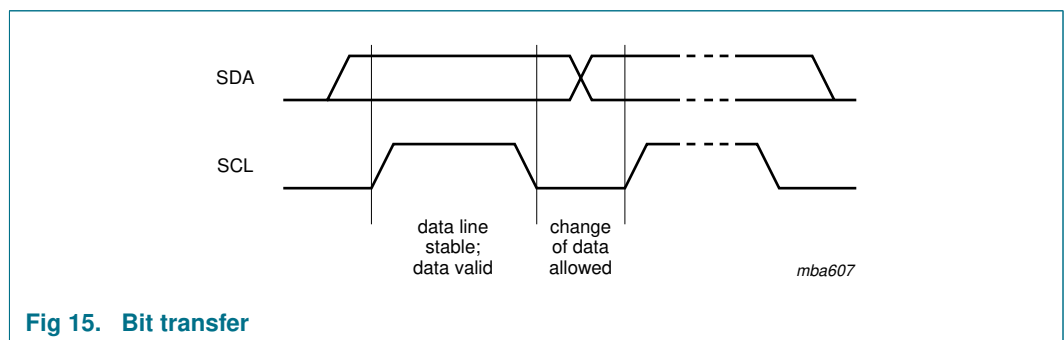**Fig 15. Bit transfer**

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 16).
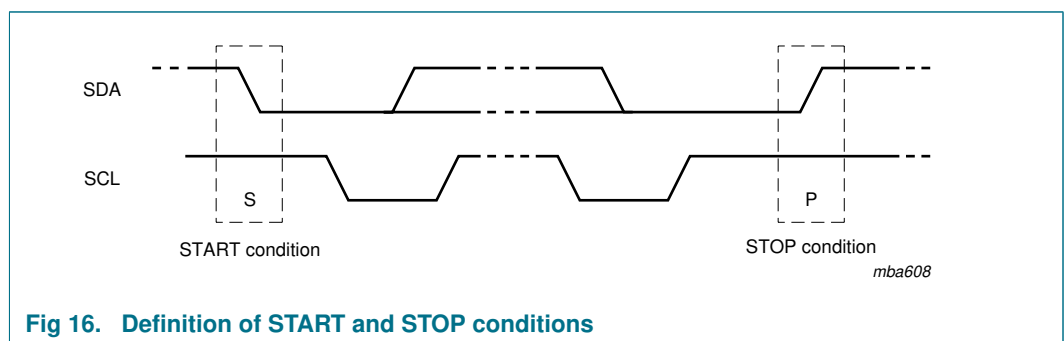
Fig 16.   Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 17).
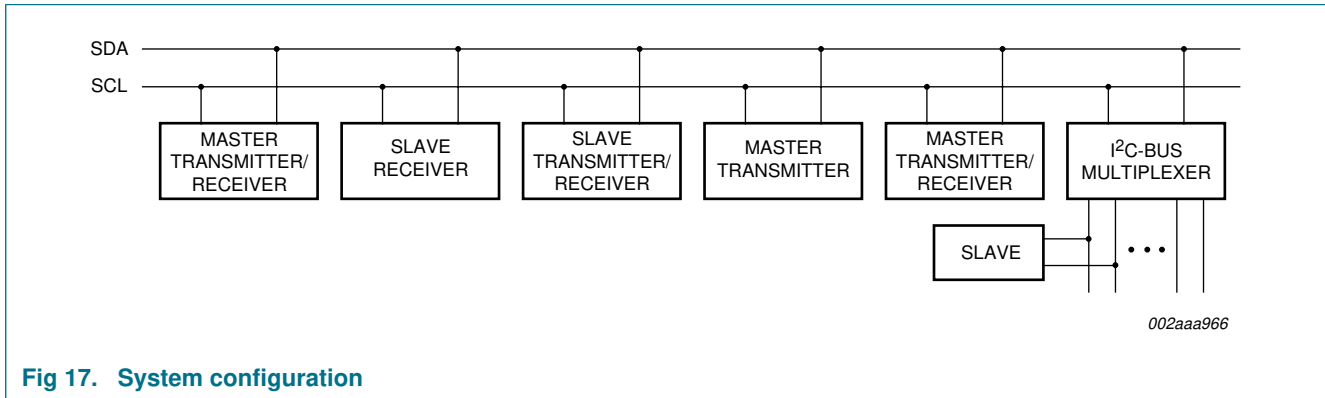
Fig 17. System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.
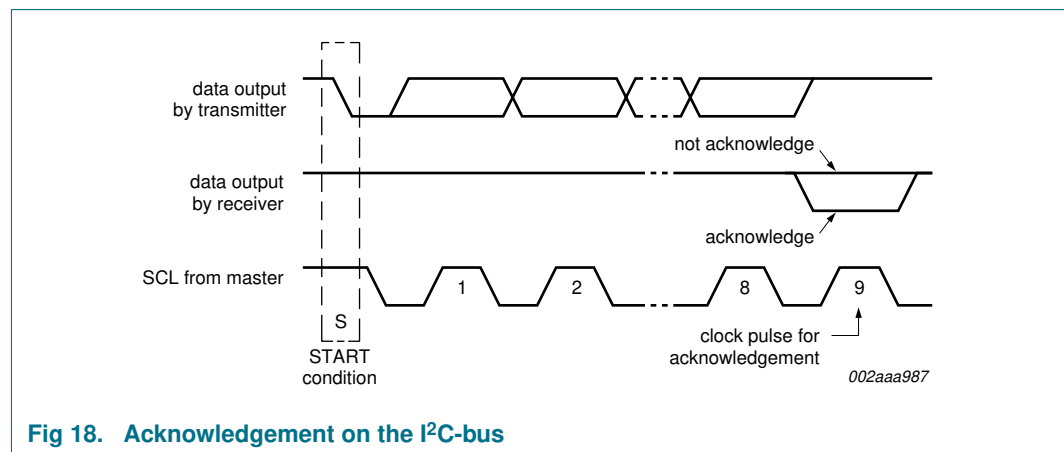
Fig 18. Acknowledgement on the I²C-bus

8. Application design-in information

Device address configured as 0100 000xb for this example.

IO0_0, IO0_2, IO0_3 configured as outputs.

IO0_1, IO0_4, IO0_5 configured as inputs.

IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.
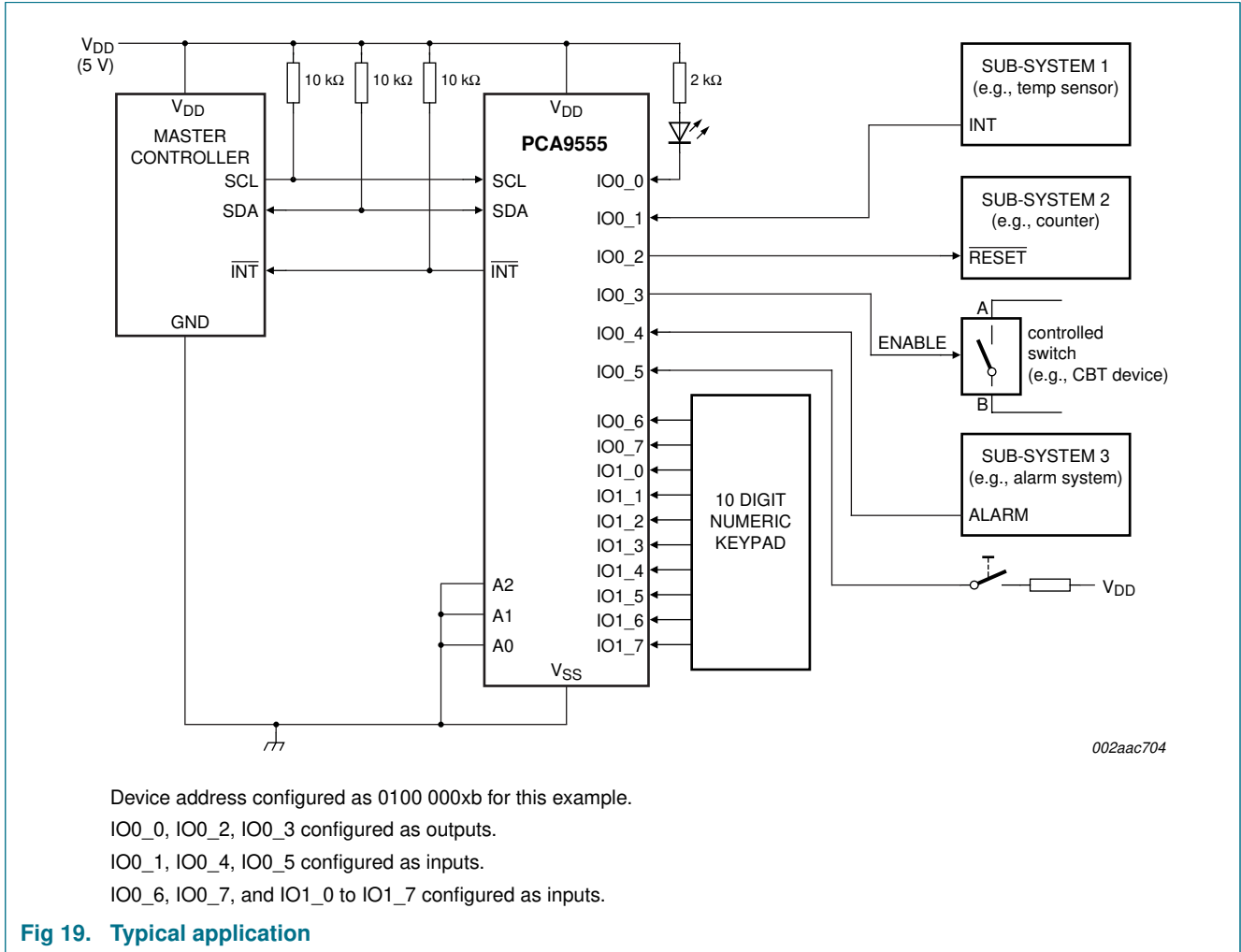
Fig 19. Typical application

9. Limiting values

Table 13.   Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		$V_{SS} - 0.5$	6	V
I_O	output current	on an I/O pin	-	±50	mA
I_I	input current		-	±20	mA
I_{DD}	supply current		-	160	mA
I_{SS}	ground supply current		-	200	mA
P_{tot}	total power dissipation		-	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C

10. Static characteristics

Table 14. **Static characteristics**

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz		-	135	200	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs		-	1.1	1.5	mA
		Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
V_{POR}	power-on reset voltage[1]	no load; V_I = V_{DD} or V_{SS}		-	1.5	1.65	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
I_L	leakage current	V_I = V_{DD} = V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.5 V	[2]	8	(8 to 20)	-	mA
		V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.7 V	[2]	10	(10 to 24)	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; V_{DD} = 2.3 V	[3]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V	[3]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V	[3]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V	[3]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V	[3]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V	[3]	4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 5.5 V; V_I = V_{DD}		-	-	1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; V_I = V_{SS}		-	-	−100	µA
C_i	input capacitance			-	3.7	5	pF
C_o	output capacitance			-	3.7	5	pF
Interrupt INT							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
Select inputs A0, A1, A2							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA

[1] V_{DD} must be lowered to 0.2 V for at least 5 µs in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.

[3] The total current sourced by all I/Os must be limited to 160 mA.
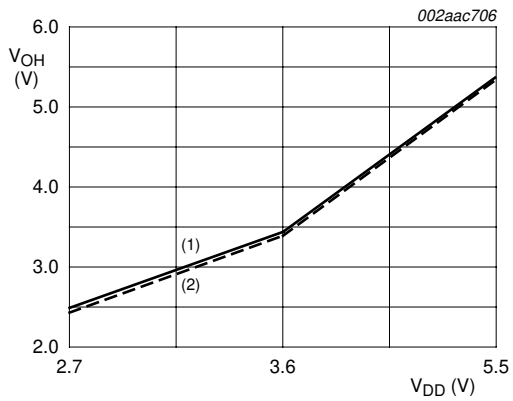
(1) $I_{OH} = -8$ mA

(2) $I_{OH} = -10$ mA

Fig 20. V_{OH} maximum
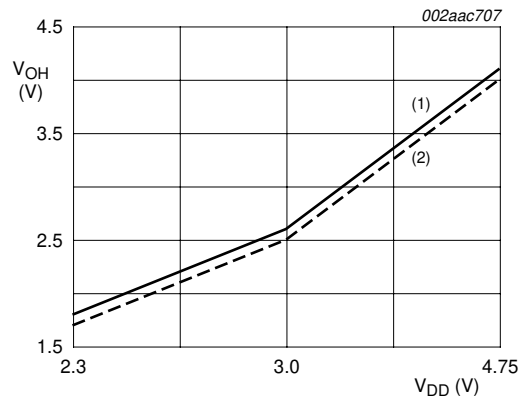
(1) $I_{OH} = -8$ mA

(2) $I_{OH} = -10$ mA

Fig 21. V_{OH} minimum
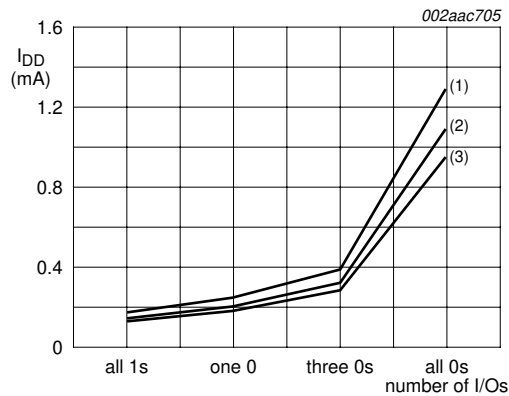
$V_{DD} = 5.5$ V; $V_{I/O} = 5.5$ V; A2, A1, A0 set to logic 0.

(1) $T_{amb} = -40$ °C

(2) $T_{amb} = +25$ °C

(3) $T_{amb} = +85$ °C

Fig 22. I_{DD} versus number of I/Os held LOW

11. Dynamic characteristics

Table 15. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	**Max**	**Min**	**Max**	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$[3]	300	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$[3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{v(Q)}$	data output valid time		-	200	-	200	ns
$t_{su(D)}$	data input set-up time		150	-	150	-	ns
$t_{h(D)}$	data input hold time		1	-	1	-	µs
Interrupt timing							
$t_{v(INT\_N)}$	valid time on pin $\overline{INT}$		-	4	-	4	µs
$t_{rst(INT\_N)}$	reset time on pin $\overline{INT}$		-	4	-	4	µs

[1] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.
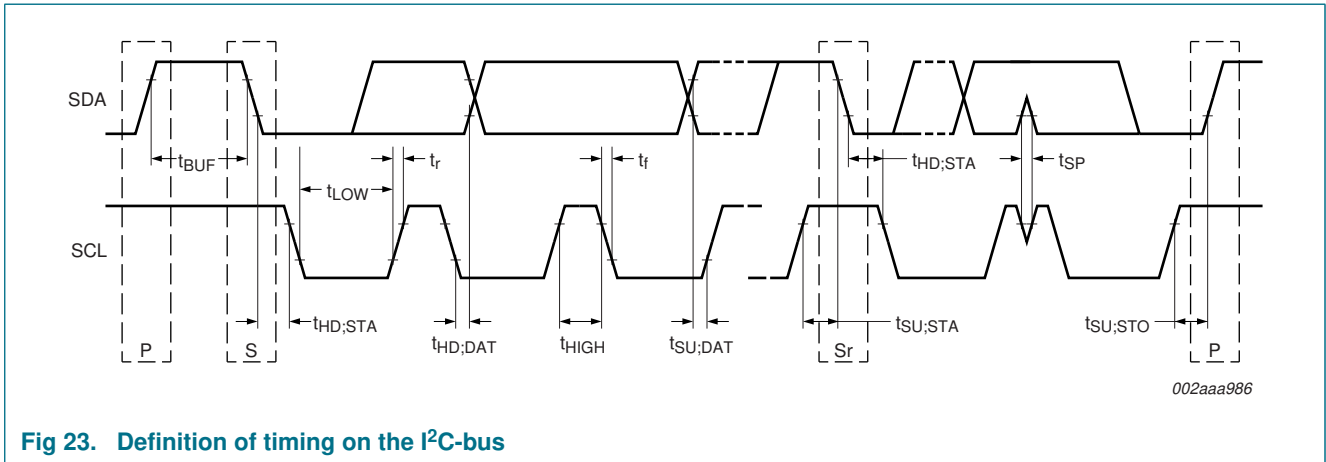
Fig 23. Definition of timing on the I2C-bus

12. Test information

R_L = load resistor.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance of Z_o of the pulse generators.
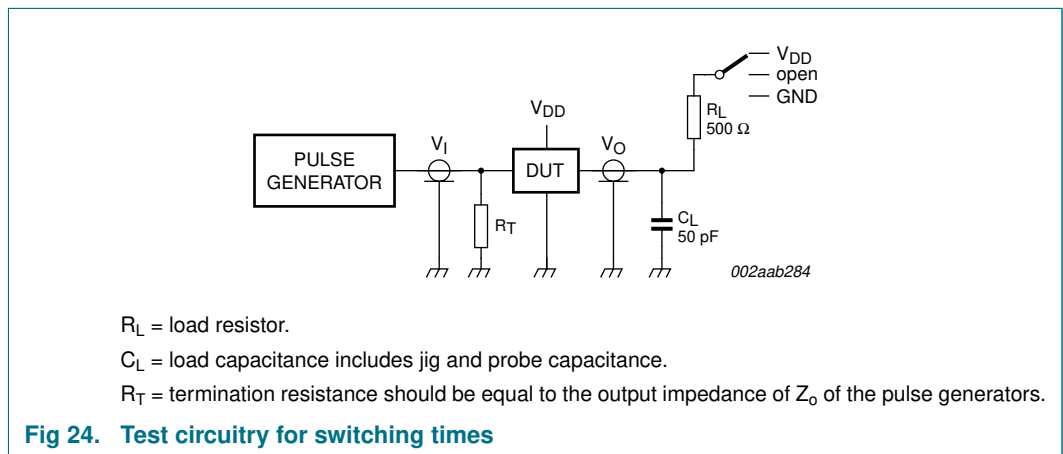
Fig 24. Test circuitry for switching times
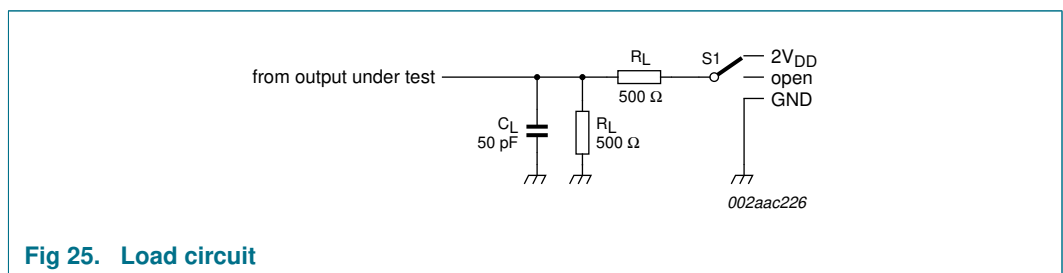
Fig 25. Load circuit

13. Package outline

DIP24: plastic dual in-line package; 24 leads (600 mil)

SOT101-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A1 min.	A2 max.	b	b1	c	D (1)	E (1)	e	e1	L	ME	MH	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.2	0.02	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT101-1	051G02	MO-015	SC-509-24			~~99-12-27~~ 03-02-13

Fig 26. Package outline SOT101-1 (DIP24)

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

0   5   10 mm

scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	Hₑ	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 27. Package outline SOT137-1 (SO24)

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	H_E	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19
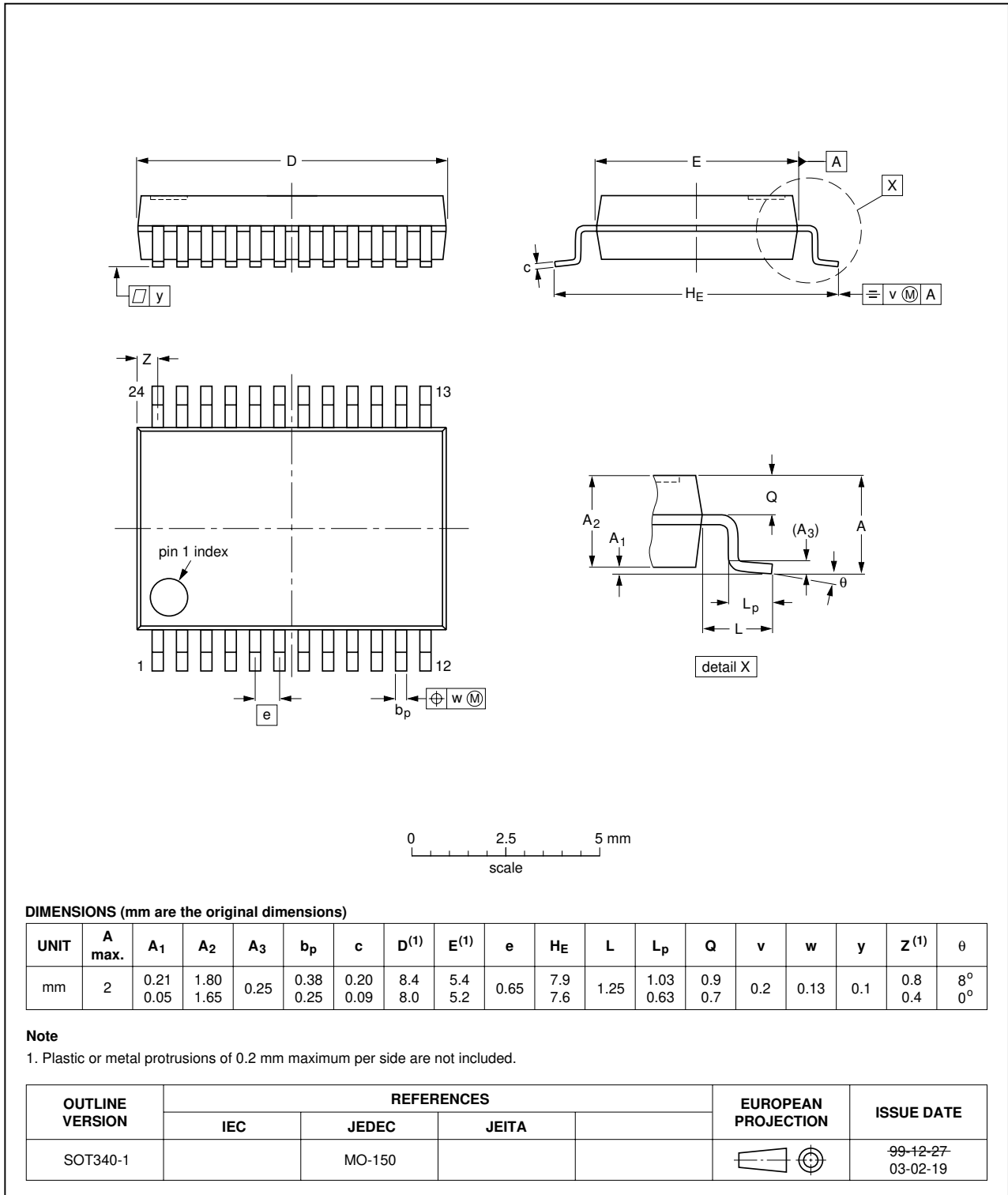
Fig 28. Package outline SOT340-1 (SSOP24)

PCA9555_8

Product data sheet

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm　　　　**SOT355-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bp	c	D(1)	E(2)	e	HE	L	Lp	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

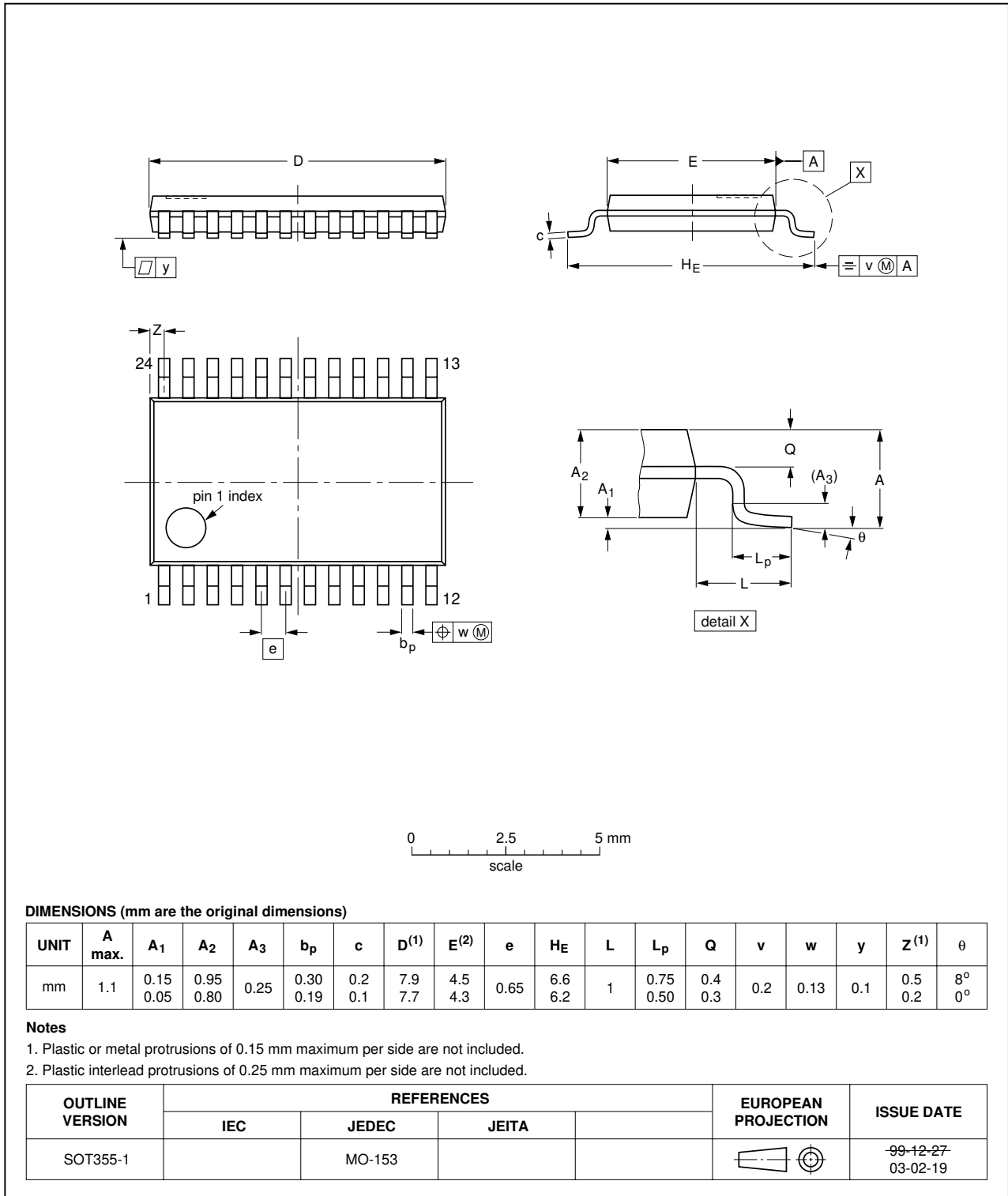| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 29. Package outline SOT355-1 (TSSOP24)