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PCA9574

8-bit I²C-bus and SMBus, level translating, low voltage GPIO with reset and interrupt

Rev. 5 — 25 September 2014 Product data sheet

1. General description

The PCA9574 is a CMOS device that provides 8 bits of General Purpose parallel Input/Output (GPIO) expansion in low voltage processor and handheld battery powered mobile applications and was developed to enhance the NXP family of I²C-bus I/O expanders. The improvements include lower supply current, lower operating voltage of 1.1 V to 3.6 V, dual and separate supply rails to allow voltage level translation anywhere between 1.1 V and 3.6 V, 400 kHz clock frequency, and smaller packaging. Any of the eight I/O ports can be configured as an input or output independent of each other and default on start-up to inputs. I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum; for example in battery powered mobile applications and clamshell devices for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level to I/O devices operating at a different (usually higher) voltage level. PCA9574 has built-in level shifting feature that makes these devices extremely flexible in mixed signal environments where communication between incompatible I/Os is required. The core of PCA9574 can operate at a voltage as low as 1.1 V while the I/O bank can operate in the range 1.1 V to 3.6 V. Bus-hold with programmable on-chip pull-up or pull-down feature for I/Os is also provided.

The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity inversion register (active HIGH or active LOW operation). Either a bus-hold function or pull-up/pull-down feature can be selected by programming corresponding registers. The bus-hold provides a valid logic level when the I/O bus is not actively driven. When bus-hold feature is not selected, the I/O ports can be configured to have pull-up or pull-down by programming the pull-up/pull-down configuration register.

An open-drain interrupt output pin ($\overline{INT}$) allows monitoring of the input pins and is asserted each time a change occurs on an input port unless that port is masked (default = masked). A ‘GPIO All Call’ command allows programming multiple PCA9574s at the same time even if they have different individual I²C-bus addresses. This allows optimal code programming when more than one device needs to be programmed with the same instruction or if all outputs need to be turned on or off at the same time. The internal Power-On Reset (POR) or hardware reset pin ($\overline{RESET}$) initializes the eight I/Os as inputs, sets the registers to their default values and initializes the device state machine. The I/O bank is held in its default state when the logic supply (V_{DD}) is off.

One address select pin allows up to two PCA9574 devices to be connected with two different addresses on the same I²C-bus.

The PCA9574 is available in TSSOP16 and HVQFN16 packages and is specified over the −40 °C to +85 °C industrial temperature range.

2. Features and benefits

- 400 kHz I²C-bus serial interface
- Compliant with I²C-bus Standard-mode (100 kHz)
- Separate supply rails for core logic and I/O bank provides voltage level shifting
- 1.1 V to 3.6 V operation with level shifting feature
- Very low standby current: < 1 μA
- 8 configurable I/O pins that default to inputs at power-up
- Outputs:
  - Totem pole: 1 mA source and 3 mA sink
  - Independently programmable 100 kΩ pull-up or pull-down for each I/O pin
  - Open-drain active LOW interrupt ($\overline{INT}$) output pin allows monitoring of logic level change of pins programmed as inputs
- Inputs:
  - Programmable bus hold provides valid logic level when inputs are not actively driven
  - Programmable Interrupt Mask Control for input pins that do not require an interrupt when their states change or to prevent spurious interrupts default to mask at power-up
  - Polarity inversion register allows inversion of the polarity of the I/O pins when read
- Active LOW reset ($\overline{RESET}$) input pin resets device to power-up default state
- GPIO All Call address allows programming of more than one device at the same time with the same parameters
- 2 programmable slave addresses using 1 address pin
- −40 °C to +85 °C operation
- ESD protection exceeds 7000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP16 and HVQFN16

3. Applications

- Cell phones
- Media players
- Multi voltage environments
- Battery operated mobile gadgets
- Motherboards
- Servers
- RAID systems
- Industrial control
- Medical equipment
- PLCs

- Gaming machines
- Instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

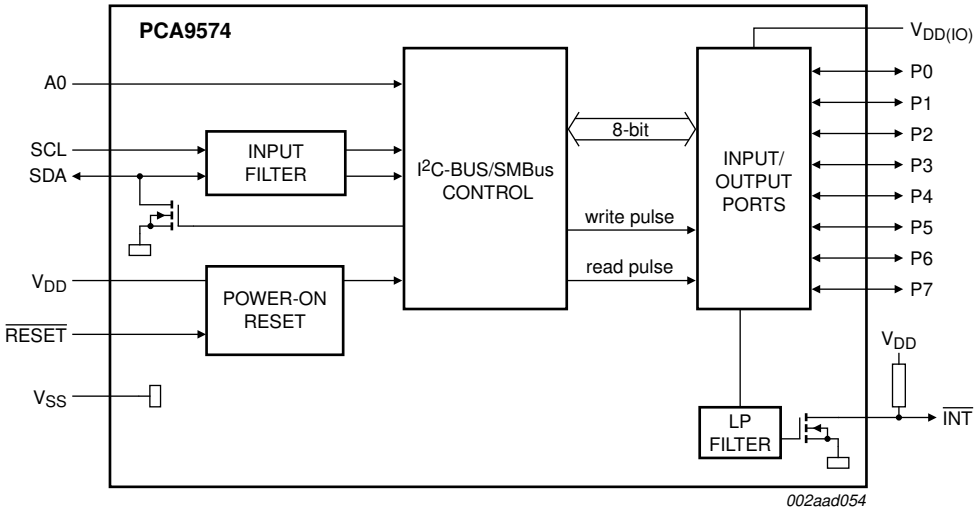
Type number	Topside marking	Package		
		Name	Description	Version
PCA9574PW	PCA9574	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9574BS	P74	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9574PW	PCA9574PW,118	TSSOP16	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9574BS	PCA9574BS,118	HVQFN16	Reel 13” Q1/T1 *standard mark SMD	6000	T_{amb} = −40 °C to +85 °C

5. Block diagram



Remark: All I/Os are set to inputs at power-up and $\overline{\text{RESET}}$.

Fig 1. Block diagram of PCA9574

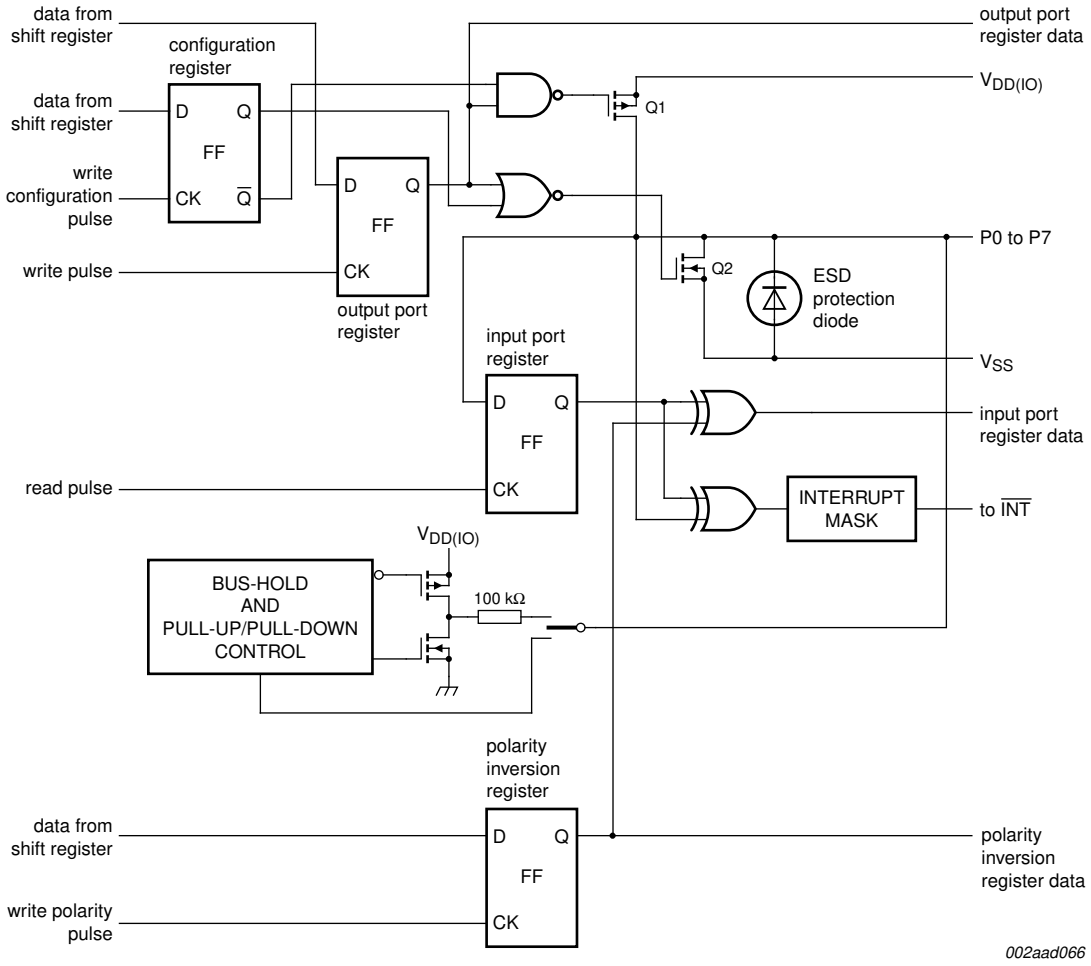


Fig 2. Simplified schematic of the I/Os (P0 to P7)

6. Pinning information

6.1 Pinning

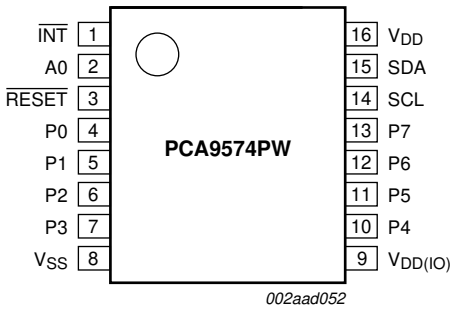


Fig 3. Pin configuration for TSSOP16

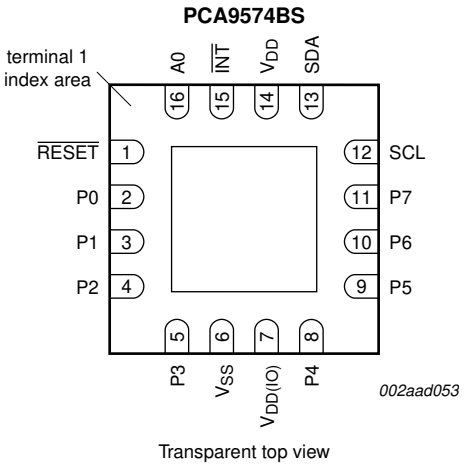


Fig 4. Pin configuration for HVQFN16

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	TSSOP16	HVQFN16		
$\overline{INT}$	1	15	O	active LOW interrupt output; active LOW SMBus alert output
A0	2	16	I	address input
$\overline{RESET}$	3	1	I	active LOW reset input
P0	4	2	I/O	input/output 0
P1	5	3	I/O	input/output 1
P2	6	4	I/O	input/output 2
P3	7	5	I/O	input/output 3
V_{SS}	8	6[1]	ground	supply ground
$V_{DD(IO)}$	9	7	power supply	I/O bank supply voltage
P4	10	8	I/O	input/output 4
P5	11	9	I/O	input/output 5
P6	12	10	I/O	input/output 6
P7	13	11	I/O	input/output 7
SCL	14	12	I	serial clock line
SDA	15	13	I/O	serial data line
V_{DD}	16	14	power supply	supply voltage

[1] HVQFN16 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

7.1 Device address

Following a START condition the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9574 is shown in Figure 5. Slave address pin A0 chooses 1 of 2 slave addresses: 40h or 42h.

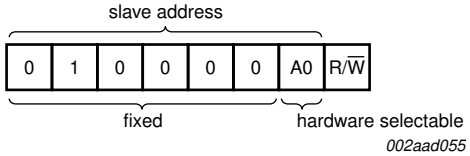
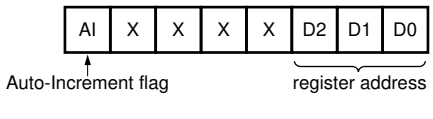


Fig 5. PCA9574 device address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while logic 0 selects a write operation.

7.2 Command register

Following the successful acknowledgement of the slave address + R/$\overline{W}$ bit, the bus master will send a byte to the PCA9574, which will be stored in the Command register.



Reset state = 00h

Remark: The Command register does not apply to Software Reset I²C-bus address.

Fig 6. Command register

The lowest three bits are used as a pointer to determine which register will be accessed. Only a command register code with the three least significant bits equal to the eight allowable values as defined in Table 4 “Register summary” will be acknowledged. Reserved or undefined command codes will not be acknowledged. At power-up, this register defaults to 00h, with the AI bit set to ‘0’, and the lowest 3 bits set to ‘0’.

If the Auto-Increment flag is set (AI = 1), the three least significant bits of the Command register are automatically incremented after a read or write. This allows the user to program and/or read the eight command registers (listed in Table 4) sequentially. It will then roll over to register 00h after the last register is accessed and the selected registers will be overwritten or re-read.

If the Auto-Increment flag is cleared (AI = 0), the three least significant bits are not incremented after data is read or written, only one register will be repeatedly read or written.

7.3 Register definitions

Table 4. Register summary

Register number	D2	D1	D0	Name	Type	Function
00h	0	0	0	IN	read only	Input port register
01h	0	0	1	INVRT	read/write	Polarity inversion register
02h	0	1	0	BKEN	read/write	Bus-hold enable register
03h	0	1	1	PUPD	read/write	Pull-up/pull-down selector register
04h	1	0	0	CFG	read/write	Port configuration register
05h	1	0	1	OUT	read/write	Output port register
06h	1	1	0	MSK	read/write	Interrupt mask register
07h	1	1	1	INTS	read only	Interrupt status register

7.4 Writing to port registers

Data is transmitted to the PCA9574 by sending the device address and setting the least significant bit to logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register will receive the data following the command byte. Each 8-bit register may be updated independently of the other registers.

7.5 Reading the port registers

In order to read data from the PCA9574, the bus master must first send the PCA9574 address with the least significant bit set to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again but this time, the least significant bit is set to logic 1. Data from the register defined by the command byte will then be sent by the PCA9574. Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read using the auto-increment feature.

7.5.1 Register 0 - Input port register

This register is read-only. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. Writes to this register will be acknowledged but will have no effect.

The default 'X' is determined by the externally applied logic level.

Table 5. Register 0 - Input port register (address 00h) bit description

Bit	Symbol	Access	Value	Description
7	I0.7	read only	X	determined by externally applied logic level
6	I0.6	read only	X	
5	I0.5	read only	X	
4	I0.4	read only	X	
3	I0.3	read only	X	
2	I0.2	read only	X	
1	I0.1	read only	X	
0	I0.0	read only	X	

7.5.2 Register 1 - Polarity inversion register

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the corresponding Input port data is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 6. Register 1 - Polarity inversion register (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	N0.7	R/W	0*	inverts polarity of Input port register data 0 = Input port register data retained (default value) 1 = Input port register data inverted
6	N0.6	R/W	0*	
5	N0.5	R/W	0*	
4	N0.4	R/W	0*	
3	N0.3	R/W	0*	
2	N0.2	R/W	0*	
1	N0.1	R/W	0*	
0	N0.0	R/W	0*	

7.5.3 Register 2 - Bus-hold/pull-up/pull-down enable register

Bit 0 of this register allows the user to enable/disable the bus-hold feature for the I/O pins. Setting the bit 0 to logic 1 enables bus-hold feature for the I/O bank. In this mode, the pull-up/pull-downs will be disabled. Setting the bit 0 to logic 0 disables bus-hold feature.

Bit 1 of this register allows the user to enable/disable pull-up/pull-downs on the I/O pins. Setting the bit 1 to logic 1 enables selection of pull-up/pull-down using Register 3. Setting the bit 1 to logic 0 disables pull-up/pull-downs on the I/O pins and contents of Register 3 will have no effect on the I/O.

Table 7. Register 2 - Bus-hold/pull-up/pull-down enable register (address 02h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	E0.7	R/W	X	not used
6	E0.6	R/W	X	
5	E0.5	R/W	X	
4	E0.4	R/W	X	
3	E0.3	R/W	X	
2	E0.2	R/W	X	
1	E0.1	R/W	0*	allows the user to enable/disable pull-up/pull-downs on the I/O pins 0 = disables pull-up/pull-downs on the I/O pins and contents of Register 3 will have no effect on the I/O (default value) 1 = enables selection of pull-up/pull-down using Register 3
0	E0.0	R/W	0*	allows user to enable/disable the bus-hold feature for the I/O pins 0 = disables bus-hold feature (default value) 1 = enables bus-hold feature

7.5.4 Register 3 - Pull-up/pull-down selector register

When bus-hold feature is not selected and bit 1 of Register 2 is set to logic 1, the I/O port can be configured to have pull-up or pull-down by programming the pull-up/pull-down register. Setting a bit to logic 1 will select a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 will select a 100 kΩ pull-down resistor for that I/O pin. If the bus-hold feature is enabled, writing to this register will have no effect on pull-up/pull-down selection.

Table 8. Register 3 - Pull-up/pull-down selector register (address 03h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	P0.7	R/W	1*	configures I/O port pin to have pull-up or pull-down when bus-hold feature not selected and bit 1 of Register 2 is logic 1 0 = selects a 100 kΩ pull-down resistor for that I/O pin 1 = selects a 100 kΩ pull-up resistor for that I/O pin (default value)
6	P0.6	R/W	1*	
5	P0.5	R/W	1*	
4	P0.4	R/W	1*	
3	P0.3	R/W	1*	
2	P0.2	R/W	1*	
1	P0.1	R/W	1*	
0	P0.0	R/W	1*	

7.5.5 Register 4 - Configuration register

This register configures the direction of the I/O pins. If a bit in this register is set (written with logic 1), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with logic 0), the corresponding port pin is enabled as an output. At reset, the device's ports are inputs.

Table 9. Register 4 - Configuration register (address 04h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	C0.7	R/W	1*	configures the direction of the I/O pins 0 = corresponding port pin enabled as an output 1 = corresponding port pin configured as input (default value)
6	C0.6	R/W	1*	
5	C0.5	R/W	1*	
4	C0.4	R/W	1*	
3	C0.3	R/W	1*	
2	C0.2	R/W	1*	
1	C0.1	R/W	1*	
0	C0.0	R/W	1*	

7.5.6 Register 5 - Output port register

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Register 4. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 10. Register 5 - Output port register (address 05h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	O0.7	R/W	0*	reflects outgoing logic levels of pins defined as outputs by Register 4
6	O0.6	R/W	0*	
5	O0.5	R/W	0*	
4	O0.4	R/W	0*	
3	O0.3	R/W	0*	
2	O0.2	R/W	0*	
1	O0.1	R/W	0*	
0	O0.0	R/W	0*	

7.5.7 Register 6 - Interrupt mask register

All the bits of Interrupt mask register are set to logic 1 upon power-on or software reset, thus disabling interrupts. Interrupts may be enabled by setting corresponding mask bits to logic 0.

Table 11. Register 6 - Interrupt mask register (address 06h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	M0.7	R/W	1*	enable or disable interrupts 0 = enable interrupt 1 = disable interrupt (default value)
6	M0.6	R/W	1*	
5	M0.5	R/W	1*	
4	M0.4	R/W	1*	
3	M0.3	R/W	1*	
2	M0.2	R/W	1*	
1	M0.1	R/W	1*	
0	M0.0	R/W	1*	

7.5.8 Register 7 - Interrupt status register

This register is read-only. It is used to identify the source of interrupt.

Remark: If the interrupts are masked, this register will return all zeros.

Table 12. Register 7 - Interrupt status register (address 07h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	S0.7	read only	0*	identifies source of interrupt
6	S0.6	read only	0*	
5	S0.5	read only	0*	
4	S0.4	read only	0*	
3	S0.3	read only	0*	
2	S0.2	read only	0*	
1	S0.1	read only	0*	
0	S0.0	read only	0*	

7.6 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9574 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9574 registers and state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

7.7 $\overline{\text{RESET}}$ input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA9574 registers and I²C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

7.8 Software reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address ‘0000 000’ with the R/$\overline{\text{W}}$ bit set to 0 (write) is sent by the I²C-bus master.
3. The PCA9574 device(s) acknowledge(s) after seeing the General Call address ‘0000 0000’ (00h) only. If the R/$\overline{\text{W}}$ bit is set to logic 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.The PCA9574 acknowledges this value only. If the byte is not equal to 06h, the PCA9574 does not acknowledge it. If more than 1 byte of data is sent, the PCA9574 does not acknowledge anymore.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the PCA9574 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed. The I²C-bus master must interpret a non-acknowledge from the PCA9574 (at any time) as a 'Software Reset Abort'. The PCA9574 does not initiate a software reset.

7.9 Interrupt output ($\overline{INT}$)

The open-drain active LOW interrupt is activated when one of the port pins changes state and the port pin is configured as an input and the interrupt on it is not masked. The interrupt is deactivated when the port pin input returns to its previous state or the Input Port register is read. It is highly recommended to program the MSK register, and the CFG registers during the initialization sequence after power-up, since any change to them during Normal mode operation may cause undesirable interrupt events to happen.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input port register. Only a read of the Input port register that contains the bit(s) image of the input(s) that generated the interrupt clears the interrupt condition.

7.10 Standby

The PCA9574 goes into standby when the I²C-bus is idle. Standby supply current is lower than 1.0 μA (typical).

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

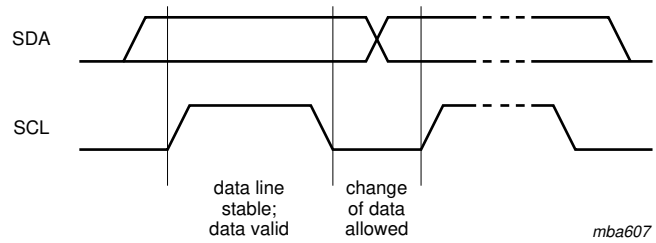


Fig 7. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 8).

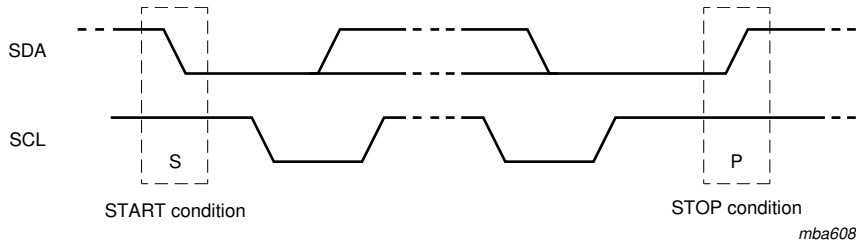


Fig 8. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 9).

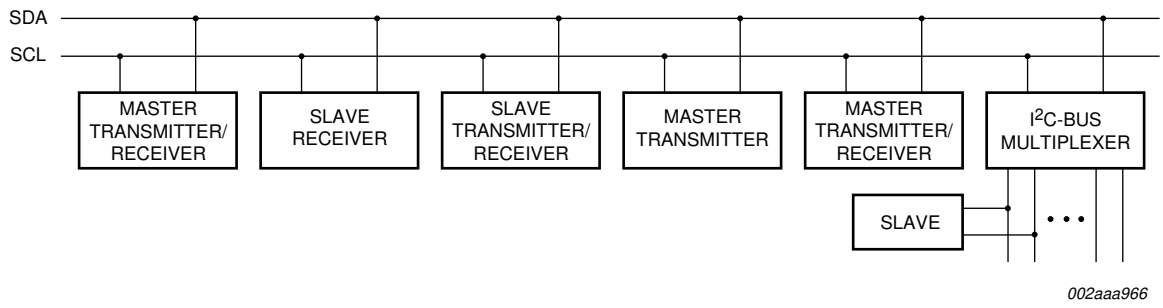


Fig 9. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

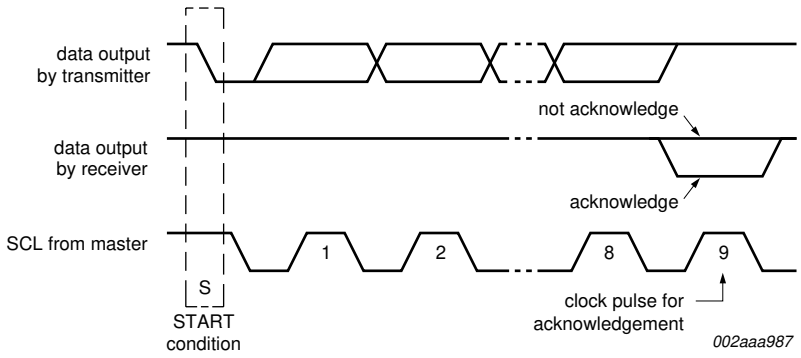


Fig 10. Acknowledgement on the I²C-bus

9. Bus transactions

Data is transmitted to the PCA9574 registers using 'Write Byte' transfers (see Figure 11 and Figure 12).

Data is read from the PCA9574 registers using 'Read Byte' transfers (see Figure 13 and Figure 14).

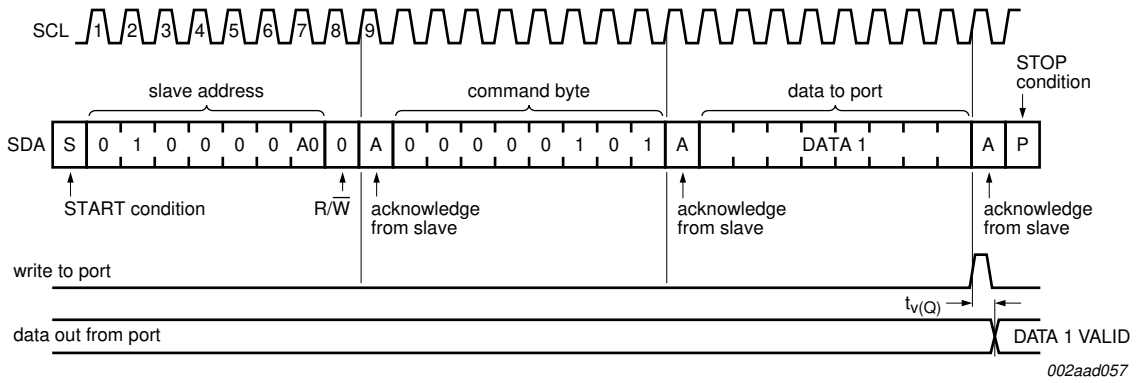


Fig 11. Write to Output port register

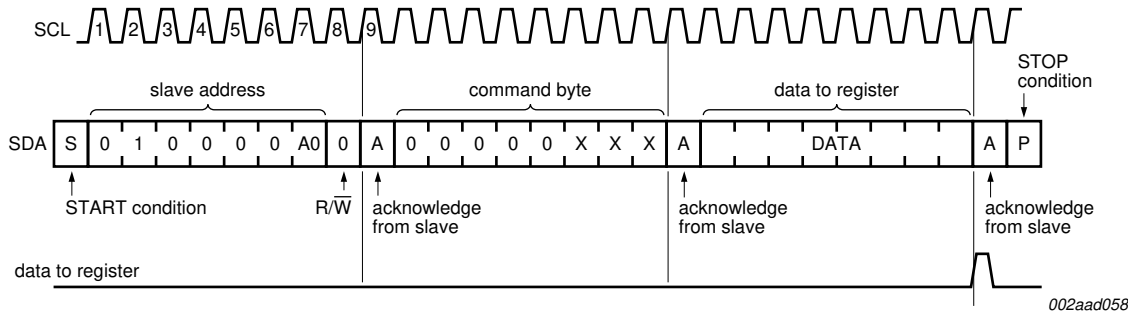


Fig 12. Write to Polarity inversion, Bus-hold enable, Pull-up/pull-down selector, Configuration, Interrupt mask and Interrupt status registers

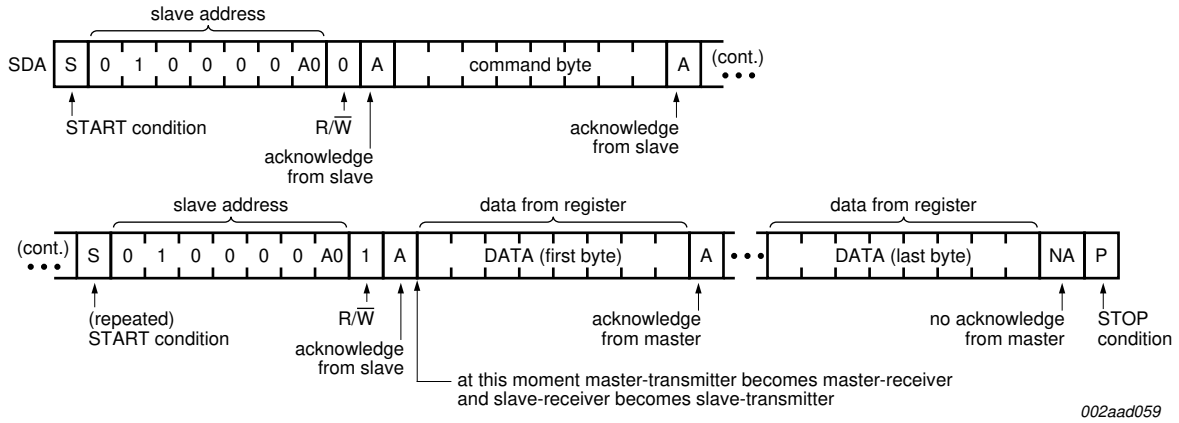
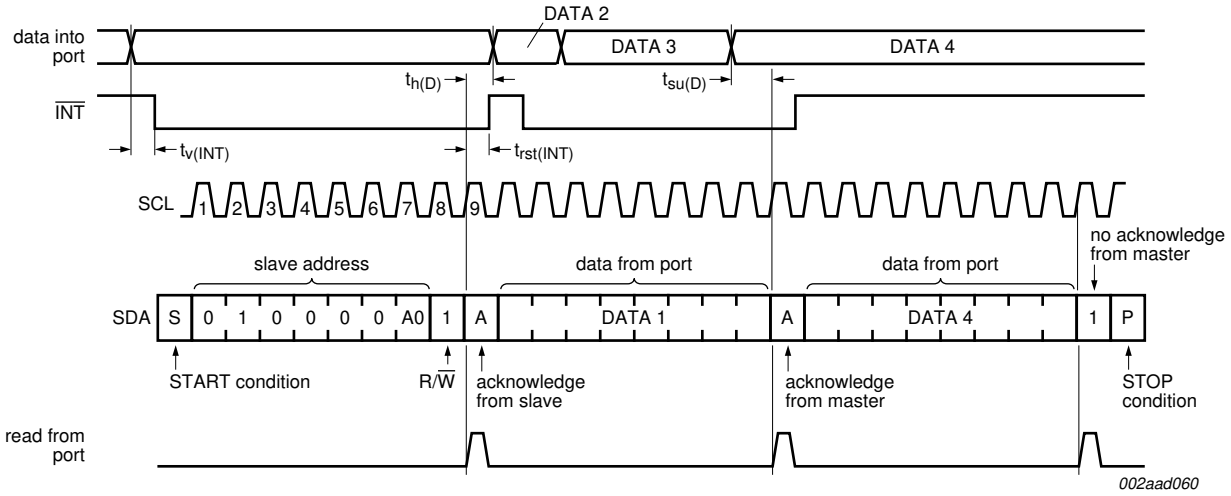


Fig 13. Read from register

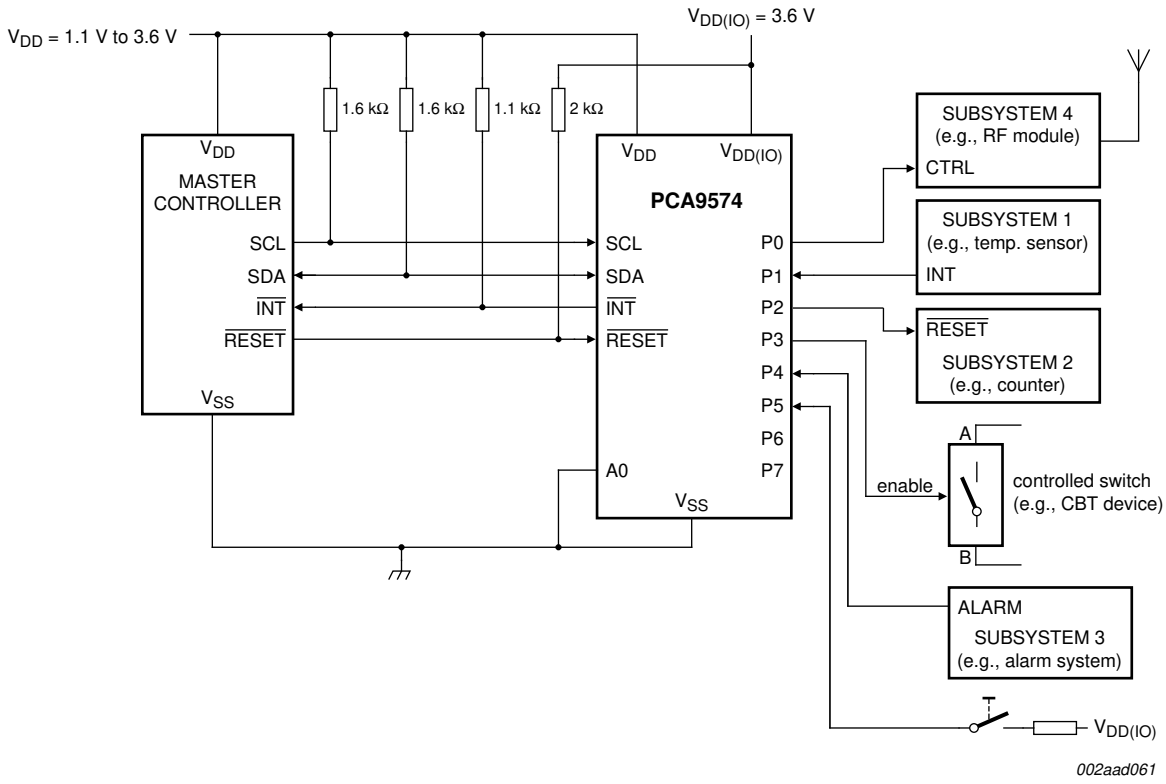


This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition.

Fig 14. Read Input port register

10. Application design-in information



Device address configured as 0100 0000b for this example.

P0, P2, P3 configured as outputs.

P1, P4, P5 configured as inputs.

P6, P7 are not used and must be configured as outputs.

Fig 15. Typical application

11. Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+4.0	V
$V_{DD(IO)}$	input/output supply voltage			V_{SS} − 0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current			-	±5	mA
I_I	input current			-	±20	mA
I_{DD}	supply current			-	90	mA
I_{SS}	ground supply current			-	90	mA
P_{tot}	total power dissipation			-	75	mW
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C

12. Static characteristics

Table 14. Static characteristics

V_{DD} = 1.1 V to 3.6 V; $V_{DD(IO)}$ = 1.1 V to 3.6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.1	-	3.6	V
$V_{DD(IO)}$	input/output supply voltage			1.1	-	V_{DD} + 0.5	V
I_{DD}	supply current	operating mode; V_{DD} = 3.6 V; no load; f_{SCL} = 100 kHz; I/O = inputs		-	135	200	µA
I_{stbL}	LOW-level standby current	Standby mode; V_{DD} = 3.6 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
I_{stbH}	HIGH-level standby current	Standby mode; V_{DD} = 3.6 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS} (rising V_{DD})		-	0.8	1.0	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	3.6	V
I_{OL}	LOW-level output current	V_{OL} = 0.2 V; V_{DD} = 1.1 V		1	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 2.3 V		3	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7$V_{DD(IO)}$	-	3.6	V
I_{OH}	HIGH-level output current	V_{OH} = 0.9 V; $V_{DD(IO)}$ = 1.1 V		1	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.2 V; $V_{DD(IO)}$ = 1.1 V		1	-	-	mA
		V_{OL} = 0.5 V; $V_{DD(IO)}$ = 3.6 V		2	3	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −1 mA; $V_{DD(IO)}$ = 1.1 V		0.8	-	-	V
I_{LIH}	HIGH-level input leakage current	$V_{DD(IO)}$ = 3.6 V; V_I = $V_{DD(IO)}$		-	-	1	µA
I_{LIL}	LOW-level input leakage current	$V_{DD(IO)}$ = 3.6 V; V_I = V_{SS}		-	-	−1	µA
C_i	input capacitance			-	3.7	5	pF
C_o	output capacitance			-	3.7	5	pF
Interrupt $\overline{INT}$							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 1.1 V		3	-	-	mA
Select input A0; $\overline{RESET}$							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	3.6	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA

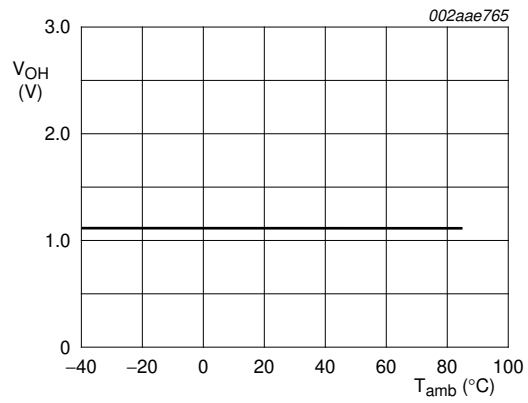


Fig 16. V_{OH} at V_{DD} = 3.3 V, $V_{DD(IO)}$ = 1.2 V, I_{OH} = −1 mA

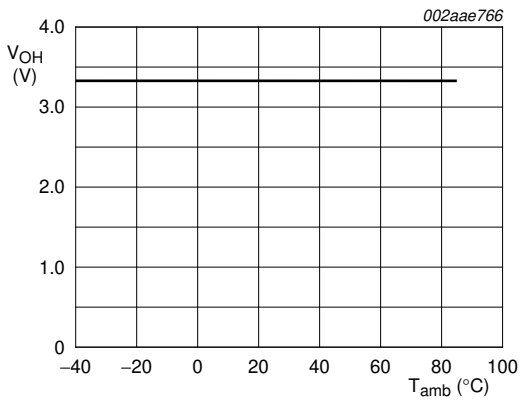


Fig 17. V_{OH} at V_{DD} = 3.3 V, $V_{DD(IO)}$ = 3.3 V, I_{OH} = −1 mA

13. Dynamic characteristics

Table 15. Dynamic characteristics

V_{DD} = 1.1 V to 3.6 V; $V_{DD(IO)}$ = 1.1 V to 3.6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{VD;ACK}$	data valid acknowledge time		[1]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;DAT}$	data valid time		[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$ [3]	300	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$ [3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
Port timing								
$t_{v(Q)}$	data output valid time			-	200	-	200	ns
$t_{su(D)}$	data input set-up time			150	-	150	-	ns
$t_{h(D)}$	data input hold time			1	-	1	-	µs
Interrupt timing								
$t_{v(INT)}$	valid time on pin $\overline{INT}$			-	4	-	4	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$			-	4	-	4	µs
Reset								
$t_{w(rst)}$	reset pulse width			6	-	6	-	ns
$t_{rec(rst)}$	reset recovery time			0	-	0	-	ns
$t_{rst(SDA)}$	SDA reset time	Figure 19		-	450	-	450	ns
$t_{rst(GPIO)}$	GPIO reset time	Figure 19		-	450	-	450	ns

[1] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

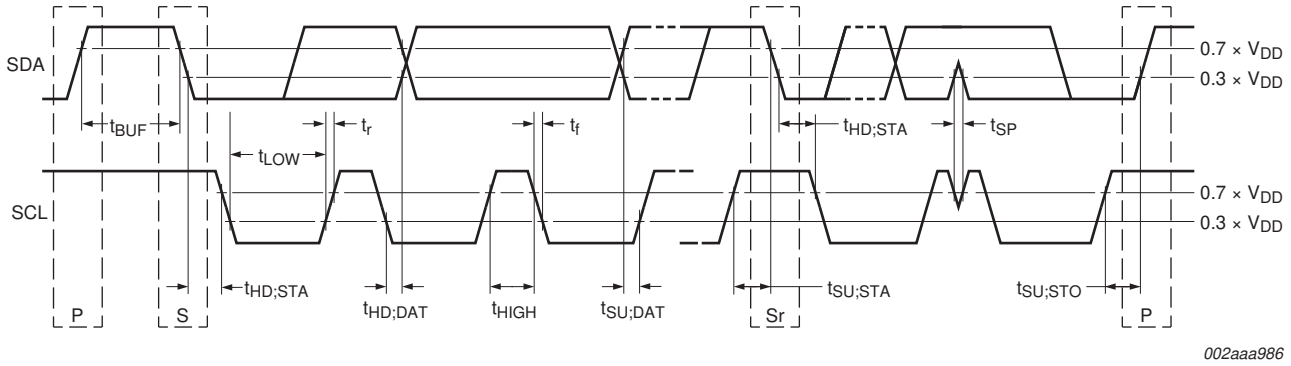


Fig 18. Definition of timing

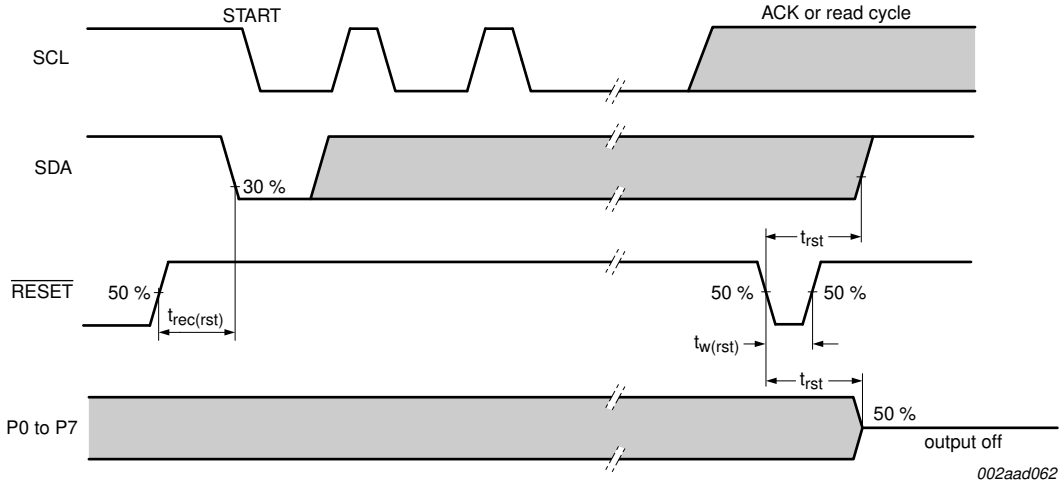
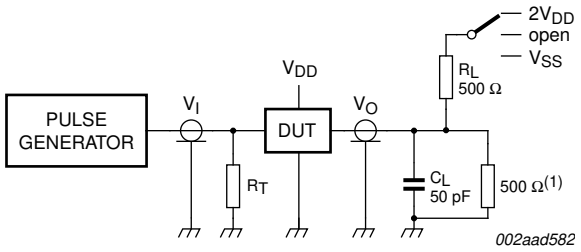


Fig 19. Reset timing

14. Test information



R_L = load resistance.

C_L = load capacitance includes jig and probe capacitance.

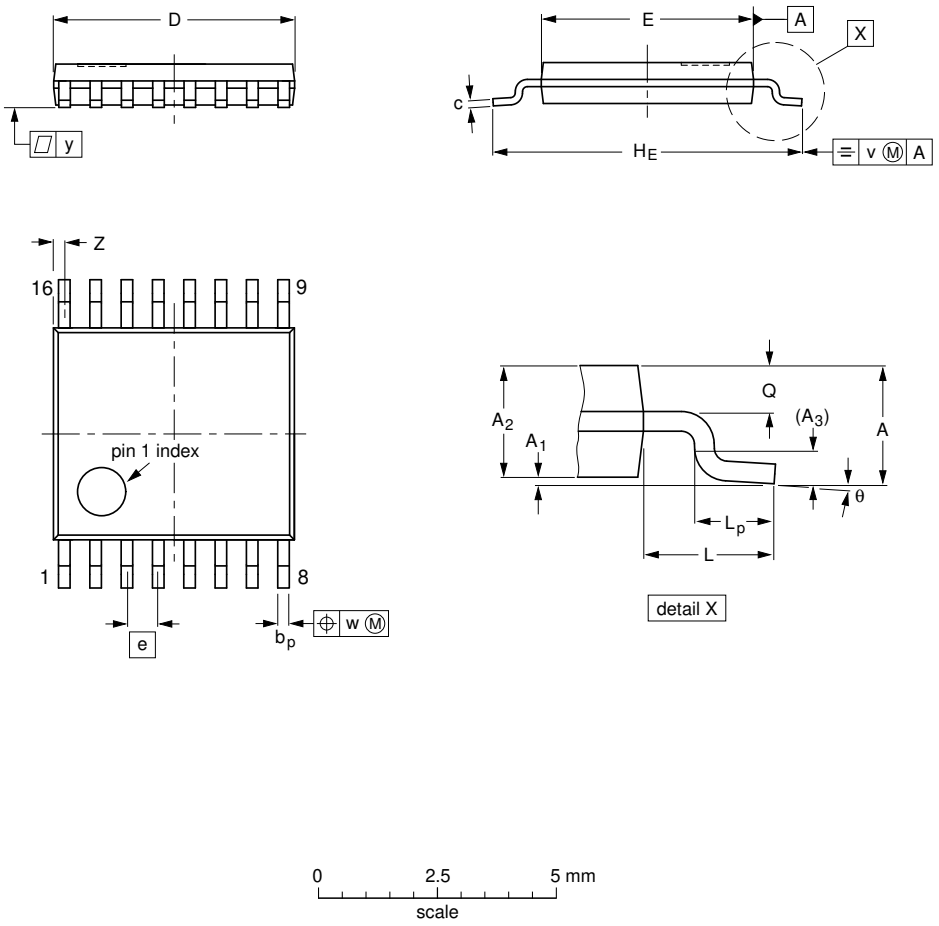
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generators.

(1) For SDA, no 500 Ω pull-down.

Fig 20. Test circuitry for switching times

15. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

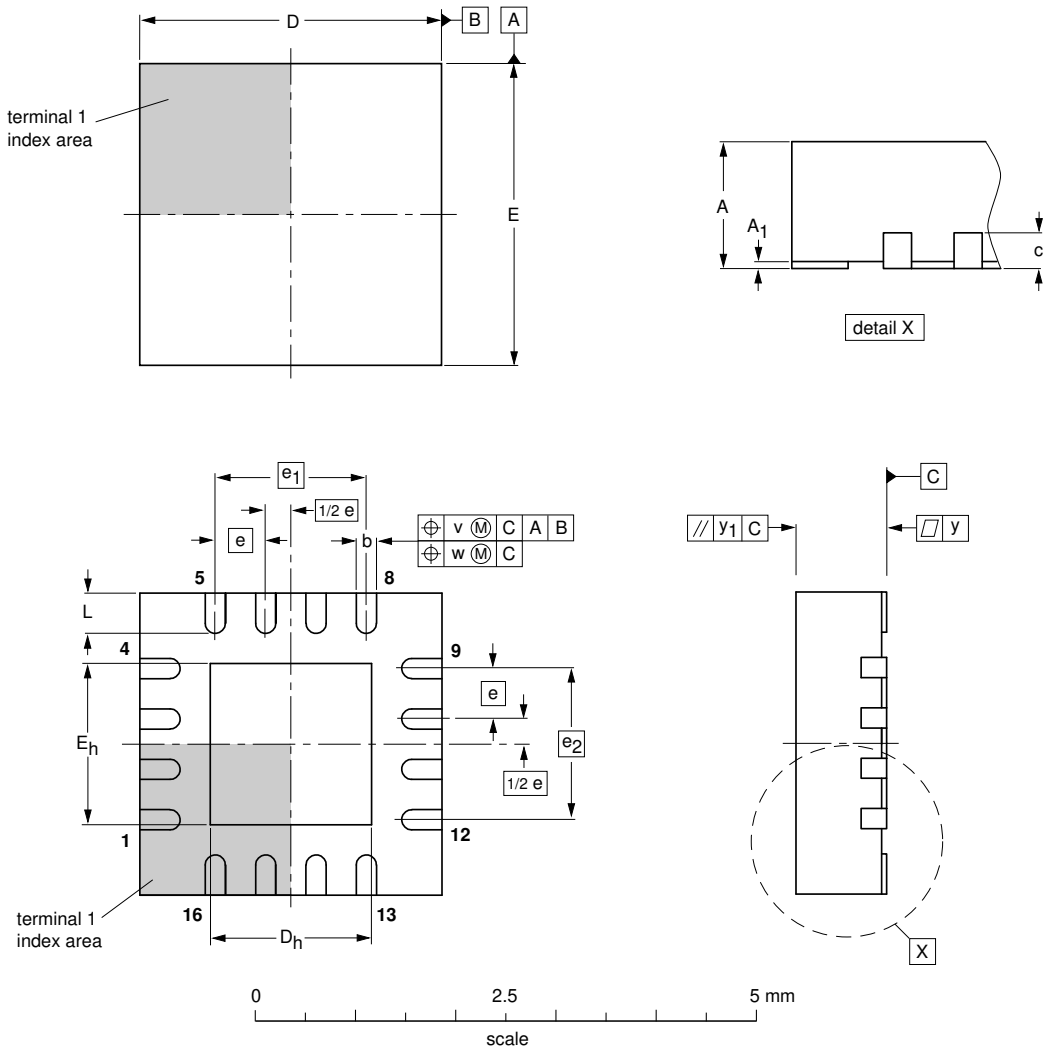
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 21. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Fig 22. Package outline SOT758-1 (HVQFN16)