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PCA9600

Dual bidirectional bus buffer

Rev. 6 — 25 September 2015 Product data sheet

1. General description

The PCA9600 is designed to isolate I²C-bus capacitance, allowing long buses to be driven in point-to-point or multipoint applications of up to 4000 pF. The PCA9600 is a higher-speed version of the P82B96. It creates a non-latching, bidirectional, logic interface between a normal I²C-bus and a range of other higher capacitance or different voltage bus configurations. It can operate at speeds up to at least 1 MHz, and the high drive side is compatible with the Fast-mode Plus (Fm+) specifications.

The PCA9600 features temperature-stabilized logic voltage levels at its SX/SY interface making it suitable for interfacing with buses that have non I²C-bus-compliant logic levels such as SMBus, PMBus, or with microprocessors that use those same TTL logic levels.

The separation of the bidirectional I²C-bus signals into unidirectional TX and RX signals enables the SDA and SCL signals to be transmitted via balanced transmission lines (twisted pairs), or with galvanic isolation using opto or magnetic coupling. The TX and RX signals may be connected together to provide a normal bidirectional signal.

2. Features and benefits

- Bidirectional data transfer of I²C-bus signals
- Isolates capacitance allowing 400 pF on SX/SY side and 4000 pF on TX/TY side
- TX/TY outputs have 60 mA sink capability for driving low-impedance or high-capacitive buses
- 1 MHz operation on up to 20 meters of wire (see *AN10658*)
- Supply voltage range of 2.5 V to 15 V with I²C-bus logic levels on SX/SY side independent of supply voltage
- Splits I²C-bus signal into pairs of forward/reverse TX/RX, TY/RY signals for interface with opto-electrical isolators and similar devices that need unidirectional input and output signal paths
- Low power supply current
- ESD protection exceeds 3500 V HBM per JESD22-A114 and 1400 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8 and TSSOP8 (MSOP8)

3. Applications

- Interface between I^2C-buses operating at different logic levels (for example, 5 V and 3 V or 15 V)
- Interface between I^2C-bus and SMBus (350 μA) standard or Fm+ standard
- Simple conversion of I^2C-bus SDA or SCL signals to multi-drop differential bus hardware, for example, via compatible PCA82C250
- Interfaces with opto-couplers to provide opto-isolation between I^2C-bus nodes up to 1 MHz
- Long distance point-to-point or multipoint architectures

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9600D	PCA9600	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9600DP	9600	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9600D	PCA9600D,118	SO8	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9600DP	PCA9600DP,118	TSSOP8	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = −40 °C to +85 °C

5. Block diagram

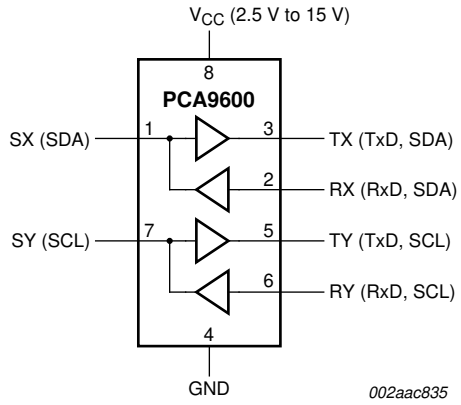


Fig 1. Block diagram of PCA9600

6. Pinning information

6.1 Pinning

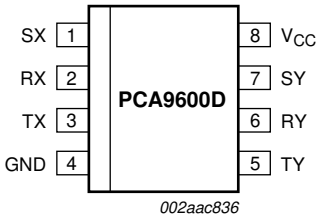


Fig 2. Pin configuration for SO8

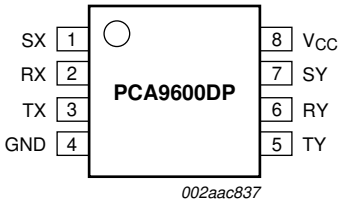


Fig 3. Pin configuration for TSSOP8 (MSOP8)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SX	1	I^2C-bus (SDA or SCL)
RX	2	receive signal
TX	3	transmit signal
GND	4	negative supply voltage
TY	5	transmit signal
RY	6	receive signal
SY	7	I^2C-bus (SDA or SCL)
V_{CC}	8	positive supply voltage

7. Functional description

Refer to Figure 1 “Block diagram of PCA9600”.

The PCA9600 has two identical buffers allowing buffering of SDA and SCL I^2C-bus signals. Each buffer is made up of two logic signal paths, a forward path from the I^2C-bus interface, pins SX and SY which drive the buffered bus, and a reverse signal path from the buffered bus input, pins RX and RY to drive the I^2C-bus interface. These paths:

- sense the voltage state of I^2C-bus pins SX (and SY) and transmit this state to pin TX (and TY respectively), and
- sense the state of pins RX and RY and pull the I^2C-bus pin LOW whenever pin RX or pin RY is LOW.

The rest of this discussion will address only the ‘X’ side of the buffer; the ‘Y’ side is identical.

The I^2C-bus pin SX is specified to allow interfacing with Fast-mode, Fm+ and TTL-based systems.

The logic threshold voltage levels at SX on this I^2C-bus are independent of the IC supply voltage V_{CC}. The maximum I^2C-bus supply voltage is 15 V.

When interfacing with Fast-mode systems, the SX pin is guaranteed to sink the normal 3 mA with a V_{OL} of 0.74 V maximum. That guarantees compliance with the Fast-mode I^2C-bus specification for all I^2C-bus voltages greater than 3 V, as well as compliance with SMBus or other systems that use TTL switching levels.

SX is guaranteed to sink an external 3 mA in addition to its internally sourced pull-up of typically 300 μA (maximum 1 mA at −40 °C). When selecting the pull-up for the bus at SX, the sink capability of other connected drivers should be taken into account. Most TTL devices are specified to sink at least 4 mA so then the pull-up is limited to 3 mA by the requirement to ensure the 0.8 V TTL LOW.

For Fast-mode I^2C-bus operation, the other connected I^2C-bus parts may have the minimum sink capability of 3 mA. SX sources typically 300 μA (maximum 1 mA at −40 °C), which forms part of the external driver loading. When selecting the pull-up it is necessary to subtract the SX pin pull-up current, so, worst-case at −40 °C, the allowed pull-up can be limited (by external drivers) to 2 mA.

When the interface at SX is an Fm+ bus with a voltage greater than 4 V, its higher specified sink capability may be used. PCA9600 has a guaranteed sink capability of 7 mA at V_{OL} = 1 V maximum. That 1 V complies with the bus LOW requirement ($0.25V_{bus}$) of any Fm+ bus operating at 4 V or greater. Since the other connected Fm+ devices have a drive capability greater than 20 mA, the pull-up may be selected for 7 mA sink current at V_{OL} = 1 V. For a nominal 5 V bus (5.5 V maximum) the allowed pull-up is (5.5 V − 1 V) / 7 mA = 643 Ω. With 680 Ω pull-up, the Fm+ rise time of 120 ns maximum can be met with total bus loading up to 200 pF.

The logic level on RX is determined from the power supply voltage V_{CC} of the chip. Logic LOW is below 40 % of V_{CC}, and logic HIGH is above 55 % of V_{CC} (with a typical switching threshold just slightly below half V_{CC}).

TX is an open-collector output without ESD protection diodes to V_{CC}. It may be connected via a pull-up resistor to a supply voltage in excess of V_{CC}, as long as the 15 V rating is not exceeded. It has a larger current sinking capability than a normal I^2C-bus device, being able to sink a static current of greater than 30 mA, and typical 100 mA dynamic pull-down capability as well.

A logic LOW is transmitted to TX when the voltage at I^2C-bus pin SX is below 0.425 V. A logic LOW at RX will cause I^2C-bus pin SX to be pulled to a logic LOW level in accordance with I^2C-bus requirements (maximum 1.5 V in 5 V applications) but not low enough to be looped back to the TX output and cause the buffer to latch LOW.

The LOW level this chip can achieve on the I^2C-bus by a LOW at RX is typically 0.64 V when sinking 1 mA.

If the supply voltage V_{CC} fails, then neither the I^2C-bus nor the TX output will be held LOW. Their open-collector configuration allows them to be pulled up to the rated maximum of 15 V even without V_{CC} present. The input configuration on SX and RX also presents no loading of external signals when V_{CC} is not present.

The effective input capacitance of any signal pin, measured by its effect on bus rise times, is less than 10 pF for all bus voltages and supply voltages including V_{CC} = 0 V.

Remark: Two or more SX or SY I/Os must not be interconnected. The PCA9600 design does not support this configuration. Bidirectional I^2C-bus signals do not allow any direction control pin so, instead, slightly different logic LOW voltage levels are used at SX/SY to avoid latching of this buffer. A 'regular I^2C-bus LOW' applied at the RX/RY of a PCA9600 will be propagated to SX/SY as a 'buffered LOW' with a slightly higher voltage level. If this special 'buffered LOW' is applied to the SX/SY of another PCA9600, that second PCA9600 will not recognize it as a 'regular I^2C-bus LOW' and will not propagate it to its TX/TY output. The SX/SY side of PCA9600 may not be connected to similar buffers that rely on special logic thresholds for their operation, for example P82B96, PCA9511A, PCA9515A, 'B' side of PCA9517, etc. The SX/SY side is only intended for, and compatible with, the normal I^2C-bus logic voltage levels of I^2C-bus master and slave chips, or even TX/RX signals of a second PCA9600 or P82B96 if required. The TX/RX and TY/RY I/O pins use the standard I^2C-bus logic voltage levels of all I^2C-bus parts. There are **no** restrictions on the interconnection of the TX/RX and TY/RY I/O pins to other PCA9600s, for example in a star or multipoint configuration with the TX/RX and TY/RY I/O pins on the common bus and the SX/SY side connected to the line card slave devices. For more details see *Application Note AN10658, "Sending I^2C-bus signals via long communication cables"*.

The PCA9600 is a direct upgrade of the P82B96 with the significant differences summarized in Table 4.

Table 4. PCA9600 versus P82B96

Detail	PCA9600	P82B96
Supply voltage (V_{CC}) range:	2.5 V to 15 V	2 V to 15 V
Maximum operating bus voltage (independent of V_{CC}):	15 V	15 V
Typical operating supply current:	5 mA	1 mA
Typical LOW-level input voltage on I^2C-bus (SX/SY side):	0.5 V over −40 °C to +85 °C	0.65 V at 25 °C

Table 4. PCA9600 versus P82B96 *…continued*

Detail	PCA9600	P82B96
LOW-level output voltage on I^2C-bus (SX/SY side; 3 mA sink):	0.74 V (max.) over −40 °C to +85 °C	0.88 V (typ.) at 25 °C
LOW-level output voltage on Fm+ I^2C-bus (SX/SY side; 7 mA sink):	1 V (max.)	n/a
Temperature coefficient of V_{IL} / V_{OL}:	0 mV/°C	−2 mV/°C
Logic voltage levels on SX/SY bus (independent of V_{CC}):	compatible with I^2C-bus and similar buses using TTL levels (SMBus, etc.)	compatible with I^2C-bus and similar buses using TTL levels (SMBus, etc.)
Typical propagation delays:	< 100 ns	< 200 ns
TX/RX switching specifications (I^2C-bus compliant):	yes, all classes including 1 MHz Fm+	yes, all classes including Fm+
RX logic levels with tighter control than I^2C-bus limit of 30 % to 70 %:	yes, 40 % to 55 % (48 % nominal)	yes, 42 % to 58 % (50 % nominal)
Maximum bus speed:	> 1 MHz	> 400 kHz
ESD rating HBM per JESD22-A114:	> 3500 V	> 3500 V
Package:	SO8, TSSOP8 (MSOP8)	SO8, TSSOP8 (MSOP8)

When the device driving the PCA9600 is an I^2C-bus compatible device, then the PCA9600 is an improvement on the P82B96 as shown in Table 4. There will always be exceptions however, and if the device driving the bus buffer is not I^2C-bus compatible (e.g., you need to use the micro already in the system and bit-bang using two GPIO pins) then here are some considerations that would point to using the P82B96 instead:

- When the pull-up must be the weakest one possible. The spec is 200 μA for P82B96, but it typically works even below that. And if designing for a temperature range −40 °C up to +60 °C, then the driver when sinking 200 μA only needs to drive a guaranteed low of 0.55 V. For the PCA9600, over that same temperature range and when sinking 1.3 mA (at −40 °C), the device driving the bus buffer must provide the required low of 0.425 V.
- When the lower operating temperature range is restricted (say 0 °C). The P82B96 larger SX voltage levels then make a better **typical** match with the driver, even when the supply is as low as 3.3 V.

  For an I^2C-bus compliant driver on 3.3 V the P82B96 is required to guarantee a bus low that is below 0.83 V. P82B96 guarantees that with a 200 μA pull-up.
- When the operating temperature range is restricted at both limits. An I^2C driver's typical output is well below 0.4 V and the P82B96 typically requires 0.6 V input even at +60 °C, so there is a reasonable margin. The PCA9600 requires a typical input low of 0.5 V so its typical margin is smaller. At 0 °C the driver requires a typical input low of 1.16 V and P82B96 provides 0.75 V, so again the typical margin is already quite big and even though PCA9600 is better, providing 0.7 V, that difference is not big.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages with respect to pin GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage	V_{CC} to GND		−0.3	+18	V
$V_{I2C\text{-}bus}$	I^2C-bus voltage	SX and SY; I^2C-bus SDA or SCL		−0.3	+18	V
V_O	output voltage	TX and TY; buffered output	[1]	−0.3	+18	V
V_I	input voltage	RX and RY; receive input	[1]	−0.3	+18	V
$I_{I2C\text{-}bus}$	I^2C-bus current	SX and SY; I^2C-bus SDA or SCL		-	250	mA
P_{tot}	total power dissipation			-	300	mW
T_j	junction temperature	operating range		−40	+125	°C
T_{stg}	storage temperature			−55	+125	°C
T_{amb}	ambient temperature	operating		−40	+85	°C

[1] See also Section 10.2 “Negative undershoot below absolute minimum value”.

9. Characteristics

Table 6. Characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; voltages are specified with respect to GND with V_{CC} = 2.5 V to 15 V unless otherwise specified. Typical values are measured at V_{CC} = 5 V and T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
V_{CC}	supply voltage	operating		2.5	-	15	V
I_{CC}	supply current	V_{CC} = 5 V; buses HIGH		-	5.2	6.75	mA
		V_{CC} = 15 V; buses HIGH		-	5.5	7.3	mA
ΔI_{CC}	additional supply current	per TX/TY output driven LOW; V_{CC} = 5.5 V		-	1.4	3.0	mA
Bus pull-up (load) voltages and currents							
Pins SX and SY; I^2C-bus							
V_I	input voltage	open-collector; RX and RY HIGH		-	-	15	V
V_O	output voltage	open-collector; RX and RY HIGH		-	-	15	V
I_O	output current	static; $V_{SX} = V_{SY}$ = 0.4 V	[1]	0.3	-	2	mA
$I_{O(sink)}$	output sink current	dynamic; $V_{SX} = V_{SY}$ = 1 V; RX and RY LOW		7	15	-	mA
I_L	leakage current	$V_{SX} = V_{SY}$ = 15 V; RX and RY HIGH		-	-	10	µA
Pins TX and TY							
V_O	output voltage	open-collector		-	-	15	V
I_{load}	load current	maximum recommended on buffered bus; $V_{TX} = V_{TY}$ = 0.4 V; SX and SY LOW on I^2C-bus = 0.4 V		-	-	30	mA
I_O	output current	from buffered bus; $V_{TX} = V_{TY}$ = 1 V; SX and SY LOW on I^2C-bus = 0.4 V		60	130	-	mA
I_L	leakage current	on buffered bus; $V_{TX} = V_{TY} = V_{CC}$ = 15 V; SX and SY HIGH		-	-	10	µA
Input currents							
I_I	input current	from I^2C-bus on SX and SY					
		RX and RY HIGH or LOW; SX and SY LOW ≤ 1 V	[1]	-	−0.3	−1	mA
		RX and RY HIGH; SX and SY HIGH > 1.4 V	[1]	-	-	10	µA
		from buffered bus on RX and RY; SX and SY HIGH or LOW; $V_{RX} = V_{RY}$ = 0.4 V	[2]	-	−1.5	−10	µA
I_L	leakage current	on buffered bus input on RX and RY; $V_{RX} = V_{RY}$ = 15 V		-	-	10	µA

Table 6. Characteristics *...continued*

T_{amb} = −40 °C to +85 °C unless otherwise specified; voltages are specified with respect to GND with V_{CC} = 2.5 V to 15 V unless otherwise specified. Typical values are measured at V_{CC} = 5 V and T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output logic LOW level							
Pins SX and SY							
V_{OL}	LOW-level output voltage	on Standard-mode or Fast-mode I^2C-bus					
		$I_{SX} = I_{SY}$ = 3 mA; Figure 6		-	0.7	0.74	V
		$I_{SX} = I_{SY}$ = 0.3 mA; Figure 5		-	0.6	0.65	V
		on 5 V Fm+ I^2C-bus					
		$I_{SX} = I_{SY}$ = 7 mA		-	-	1	V
$\Delta V/\Delta T$	voltage variation with temperature	$I_{SX} = I_{SY}$ = 0.3 mA to 3 mA		-	0	-	%/K
Input logic switching threshold voltages							
Pins SX and SY							
V_{IL}	LOW-level input voltage	on normal I^2C-bus; Figure 7	[3]	-	-	425	mV
$V_{th(IH)}$	HIGH-level input threshold voltage	on normal I^2C-bus; Figure 8		580	-	-	mV
$\Delta V/\Delta T$	voltage variation with temperature			-	0	-	%/K
Pins RX and RY							
V_{IH}	HIGH-level input voltage	fraction of applied V_{CC}		$0.55V_{CC}$	-	-	V
$V_{th(i)}$	input threshold voltage	fraction of applied V_{CC}		-	$0.48V_{CC}$	-	V
V_{IL}	LOW-level input voltage	fraction of applied V_{CC}		-	-	$0.4V_{CC}$	V
Logic level threshold difference							
ΔV	voltage difference	SX and SY; SX output LOW at 0.3 mA to SX input HIGH maximum	[4]	50	-	-	mV
Thermal resistance							
$R_{th(j-pcb)}$	thermal resistance from junction to printed-circuit board	SOT96-1 (SO8); average lead temperature at board interface		-	127	-	K/W
Bus release on V_{CC} failure							
V_{CC}	supply voltage	SX, SY, TX and TY; voltage at which all buses are to be released at 25 °C		-	-	1	V
$\Delta V/\Delta T$	voltage variation with temperature	Figure 9		-	−4	-	%/K

Table 6. Characteristics *...continued*

T_{amb} = −40 °C to +85 °C unless otherwise specified; voltages are specified with respect to GND with V_{CC} = 2.5 V to 15 V unless otherwise specified. Typical values are measured at V_{CC} = 5 V and T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Buffer response time[5]						
V_{CC} = 5 V; pin TX pull-up resistor = 160 Ω; pin SX pull-up resistor = 2.2 kΩ; no capacitive load						
t_d	delay time	V_{SX} to V_{TX}, V_{SY} to V_{TY}; on **falling** input between V_{SX} = input switching threshold, and V_{TX} output falling to 50 % V_{CC}	-	50	-	ns
		V_{SX} to V_{TX}, V_{SY} to V_{TY}; on **rising** input between V_{SX} = input switching threshold, and V_{TX} output reaching 50 % V_{CC}	-	60	-	ns
		V_{RX} to V_{SX}, V_{RY} to V_{SY}; on **falling** input between V_{RX} = input switching threshold, and V_{SX} output falling to 50 % V_{CC}	-	100	-	ns
		V_{RX} to V_{SX}, V_{RY} to V_{SY}; on **rising** input between V_{RX} = input switching threshold, and V_{SX} output reaching 50 % V_{CC}	-	95	-	ns
Input capacitance						
C_i	input capacitance	effective input capacitance of any signal pin measured by incremental bus rise times; guaranteed by design, not production tested	-	-	10	pF

[1] This bus pull-up current specification is intended to assist design of the bus pull-up resistor. It is not a specification of the sink capability (see V_{OL} under sub-section “Output logic LOW level”). The maximum static sink current for a Standard/Fast-mode I²C-bus is 3 mA and PCA9600 is guaranteed to sink 3 mA at SX/SY when its pins are holding the bus LOW. However, when an external device pulls the SX/SY pins below 1.4 V, the PCA9600 may source a current between 0 mA and 1 mA maximum. When that other external device is driving LOW it will pull the bus connected to SX or SY down to, or below, the 0.4 V level referenced in the I²C-bus specification and in these test conditions. Then that device must be able to sink up to 1 mA coming from SX/SY plus the usual pull-up current. Therefore the external pull-up used at SX/SY should be limited to 2 mA. The typical and maximum currents sourced by SX/SY as a function of junction temperature are shown in Figure 10, and the equivalent circuit at the SX/SY interface is shown in Figure 4.

[2] Valid over temperature for $V_{CC} \leq 5$ V. At higher V_{CC}, this current may increase to maximum −20 μA at V_{CC} = 15 V.

[3] The input logic threshold is independent of the supply voltage.

[4] The minimum value requirement for pull-up current, 0.3 mA, guarantees that the minimum value for V_{SX} output LOW will always exceed the maximum V_{SX} input HIGH level to eliminate any possibility of latching. The specified difference is guaranteed by design within any IC. While the tolerances on absolute levels allow a small probability, the LOW from one SX output is recognized by an SX input of another PCA9600, this has no consequences for normal applications. In any design the SX pins of different ICs should never be linked because the resulting system would be very susceptible to induced noise and would not support all I²C-bus operating modes.

[5] The fall time of V_{TX} from 5 V to 2.5 V in the test is approximately 10 ns.
The fall time of V_{SX} from 5 V to 2.5 V in the test is approximately 20 ns.
The rise time of V_{TX} from 0 V to 2.5 V in the test is approximately 15 ns.
The rise time of V_{SX} from 0.7 V to 2.5 V in the test is approximately 25 ns.

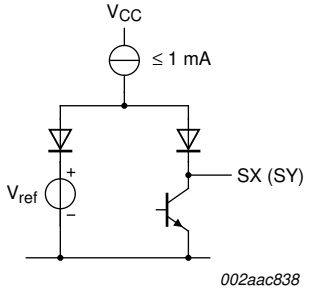
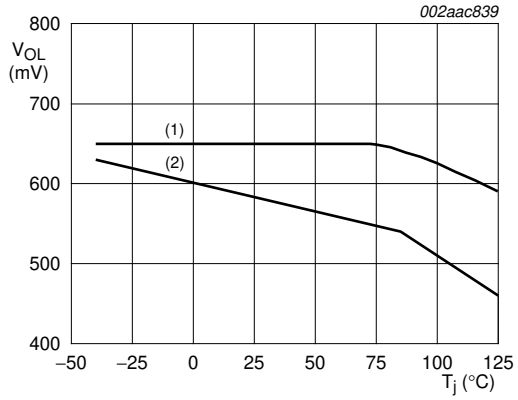


Fig 4. Equivalent circuit at SX/SY

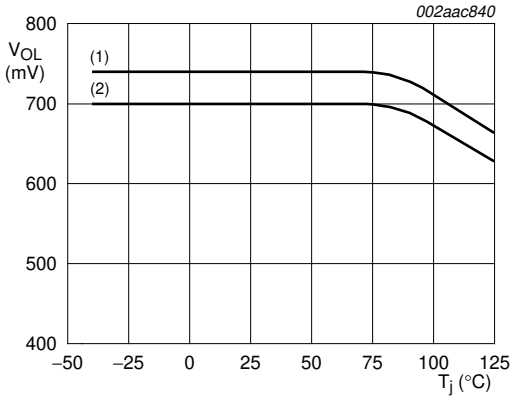


V_{OL} at SX typical and limits over temperature.

(1) Maximum.

(2) Typical.

Fig 5. V_{OL} as a function of junction temperature (I_{OL} = 0.3 mA)

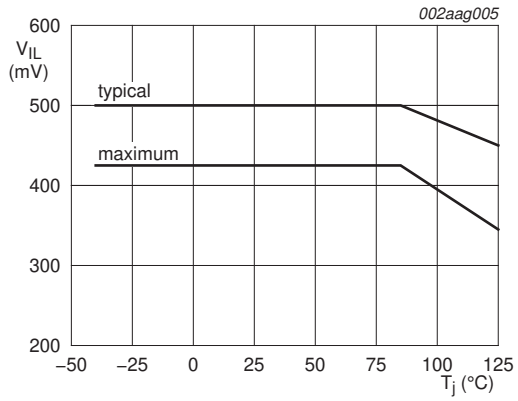


V_{OL} at SX typical and limits over temperature.

(1) Maximum.

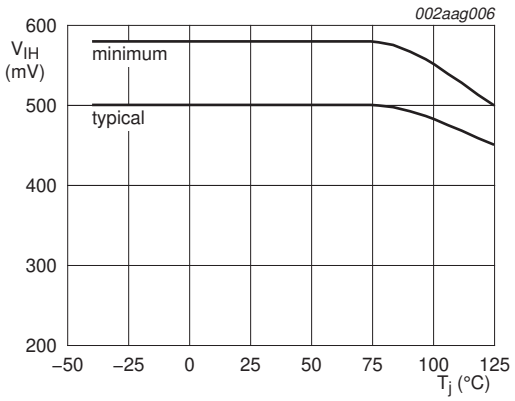
(2) Typical.

Fig 6. V_{OL} as a function of junction temperature (I_{OL} = 3 mA)



V_{IL} at SX changes over temperature range.

Fig 7. V_{IL} as a function of junction temperature; maximum and typical values



V_{IH} at SX changes over temperature range.

Fig 8. V_{IH} as a function of junction temperature; minimum and typical values

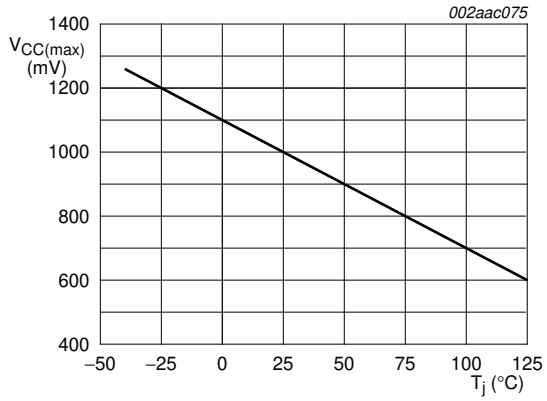
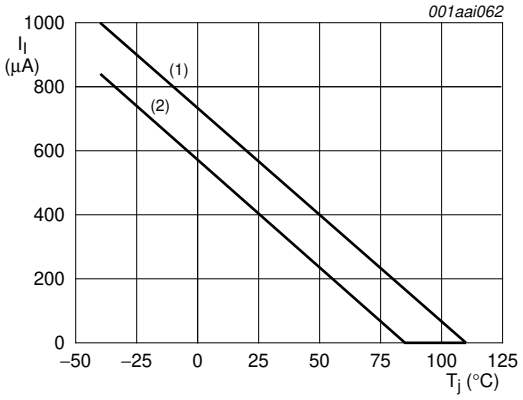


Fig 9. V_{CC} bus release limit over temperature; maximum values



(1) Maximum.

(2) Typical.

Fig 10. Current sourced out of SX/SY as a function of junction temperature if these pins are externally pulled to 0.4 V or lower

10. Application information

Refer to PCA9600 data sheet and application notes *AN10658* and *AN255* for more detailed application information.

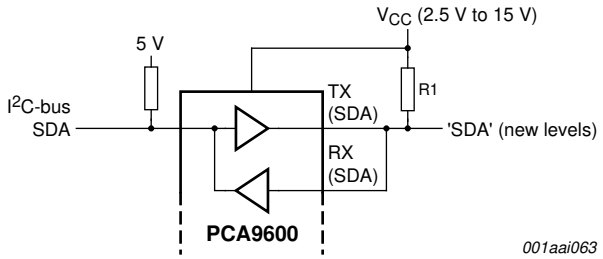
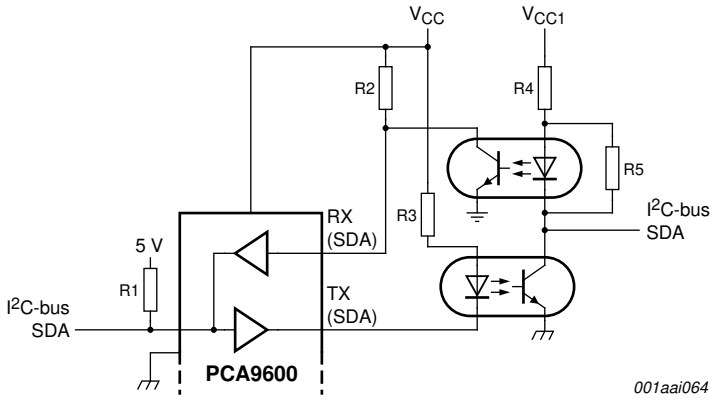


Fig 11. Interfacing a standard 3 mA I²C-bus or one with TTL levels (e.g. SMBus) to higher voltage or higher current sink (e.g. Fast-mode Plus) devices



This simple example may be limited, if using lowest-cost couplers, to speeds as low as 5 kHz. Refer to application notes for schematics suitable for operation to 400 kHz or higher.

Fig 12. Galvanic isolation of I²C-bus nodes via opto-couplers

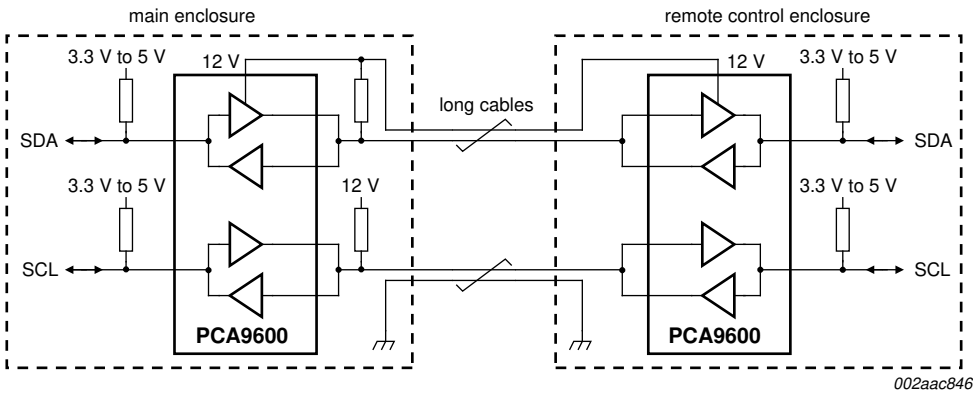


Fig 13. Long distance I²C-bus communication

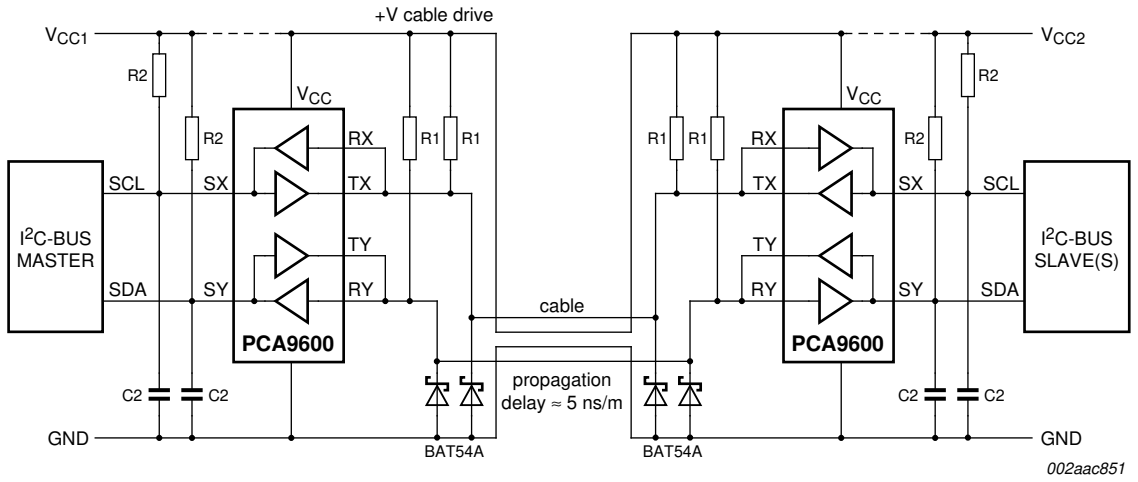


Fig 14. Driving ribbon or flat telephone cables

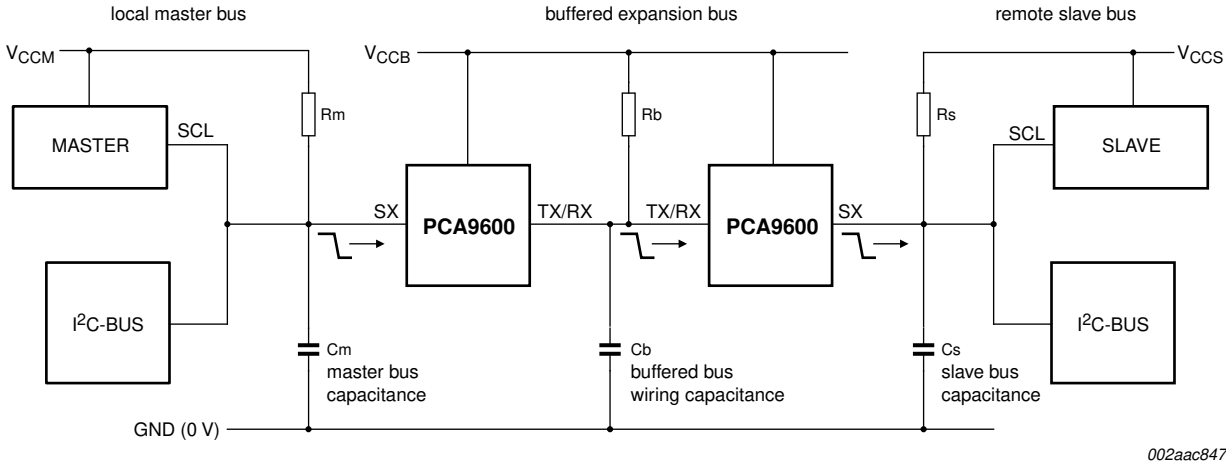
Table 7. Examples of bus capability

Refer to Figure 14.

V_{CC1} (V)	+V cable (V)	V_{CC2} (V)	R1 (Ω)	R2 (kΩ)	C2 (pF)	Cable length (m)	Cable capacitance	Cable delay	Set master nominal SCL		Effective bus clock speed (kHz)	Max. slave response delay
									HIGH period (ns)	LOW period (ns)		
5	12	5	750	2.2	400	250	n/a (delay based)	1.25 µs	600	3850	125	normal specification 400 kHz parts
5	12	5	750	2.2	220	100	n/a (delay based)	500 ns	600	2450	195	normal specification 400 kHz parts
3.3	5	3.3	330	1	220	25	1 nF	125 ns	260	770	620	meets Fm+ specification
3.3	5	3.3	330	1	100	3	120 pF	15 ns	260	720	690	meets Fm+ specification

For more examples of faster alternatives for driving over longer cables such as Cat5 communication cable, see *AN10658*. Communication at 1 MHz is possible over short cables and > 400 kHz is possible over 50 m of cable.

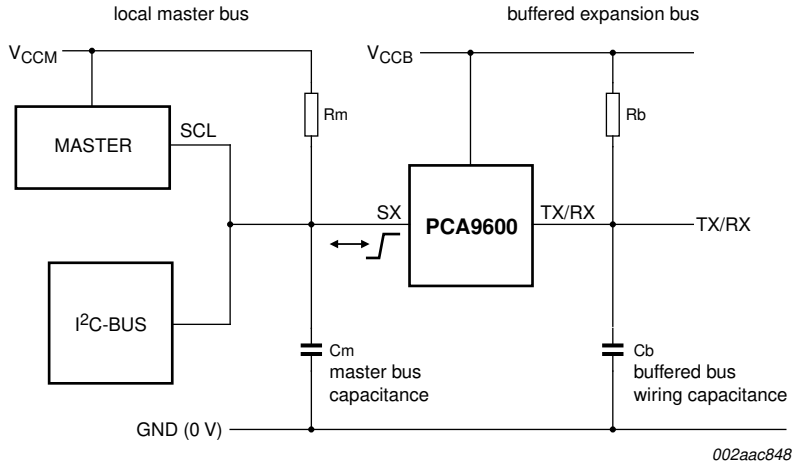
10.1 Calculating system delays and bus clock frequency



Effective delay of SCL at slave: $120 + 17V_{CCM} + (2.5 + 4 \times 10^9 \times C_b) \times V_{CCB} + 10V_{CCS}$ (ns).

C = F; V = V.

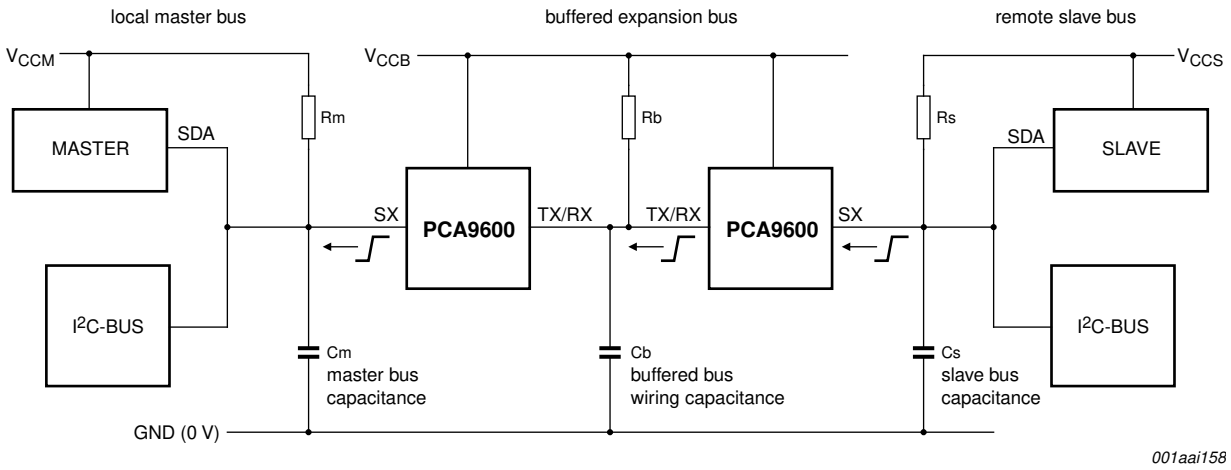
Fig 15. Falling edge of SCL at master is delayed by the buffers and bus fall times



Effective delay of SCL at master: $115 + (Rm \times Cm) + (0.7 \times Rb \times Cb)$ (ns).

C = F; R = Ω.

Fig 16. Rising edge of SCL at master is delayed (clock stretch) by buffer and bus rise times



Effective delay of SDA at master: 115 + 0.2(Rs × Cs) + 0.7[(Rb × Cb) + (Rm × Cm)] (ns).

C = F; R = Ω.

Fig 17. Rising edge of SDA at slave is delayed by the buffers and bus rise times

Figure 15, Figure 16, and Figure 17 show the PCA9600 used to drive extended bus wiring with relatively large capacitances linking two I²C-bus nodes. It includes simplified expressions for making the relevant timing calculations for 3.3 V or 5 V operation. Because the buffers and the wiring introduce timing delays, it may be necessary to decrease the nominal SCL frequency. In most cases the actual bus frequency will be lower than the nominal Master timing due to bit-wise stretching of the clock periods.

The delay factors involved in calculation of the allowed bus speed are:

A — The propagation delay of the master signal through the buffers and wiring to the slave. The important delay is that of the falling edge of SCL because this edge 'requests' the data or acknowledge from a slave. See Figure 15.

B — The effective stretching of the nominal LOW period of SCL at the master caused by the buffer and bus rise times. See Figure 16.

C — The propagation delay of the slave's response signal through the buffers and wiring back to the master. The important delay is that of a rising edge in the SDA signal. Rising edges are always slower and are therefore delayed by a longer time than falling edges. (The rising edges are limited by the passive pull-up while falling edges are actively driven); see Figure 17.

The timing requirement in any I²C-bus system is that a slave's data response (which is provided in response to a falling edge of SCL) must be received at the master before the end of the corresponding LOW period of SCL as appears on the bus wiring at the master. Since all slaves will, as a minimum, satisfy the worst case timing requirements of their speed class (Fast-mode, Fm+, etc.), they must provide their response, allowing for the set-up time, within the minimum allowed clock LOW period, e.g., 450 ns (max.) for Fm+ parts. In systems that introduce additional delays it may be necessary to extend the minimum clock LOW period to accommodate the 'effective' delay of the slave's response. The effective delay of the slave's response equals the total delays in SCL falling edge from the master reaching the slave (Figure 15) minus the effective delay (stretch) of the SCL rising edge (Figure 16) plus total delays in the slave's response data, carried on

SDA, reaching the master (Figure 17).

The master microcontroller should be programmed to produce a nominal SCL LOW period as follows:

$$SCL\ LOW \geq (slave\ response\ delay\ to\ valid\ data\ on\ its\ SDA + A - B + C + data\ set\text{-}up\ time)\ ns \quad (1)$$

The actual LOW period will become (the programmed value + the stretching time B). When this actual LOW period is then less than the specified minimum, the specified minimum should be used.

Example 1:

It is required to connect an Fm+ slave, with Rs × Cs product of 100 ns, to a 5 V Fast-mode system also having 100 ns Rm × Cm using two PCA9600's to buffer a 5 V bus with 4 nF loading and 160 Ω pull-up.

Calculate the allowed bus speed:

Delay A = 120 + 85 + (2.5 + [4 × 4]) × 5 + 50 = 347.5 ns

Delay B = 115 + 100 + 70 = 285 ns

Delay C = 115 + 20 + 0.7(100 + 100) = 275 ns

The maximum Fm+ slave response delay must be < 450 ns so the programmed LOW period is calculated as:

LOW ≥ 450 + 347.5 − 285 + 275 + 100 = 887.5 ns

The actual LOW period will be 887.5 + 285 = 1173 ns, which is below the Fast-mode minimum, so the programmed LOW period must be increased to (1300 − 285) = 1015 ns, so the actual LOW equals the 1300 ns requirement and this shows that this Fast-mode system may be safely run to its limit of 400 kHz.

Example 2:

It is required to buffer a Master with Fm+ speed capability, but only 3 mA sink capability, to an Fm+ bus. All the system operates at 3.3 V. The Master Rm × Cm product is 50 ns. Only one PCA9600 is used. The Fm+ bus becomes the buffered bus. The Fm+ bus has 200 pF loading and 150 Ω pull-up, so its Rb × Cb product is 30 ns. The Fm+ slave has a specified data valid time $t_{VD;DAT}$ maximum of 300 ns.

Calculate the allowed maximum system bus speed. (Note that the fixed values in the delay equations represent the internal propagation delays of the PCA9600. Only one PCA9600 is used here, so those fixed values used below are taken from the characteristics.)

The delays are:

Delay A = 40 + 56 + (2.5 + [4 × 0.2]) × 3.3 = 107 ns

Delay B = 115 + 50 + 21 = 186 ns

Delay C = 70 + 0.7(50 + 30) = 126 ns

The programmed LOW period is calculated as:

SCL LOW ≥ 300 + 117 − 186 + 126 + 50 = 407 ns

The actual LOW period will be 407 + 126 = 533 ns, which exceeds the minimum Fm+ 500 ns requirement. This system requires the bus LOW period, and therefore cycle time, to be increased by 33 ns so the system must run slightly below the 1 MHz limit.

The possible maximum speed has a cycle period of 1033 ns or 968 kHz.

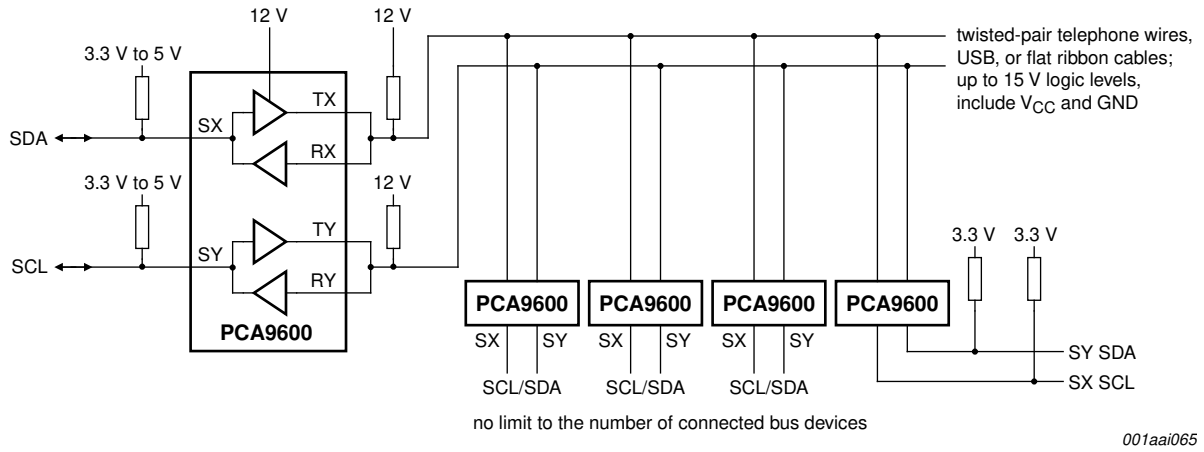
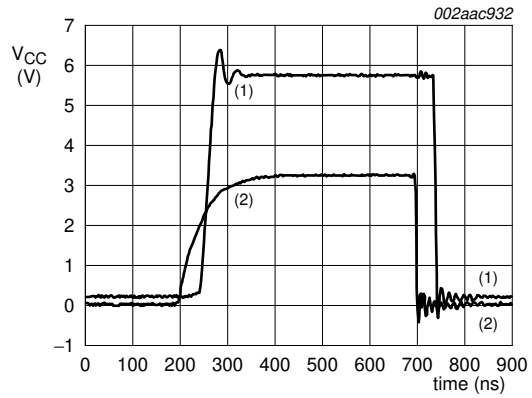


Fig 18. I²C-bus multipoint application

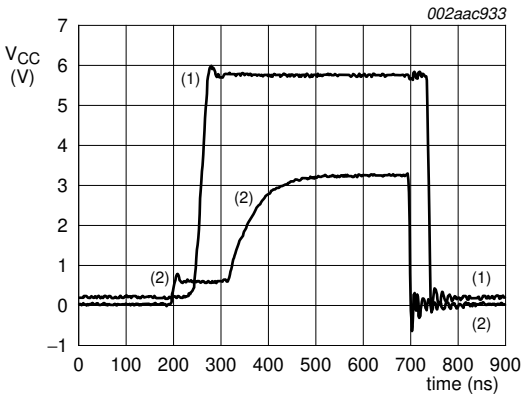
There is an Excel calculator which makes it easy to determine the maximum I²C-bus clock speed when using the PCA9600. The calculator and instructions can be found at www.nxp.com/clockspeedcalculator.



(1) TX output.

(2) SX input.

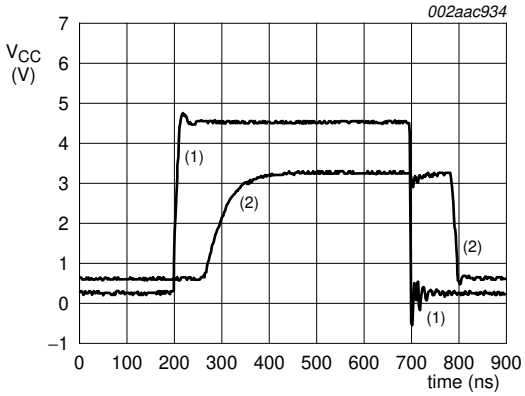
Fig 19. Propagation SX to TX with V_{RX} = V_{CC} = 3.3 V (SX pull-up to 3.3 V; TX pull-up to 5.7 V)



(1) TX/RX output.

(2) SX input.

Fig 20. Propagation SX to TX with RX tied to TX; V_{CC} = 3.3 V (SX pull-up to 3.3 V; TX pull-up to 5.7 V)



(1) RX input.

(2) SX output.

Fig 21. Propagation RX to SX (SX pull-up to 3.3 V; V_{CC} = 3.3 V; RX pull-up to 4.6 V)

10.2 Negative undershoot below absolute minimum value

The reason why the IC pin reverse voltage on pins TX and RX in Table 5 “Limiting values” is specified at such a low value, −0.3 V, is **not** that applying larger voltages is likely to cause damage but that it is expected that, in normal applications, there is no reason why larger DC voltages will be applied. This ‘absolute maximum’ specification is intended to be a DC or continuous ratings and the nominal DC I^2C-bus voltage LOW usually does not even reach 0 V. Inside PCA9600 at every pin there is a large protective diode connected to the GND pin and that diode will start to conduct when the pin voltage is more than about −0.55 V with respect to GND at 25 °C ambient.

Figure 22 shows the measured characteristic for one of those diodes inside PCA9600. The plot was made using a curve tracer that applies 50 Hz mains voltage via a series resistor, so the pulse durations are long duration (several milliseconds) and are reaching peaks of over 2 A when more than −1.5 V is applied. The IC becomes very hot during this

testing but it was not damaged. Whenever there is current flowing in any of these diodes it is **possible** that there can be faulty operation of any IC. For that reason we put a specification on the negative voltage that is allowed to be applied. It is selected so that, at the highest allowed junction temperature, there will be a big safety factor that guarantees the diode will not conduct and then we do not need to make any 100 % production tests to guarantee the published specification.

For the PCA9600, in specific applications, there will always be transient overshoot and ringing on the wiring that can cause these diodes to conduct. Therefore we designed the IC to withstand those transients and as a part of the qualification procedure we made tests, using DC currents to more than twice the normal bus sink currents, to be sure that the IC was not affected by those currents. For example, the TX/TY and RX/RY pins were tested to at least −80 mA which, from Figure 22, would be more than −0.8 V. The correct functioning of the PCA9600 is not affected even by those large currents. The Absolute Maximum (DC) ratings are not intended to apply to transients but to steady state conditions. This explains why you will never see any problems in practice even if, during transients, more than −0.3 V is applied to the bus interface pins of PCA9600.

Figure 22 “Diode characteristic curve” also explains how the general Absolute Maximum DC specification was selected. The current at 25 °C is near zero at −0.55 V. The PCA9600 is allowed to operate with +125 °C junction and that would cause this diode voltage to decrease by 100 × 2 mV = 200 mV. So for zero current we need to specify −0.35 V and we publish −0.3 V just to have some extra margin.

Remark: You should not be concerned about the **transients** generated on the wiring by a PCA9600 in normal applications and that is input to the TX/RX or TY/RY pins of another PCA9600. Because not all ICs that may be driven by PCA9600 are designed to tolerate negative transients, in Section 10.2.1 “Example with questions and answers” we show they can be managed if required.

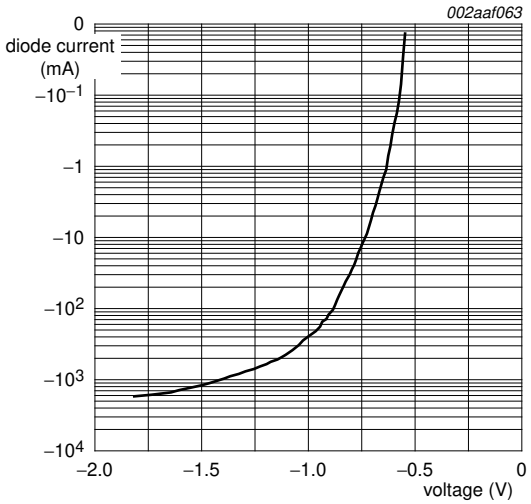


Fig 22. Diode characteristic curve

10.2.1 Example with questions and answers

Question: On a falling edge of TX we measure undershoot at −800 mV at the linked TX, RX pins of the PCA9600 that is generating the LOW, but the PCA9600 data sheet specifies minimum −0.3 V. Does this mean that we violate the data sheet absolute value?

Answer: For PCA9600 the −0.3 V Absolute Maximum rating is not intended to apply to transients, it is a DC rating. As shown in Figure 23, there is no theoretical reason for any undershoot at the IC that is driving the bus LOW and no significant undershoot should be observed when using reasonable care with the ground connection of the 'scope. It is more likely that undershoot observed at a driving PCA9600 is caused by local stray inductance and capacitance in the circuit and by the oscilloscope connections. As shown, undershoot will be generated by PCB traces, wiring, or cables driven by a PCA9600 because the allowed value of the I^2C-bus pull-up resistor generally is larger than that required to correctly terminate the wiring. In this example, with no IC connected at the end of the wiring, the undershoot is about 2 V.

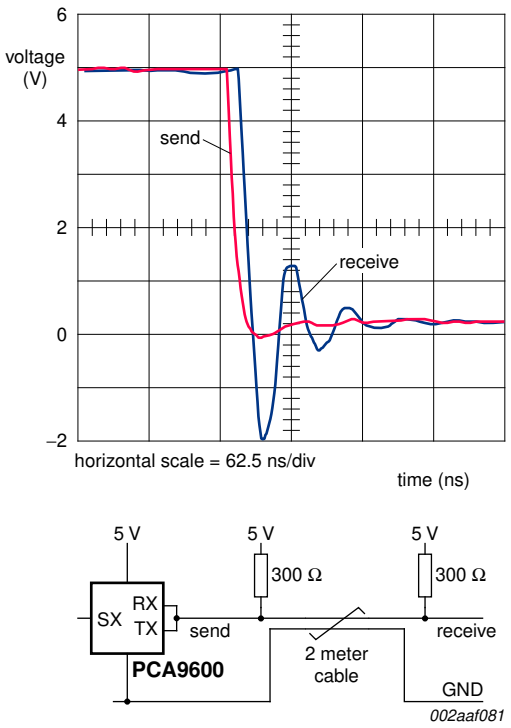


Fig 23. Transients generated by the bus wiring

Question: We have 2 meters of cable in a bus that joins the TX/RX sides of two PCA9600 devices. When one TX drives LOW the other PCA9600 TX/RX is driven to −0.8 V for over 50 ns. What is the expected value and the theoretically allowed value of undershoot?

Answer: Because the cable joining the two PCA9600s is a 'transmission line' that will have a characteristic impedance around 100 Ω and it will be terminated by pull-up resistors that are larger than that characteristic impedance there will always be negative undershoot generated. The duration of the undershoot is a function of the cable length and the input impedance of the connected IC. As shown in Figure 24, the transient undershoot will be limited, by the diodes inside PCA9600, to around −0.8 V and that will not cause problems for PCA9600. Those transients will **not** be passed inside the IC to the SX/SY side of the IC.

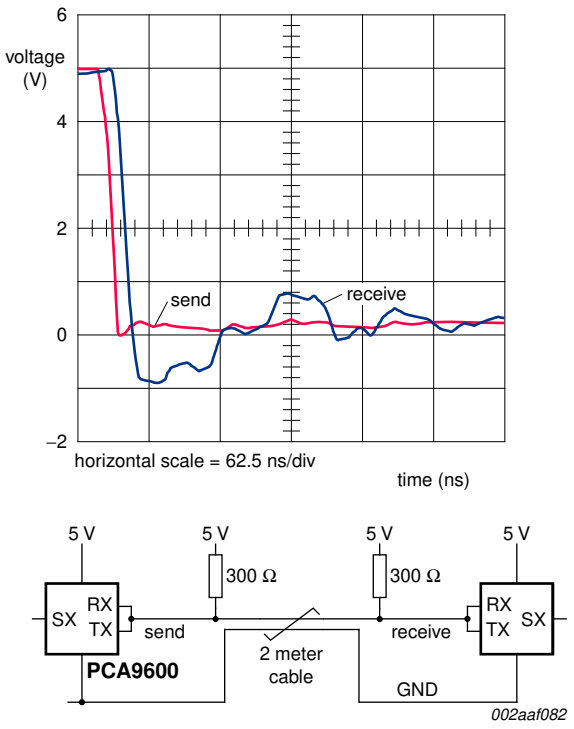


Fig 24. Wiring transients limited by the diodes in PCA9600

Question: If we input 800 mV undershoot at TX, RX pins, what kind of problem is expected?

Answer: When that undershoot is generated by another PCA9600 and is simply the result of the system wiring, then there will be no problems.

Question: Will we have any functional problem or reliability problem?

Answer: No.

Question: If we add 100 Ω to 200 Ω at signal line, the overshoot becomes slightly smaller. Is this a good idea?

Answer: No, it is not necessary to add any resistance. When the logic signal generated by TX or TY of PCA9600 drives long traces or wiring with ICs other than PCA9600 being driven, then adding a Schottky diode (BAT54A) as shown in Figure 25 will clamp the wiring undershoot to a value that will not cause conduction of the IC's internal diodes.

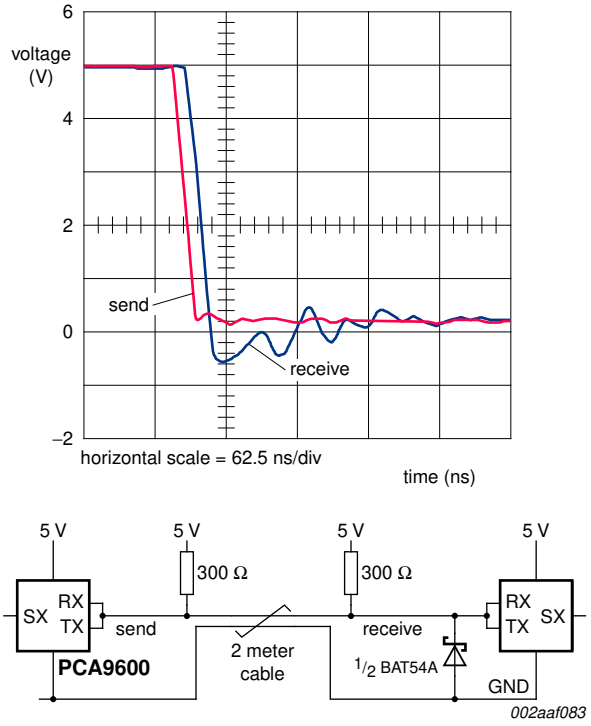
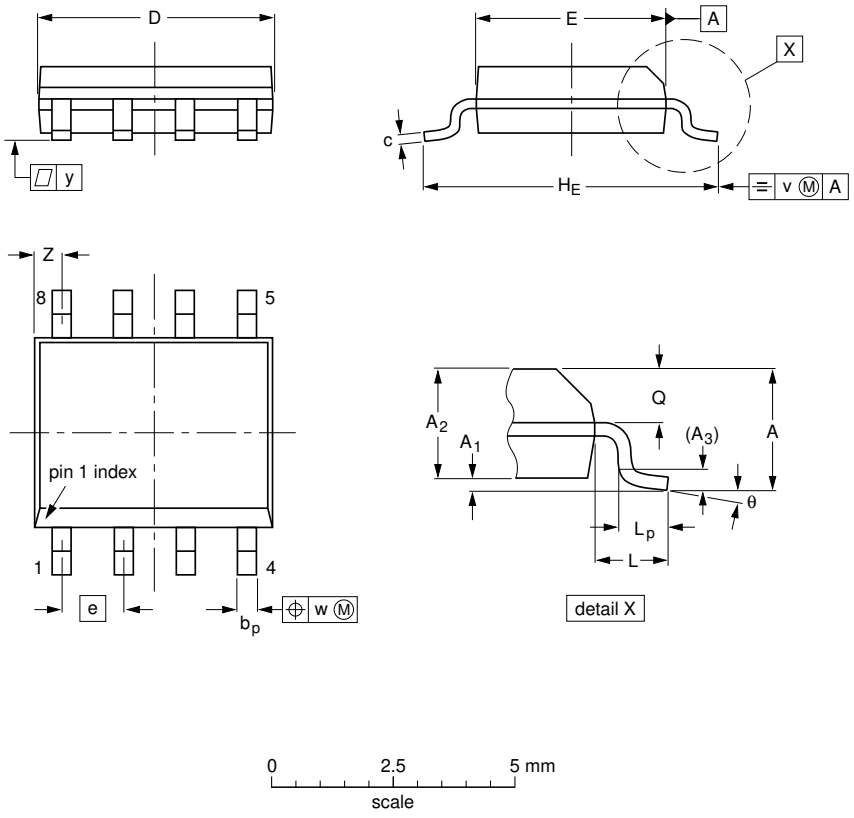


Fig 25. Wiring transients limited by a Schottky diode

11. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

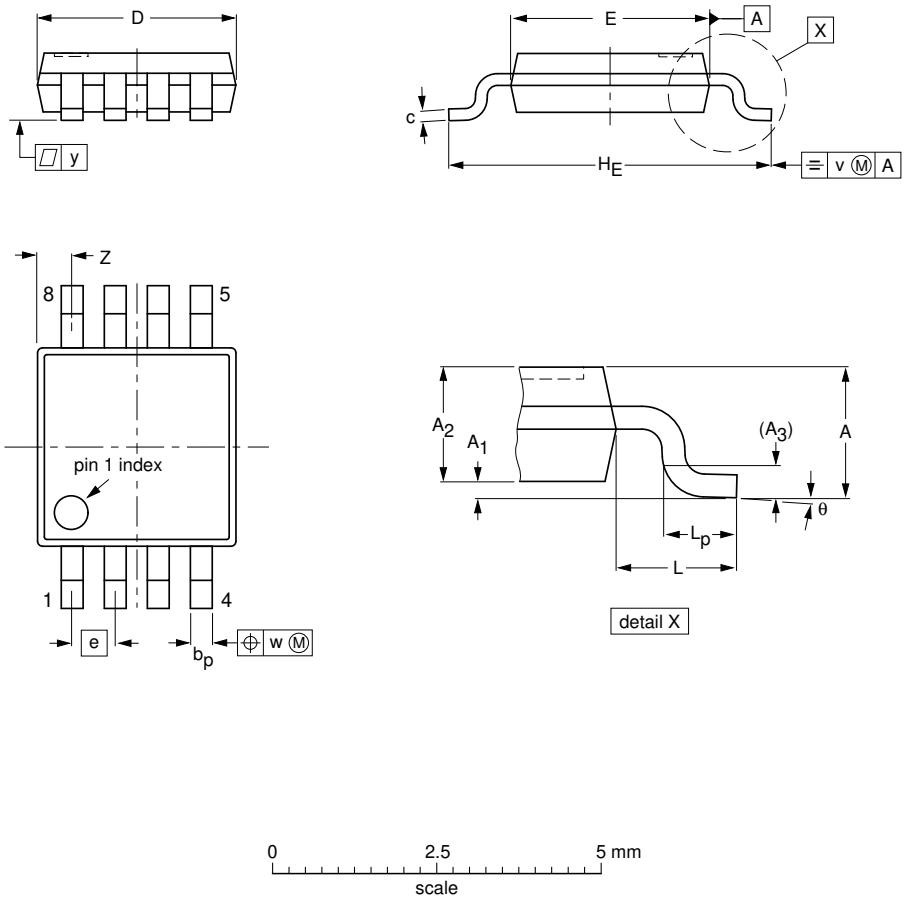
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 26. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 27. Package outline SOT505-1 (TSSOP8)