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# PCA9617A

# Level-Translating Fm+ I²C-Bus Repeater

The PCA9617A is an I²C−bus repeater that provides level shifting between low voltage (0.8 V to 5.5 V) and higher voltage (2.2 V to 5.5 V) for Fast−Mode Plus (Fm+) I²C−bus or SMBus applications.

### Features

- Two Channel, Bidirectional Buffer Isolates Capacitance and Allows 540 pF on Either Side of the Device at 1 MHz and up to 4000 pF at Lower Speeds
- Voltage Level Translation from 0.8 V to 5.5 V and from 2.2 V to 5.5 V
- Footprint and Functional replacement for PCA9517A at Fast−mode speeds
- Port A Operating Supply Voltage Range of 0.8 V to 5.5 V with Normal Levels
- Port B Operating Supply Voltage Range of 2.2 V to 5.5 V with Static Offset Level
- 5 V Tolerant I²C−bus and Enable Pins
- 0 Hz to 1000 kHz Clock Frequency (the Maximum System Operating Frequency May be Less than 1000 kHz Because of the Delays Added by the Repeater)
- Active HIGH Repeater Enable Input Feferenced to $V_{CC(B)}$
- Open−Drain Input/Outputs
- Latching Free Operation
- Supports Arbitration and Clock Stretching Across the Repeater
- Accommodates Standard−mode, Fast−mode and Fast−mode Plus I²C−bus Devices, SMBus (Standard and High Power Mode), PMBus and Multiple Masters
- Powered−off High−impedance I²C−bus Pins
- Available in: Micro−8,
- ESD Performance: 8 kV HBM, 800 V MM
  2000 V CDM
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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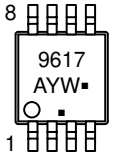
**MARKING DIAGRAMS**

**Micro8™**
**DM SUFFIX**
**CASE 846A**




A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

### General Description

The PCA9617A is an $I^2C$−bus repeater that provides level shifting between low voltage (0.8 V to 5.5 V) and higher voltage (2.2 V to 5.5 V) for Fast−Mode Plus (Fm+) $I^2C$−bus or SMBus applications. While retaining all the operating modes and features of the $I^2C$−bus system during the level shifts, it also permits extension of the $I^2C$−bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 540 pF at 1 MHz or up to 4000 pF at lower speeds. Using the PCA9617A enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high−impedance when the PCA9617A is unpowered.

The 2.2 V to 5.5 V bus port B drivers have the static level offset, while the adjustable voltage bus port A drivers eliminate the static offset voltage. This results in a LOW on the port B translating into a nearly 0 V LOW on the port A which accommodates the smaller voltage swings of lower voltage logic.

The static offset design of the port B PCA9617A I/O drivers prevents them from being connected to the static or incremented offset of other bus buffers. Port A of two or more PCA9617As can be connected together, however, to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or incremented offset outputs. Multiple PCA9617As can be connected in series, port A to port B, with no build−up in offset voltage with only time of flight delays to consider.

The PCA9617A drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.2 V. The EN pin is referenced to $V_{CC(B)}$ and can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull−down on the port B internal buffer LOW is set for approximately 0.55 V, while the input threshold of the internal buffer is set about 90 mV lower (0.45 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a latching condition from occurring. The output pull−down on port A drives a hard LOW and the input level is set at $0.35V_{CC(A)}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.8 V.

## BLOCK DIAGRAM

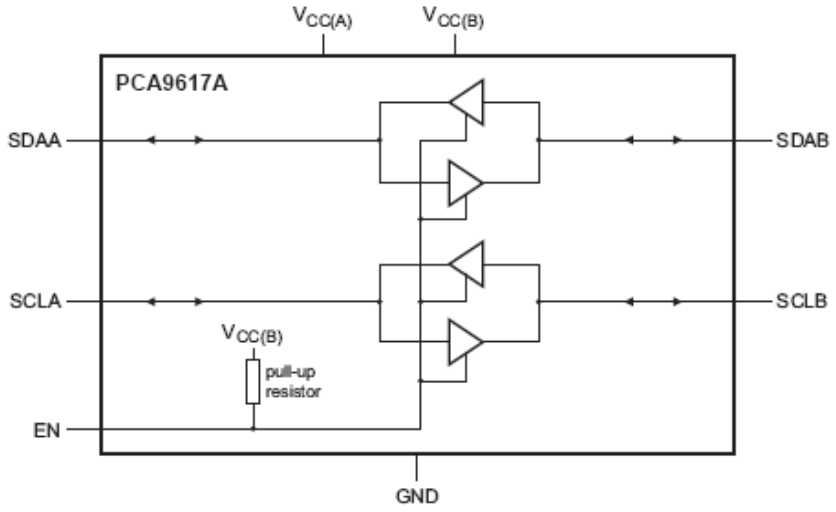



**Figure 1. Block Diagram of PCA9617A**

## PIN ASSIGNMENT

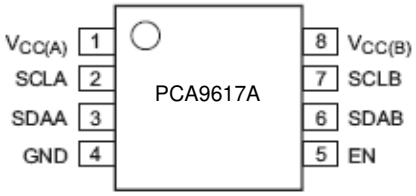



**Figure 2. Micro−8**

### PIN DESCRIPTIONS

| Symbol | Pin | Description |
|---|---|---|
| $V_{CC(A)}$ | 1 | A−Side Supply Voltage (0.8 V to 5.5 V) |
| SCLA | 2 | Open−Drain I/O, Serial Clock A−Side Bus |
| SDAA | 3 | Open−Drain I/O, Serial Data A−Side Bus |
| GND | 4 | Ground |
| EN | 5 | Active−HIGH Repeater Enable |
| SDAB | 6 | Open−Drain I/O, Serial Data B−Side Bus |
| SCLB | 7 | Open−Drain I/O, Serial Clock B−Side Bus |
| $V_{CC(B)}$ | 8 | B−Side Supply Voltage (2.2 V to 5.5 V) |

## FUNCTIONAL DESCRIPTION

Please refer to Figure 1 "Block Diagram of PCA9617A".

The PCA9617A enables I²C−bus or SMBus translation down to $V_{CC(A)}$ as low as 0.8 V without degradation of system performance. The PCA9617A contains two bidirectional open−drain buffers specifically designed to support up−translation/down−translation between the low voltage (as low as 0.8 V) and a 2.5 V, 3.3 V or 5 V I²C−bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered ($V_{CC(B)}$ and/or $V_{CC(A)}$ = 0 V). The PCA9617A includes a power−up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.2 V and until after the internal reference circuits have settled in ~400 μs, and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power−up. After power−up and with the enable (EN) HIGH, a LOW level on port A (below $0.3V_{CC(A)}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.55 V. When port A rises above $0.3V_{CC(A)}$, the port B pull−down driver is turned off and the external pull−up resistor pulls the pin HIGH. When port B falls first and goes below 0.4 V, the port A driver is turned on and port A pulls down to ~0 V. The port A pull−down is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage goes below 0.4 V, the port B pull−down driver is enabled and port B will only be able to rise to 0.55 V until port A rises above $0.3V_{CC(A)}$, then port B will continue to rise being pulled up by the external pull−up resistor. The $V_{CC(A)}$ is only used to provide the $0.35V_{CC(A)}$ reference to the port A input comparators and for the power good detect circuit. The PCA9617A includes a $V_{CC(A)}$ overvoltage disable that turns the channel off if $0.4V_{CC(A)}$ + 0.8 V > $V_{CC(B)}$. The PCA9617A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

### Enable Pin (EN)

The EN pin is active HIGH with thresholds referenced to $V_{CC(B)}$ and an internal pull−up to $V_{CC(B)}$ that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved slave on power−up until after the system power−up reset. It should never change state during an I²C−bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C−bus parts being enabled. The enable does not switch the internal reference circuits so the ~400 μs delay is only seen when $V_{CC(B)}$ comes up.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

### I²C−Bus Systems

As with the standard I²C−bus system, pull−up resistors are required to provide the logic HIGH levels on the buffered bus (standard open−collector configuration of the I²C−bus). The size of these pull−up resistors depends on the system, but each side of the repeater must have a pull−up resistor. This part is designed to work with Standard mode, Fast−mode and Fast−mode Plus I²C−bus devices in addition to SMBus devices. Standard mode and Fast−mode I²C−bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C−bus system where Standard−mode devices, Fast−mode devices and multiple masters are possible. When only Fast−mode Plus devices are used with 30 mA at 5 V drive strength, then lower value pull−up resistors can be used. The B−side RC should not be less than 67.5 ns because shorter RCs increase the turnaround bounce when the B−side transitions from being externally driven to pulled down by its offset buffer.

## APPLICATION DESIGN–IN INFORMATION

A typical application is shown in Figure 3. In this example, the system master is running on a 3.3 V I$^2$C–bus while the slave is connected to a 1.2 V bus. Both buses run at 1000 kHz. Master devices can be placed on either bus.

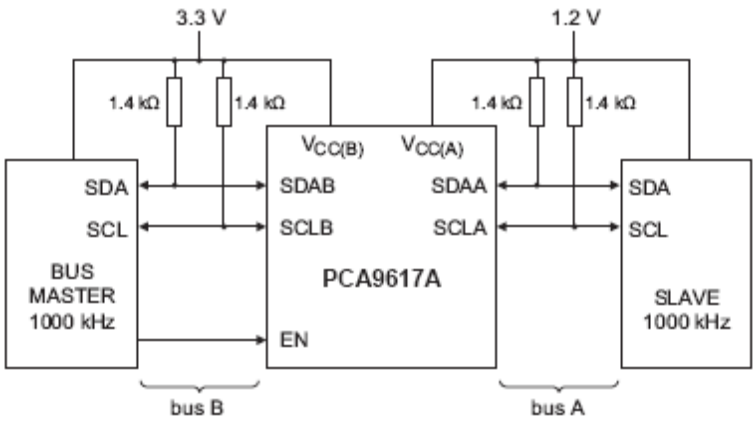



**Figure 3. Typical Application**

The PCA9617A is 5 V tolerant, so it does not require any additional circuitry to translate between 0.8 V to 5.5 V bus voltages and 2.2 V to 5.5 V bus voltages.

When port A of the PCA9617A is pulled LOW by a driver on the I$^2$C–bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9617A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figures 4 and 5. If the bus master in Figure 3 were to write to the slave through the PCA9617A, waveforms shown in Figure 4 would be observed on the A bus. This looks like a normal I$^2$C–bus transmission except that the HIGH level may be as low as 0.8 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

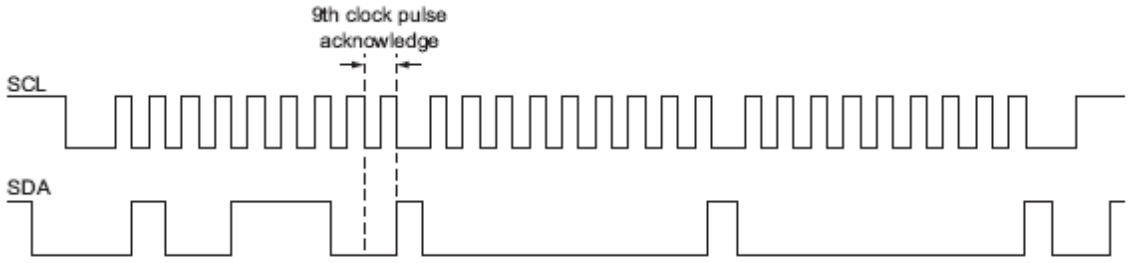



**Figure 4. Bus A (0.9 V to 5.5 V Bus) Waveform**

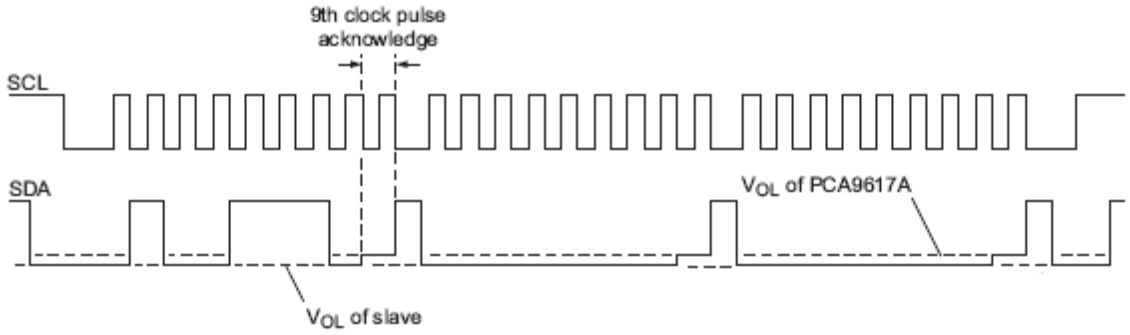



**Figure 5. Bus A (0.9 V to 5.5 V Bus) Waveform**

The internal comparator requires that 0.4 x $V_{CC(A)}$ be less than or equal to $V_{CC(B)}$ – 0.8 V for the device to operate. Since A port is 5 V tolerant, the $V_{CC(A)}$ can be lowered to support device spectrum while still supporting 5 V signals on the A port.

On the B bus side of the PCA9617A, the clock and data lines would have a positive offset from ground equal to the $V_{OL}$ of the PCA9617A. After the eighth clock pulse, the data line will be pulled to the $V_{OL}$ of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9617A for a short delay while the A bus side rises above 0.3 $V_{CC(A)}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9617A ($V_{IL}$) be at or below 0.4 V to be recognized by the PCA9617A and then transmitted to the A bus side.

Multiple PCA9617A port A sides can be connected in a star configuration (Figure 6), allowing all nodes to communicate with each other.

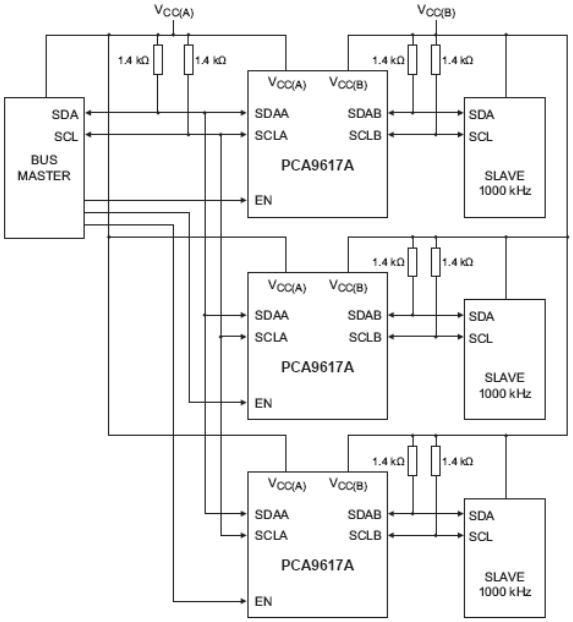
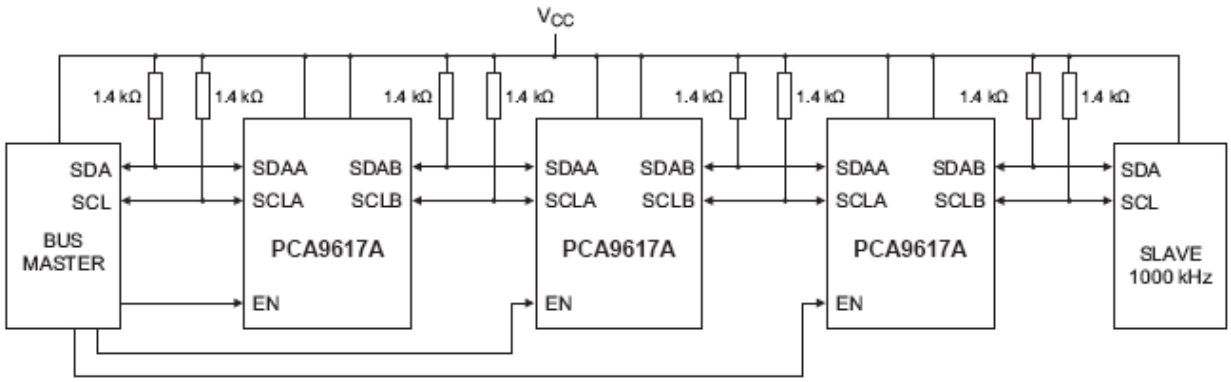


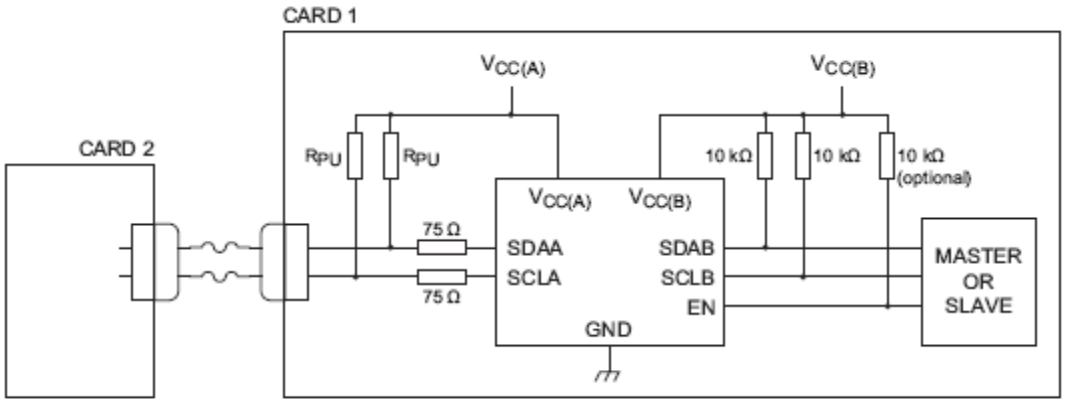

**Figure 6. Typical Star Application**

Multiple PCA9617As can be connected in series (Figure 7) as long as port A is connected to port B. $I^2C$–bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time−of−flight considerations on the maximum bus speed requirements.




Decoupling capacitors not shown for simplicity, but they are required. It is especially important that the decoupling for the PCA9617A $V_{CC(B)}$ be close to the $V_{CC(B)}$ pin.

**Figure 7. Typical Series Application**




Decoupling capacitors not shown for simplicity, but they are required. It is especially important that the decoupling for the PCA9617A $V_{CC(B)}$ be close to the $V_{CC(B)}$ pin.

**Figure 8. Typical Application of PCA9617A Driving a Short Cable**

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC(B)}$ | Supply Voltage Port B | −0.5 to +7.0 | V |
| $V_{CC(A)}$ | Supply Voltage Port A (Adjustable) | −0.5 to +7.0 | V |
| $V_{I/O}$ | Input/Output Pin Voltage Port A, Port B, EN | −0.5 to +7.0 | V |
| $I_{I/O}$ | Input/Output Current Port A, Port B | 50 | mA |
| $I_I$ | Input Current EN | 50 | mA |
| $I_{CC(A)}$, $I_{CC(B)}$ | DC Supply Current | ±100 | mA |
| $I_{GND}$ | DC Ground Current | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | 150 | °C |
| $\theta_{JA}$ | Thermal Resistance Micro8 (Note 1) | 205 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 85°C Micro8 | 609 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| $F_R$ | Flammability Rating Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage Human Body Mode (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4) | > 8000<br>> 800<br>> 2000 | V |
| $I_{LATCHUP}$ | Latchup Performance Above $V_{CC}$ and Below GND at 125°C (Note 5) | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm by 1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22−A114−A.
3. Tested to EIA / JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC(B)}$ | Supply Voltage Port B | 2.2 | 5.5 | V |
| $V_{CC(A)}$ (Note 6) | Supply Voltage Port A | 0.8 | 5.5 | V |
| $V_{I/O}$ | Input/Output Pin Voltage | 0 | 5.5 | V |
| $T_A$ | Operating Free−Air Temperature | −55 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. For part to function, 0.4 x $V_{CC(A)}$ must be equal to or less than $V_{CC(B)}$ − 0.8 V. The voltage on the A port can still be up to 5.5 V without damage to the pins.

**DC CHARACTERISTICS** $V_{CC(A)}$ = 0.8 V to 5.5 V (Note 7); $V_{CC(B)}$ = 2.2 V to 5.5 V; GND = 0 V; $T_A$ = –40°C to +85°C; unless otherwise specified. Typical values measured with $V_{CC(A)}$ = 0.95 V and $V_{CC(B)}$ = 2.5 V at 25°C, unless otherwise noted.

| Symbol | Parameter | Conditions | $T_A$ = –40°C to +85°C | | | $T_A$ = –55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| **SUPPLIES** | | | | | | | | |
| $I_{CC(A)}$ | Supply Current Port A | $V_{CC(A)}$ = 0.95 V | | | 8 | | 8 | μA |
| | | $V_{CC(A)}$ = 5.5V | | | 50 | | 50 | |
| $I_{CCH(B)}$ | Port B HIGH–Level Supply Current | $V_{CC(B)}$ = 5.5 V; | | 1.5 | 2.1 | | 2.1 | mA |
| | | SDAn = SCLn = $V_{CC(n)}$ | | | | | | |
| $I_{CCL(B)}$ | Port B LOW–Level Supply Current | $V_{CC(B)}$ = 5.5 V; | | 1.51 | 2.1 | | 2.1 | mA |
| | | One SDA and SCL = GND; | | | | | | |
| | | Other SDA and SCL Open (with pull–up resistors) | | | | | | |
| **INPUT / OUTPUT SDAB, SCLB** | | | | | | | | |
| $V_{IH}$ | High–Level Input Voltage | | 0.7 x $V_{CC(B)}$ | | | 0.7 x $V_{CC(B)}$ | | V |
| $V_{IL}$ (Note 7) | Low–Level Input Voltage | | | | +0.4 | | +0.4 | V |
| $V_{IK}$ | Input Clamping Voltage | $I_I$ = –18 mA | –1.2 | | –0.3 | –1.2 | –0.3 | V |
| $V_{OL}$ | LOW–Level Output Voltage | $I_{OL}$ = 150 μA; $V_{CC(B)}$ = 2.2 V (Note 8) | 0.425 | | | 0.425 | | V |
| | | $I_{OL}$ = 13 mA; $V_{CC(B)}$ = 2.2 V (Note 9) | | 0.54 | 0.639 | | 0.639 | |
| $V_{OL}$ – $V_{IL}$ (Note 8) | Difference between LOW–Level Output and LOW–Level Input Voltage | $V_{OL}$ at $I_{OL}$ = 1 mA; Guaranteed by design | 60 | 90 | 160 | 60 | 160 | mV |
| $I_{LI}$ | Input Leakage Current | $V_I$ = 5.5 V | | | ±1 | | ±1 | μA |
| $I_{IL}$ | LOW–Level Input Current | SDA, SCL, $V_I$ = 0.2 V | | | 10 | | 10 | μA |
| $C_{I/O}$ | Input/Output Capacitance | $V_I$ = 3 V or 0 V; $V_{CC(B)}$ = 3.3 V; EN = Low | | 7 | 10 | | 10 | pF |
| | | $V_I$ = 3 V or 0 V; $V_{CC}$ = 0 V | | 7 | 10 | | 10 | |
| **INPUT / OUTPUT SDAA, SCLA** | | | | | | | | |
| $V_{IH}$ | High–Level Input Voltage | | 0.7 x $V_{CC(A)}$ | | | 0.7 x $V_{CC(A)}$ | | V |
| $V_{IL}$ (Note 10) | Low–Level Input Voltage | | | | 0.25 x $V_{CC(A)}$ (Note 11) | | 0.25 x $V_{CC(A)}$ (Note 11) | V |
| $V_{IK}$ | Input Clamping Voltage | $I_I$ = –18 mA | –1.2 | | –0.3 | –1.2 | –0.3 | V |
| $V_{OL}$ | LOW–Level Output Voltage | $I_{OL}$ = 13 mA; $V_{CC(B)}$ = 2.2 V | | 0.1 | 0.2 | | 0.2 | V |

7. $V_{CC(A)}$ may be as high as 5.5 V for overvoltage tolerance but 0.4 $V_{CC(A)}$ + 0.8 V ≤ $V_{CC(B)}$ for the channels to be enabled and functional normally.
8. Pull–up should result in $I_{OL}$ ≥ 150 μA.
9. Guaranteed by design and characterization.
10. $V_{IL}$ for port A with envelope noise must be below 0.3 $V_{CC(A)}$ for stable performance.
11. When $V_{CC(A)}$ is less than 1 V, care is required to make certain that the system ground offset and noise are minimized such that there is reasonable difference between the $V_{IL}$ present at the PCA9617A A–side input and the 0.25 $V_{CC(A)}$ input threshold.
12. Power supply decoupling capacitors need to be present for both $V_{CC(A)}$ and $V_{CC(B)}$ and the 0.1 μF decoupling for $V_{CC(B)}$ needs to be located near the $V_{CC(B)}$ pin.

**DC CHARACTERISTICS** $V_{CC(A)}$ = 0.8 V to 5.5 V (Note 7); $V_{CC(B)}$ = 2.2 V to 5.5 V; GND = 0 V; $T_A$ = –40°C to +85°C; unless otherwise specified. Typical values measured with $V_{CC(A)}$ = 0.95 V and $V_{CC(B)}$ = 2.5 V at 25°C, unless otherwise noted.

| Symbol | Parameter | Conditions | $T_A$ = –40°C to +85°C | | | $T_A$ = –55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| **INPUT / OUTPUT SDAA, SCLA** | | | | | | | | |
| $I_{LI}$ | Input Leakage Current | $V_I$ = 5.5 V | | | ±1 | | ±1 | μA |
| $I_{IL}$ | LOW–Level Input Current | SDA, SCL, $V_I$ = 0.2 V | | | 10 | | 10 | μA |
| $C_{I/O}$ | Input/Output Capacitance | $V_I$ = 3 V or 0 V; $V_{CC}$ = 3.3 V; EN = Low | | 7 | 10 | | 10 | pF |
| | | $V_I$ = 3 V or 0 V; $V_{CC}$ = 0 V | | 7 | 10 | | 10 | |
| **INPUT EN** | | | | | | | | |
| $V_{IH}$ | High–Level Input Voltage | | 0.7 x $V_{CC(B)}$ | | | 0.7 x $V_{CC(B)}$ | | V |
| $V_{IL}$ | Low–Level Input Voltage | | | | 0.3 x $V_{CC(B)}$ | | 0.3 x $V_{CC(B)}$ | V |
| $I_{LI}$ | Input Leakage Current | | | | ±1 | | ±1 | μA |
| $I_{IL(EN)}$ | LOW–Level Input Current | $V_I$ = 0.2 V, EN; $V_{CC(B)}$ = 2.2 V | –18 | –7 | –4 | –18 | –4 | μA |
| $C_I$ | Input Capacitance | $V_I = V_{CC(B)}$ | | 6 | 7 | | 7 | pF |

7. $V_{CC(A)}$ may be as high as 5.5 V for overvoltage tolerance but 0.4 $V_{CC(A)}$ + 0.8 V ≤ $V_{CC(B)}$ for the channels to be enabled and functional normally.
8. Pull–up should result in $I_{OL} \geq 150$ μA.
9. Guaranteed by design and characterization.
10. $V_{IL}$ for port A with envelope noise must be below 0.3 $V_{CC(A)}$ for stable performance.
11. When $V_{CC(A)}$ is less than 1 V, care is required to make certain that the system ground offset and noise are minimized such that there is reasonable difference between the $V_{IL}$ present at the PCA9617A A–side input and the 0.25 $V_{CC(A)}$ input threshold.
12. Power supply decoupling capacitors need to be present for both $V_{CC(A)}$ and $V_{CC(B)}$ and the 0.1 μF decoupling for $V_{CC(B)}$ needs to be located near the $V_{CC(B)}$ pin.

## TYPICAL CHARACTERISTICS

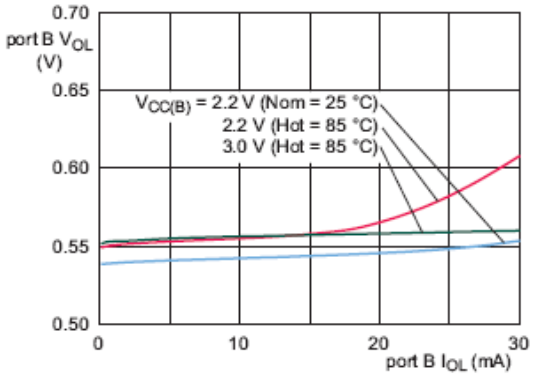



**Figure 9. Port B $V_{OL}$ vs $I_{OL}$**

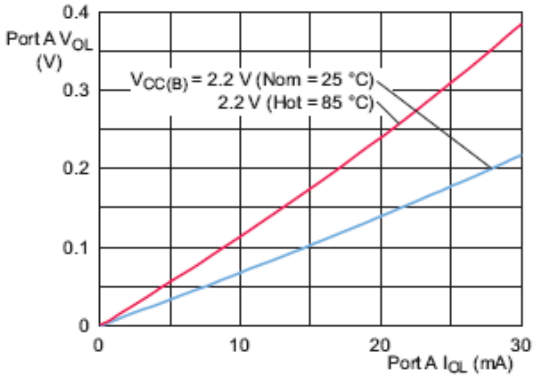
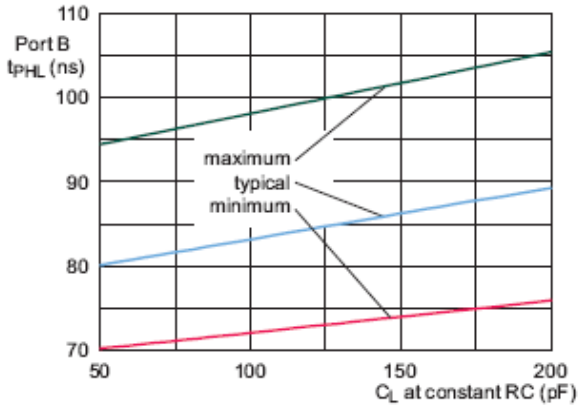



**Figure 10. Port A $V_{OL}$ vs $I_{OL}$**




RC = 67.5 ns, $V_{CC(A)}$ = 0.95 V, $V_{CC(B)}$ = 2.5 V, and $T_A$ = 25°C.

**Figure 11. Nominal Port B $t_{PHL}$ with Load Capacitance at Constant RC**

**AC CHARACTERISTICS** $V_{CC(A)}$ = 0.8 V to 5.5 V (Note 13); $V_{CC(B)}$ = 2.2 V to 5.5 V; GND = 0 V; $T_A$ = –40 °C to +85 °C; unless otherwise specified. (Notes 14 and 15)

| Symbol | Parameter | Conditions | $T_A$ = –40°C to +85°C | | | $T_A$ = –55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ (Note 16) | Max | Min | Max | |
| $t_{PLH}$ (Note 16) | LOW–to–HIGH Propagation Delay | Port B to Port A; Figure 16 | –20 | –65 | –103 | –20 | –103 | ns |
| $t_{PLH2}$ (Note 17) | LOW–to–HIGH Propagation Delay 2 | Port B to Port A; Figure 16 | 67 | 94 | 150 | 67 | 150 | ns |
| $t_{PHL}$ | HIGH–to–LOW Propagation Delay | B–Side to A–Side; Figure 14 | 46 | 4 | 152 | 46 | 152 | ns |
| $t_{TLH}$ (Note 18) | LOW–to–HIGH Output Transition Time | Port A; Figure 14 | | 88 | | | | ns |
| $SR_f$ | Falling Slew Rate | Port A; 0.7 $V_{CC(A)}$ to 0.3 $V_{CC(A)}$ | 0.022 | 0.037 | 0.13 | 0.022 | 0.14 | V/ns |
| $t_{PLH}$ (Note 19) | LOW–to–HIGH Propagation Delay | Port A to Port B; Figure 15 | 40 | 60 | 115 | 40 | 120 | ns |
| $t_{PHL}$ (Note 19) | HIGH–to–LOW Propagation Delay | Port A to Port B; Figure 15 | 35 | 80 | 173 | 35 | 173 | ns |
| $t_{TLH}$ (Note 18) | LOW–to–HIGH Output Transition Time | Port B; Figure 15 | | 80 | | | | ns |
| $SR_f$ | Falling Slew Rate | Port B; 0.7 $V_{CC(B)}$ to 0.3$V_{CC(B)}$ | 0.011 | 0.056 | 0.17 | 0.011 | 0.17 | V/ns |
| $t_{en}$ (Note 20) | Enable Time | Quiescent – 0.3 V; EN HIGH to enable; Figure TBD | | | 100 | | 100 | ns |
| $t_{dis}$ (Note 20) | Disable Time | Quiescent + 0.3 V; EN LOW to disable; Figure TBD | | | 100 | | 100 | ns |

13. 0.4 $V_{CC(A)}$ + 0.8 V ≤ $V_{CC(B)}$ for the channels to be enabled and functional normally.
14. Times are specified with loads of 1.35 kΩ pull–up resistance and 50 pF load capacitance on port A and port B, and a falling edge slew rate of 0.05 V/ns input signals.
15. Pull–up voltages are $V_{CC(A)}$ on the A side and $V_{CC(B)}$ on the B side.
16. Typical values were measured with $V_{CC(A)}$ = 0.95 V, $V_{CC(B)}$ = 2.5 V at $T_A$ = 25°C, unless otherwise noted.
17. The $t_{PLH2}$ delay data from port B to port A is measured at 0.45 V on port B to 0.5 $V_{CC(A)}$ on port A.
18. The $t_{TLH}$ of the bus is determined by the pull–up resistance (1.35 kΩ) and the total capacitance (50 pF).
19. The proportional delay data from port A to port B is measured at 0.5 $V_{CC(A)}$ on port A to 0.5 $V_{CC(B)}$ on port B.
20. The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

## AC WAVEFORMS

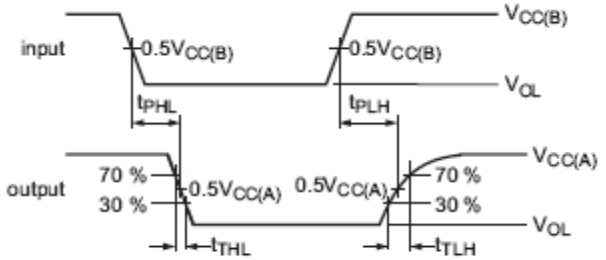



**Figure 12. Propagation Delay and Transition Times; Port B to Port A**

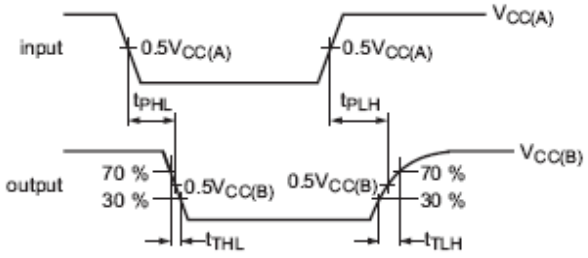



**Figure 13. Propagation Delay and Transition Times; Port A to Port B**

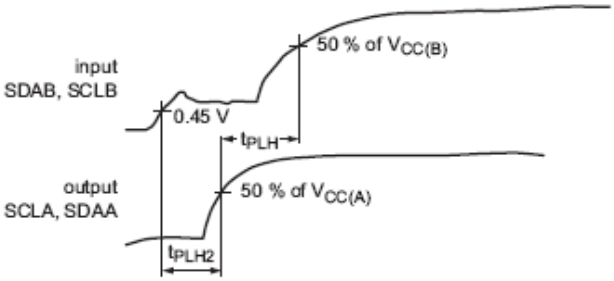



**Figure 14. Propagation Delay**

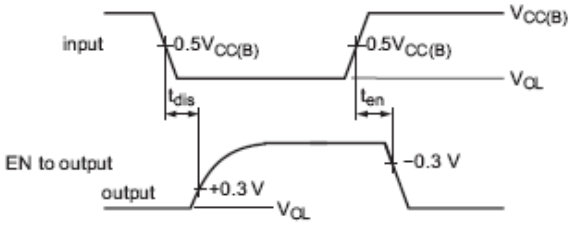
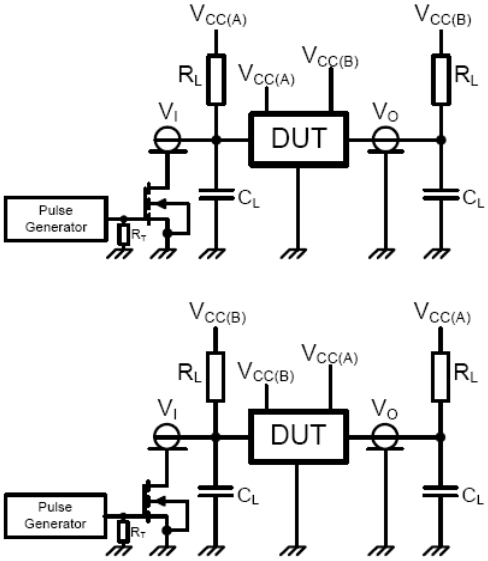



**Figure 15. Enable and Disable Times**

## TEST SETUP




$R_L$ = load resistor; 1.35 kΩ on port A and port B.
$C_L$ = load capacitance includes jig and probe capacitance; 50 pF
$R_T$ = termination resistance should be equal to $Z_O$ of pulse generators

**Figure 16. Test Circuit for Open−Drain Outputs**

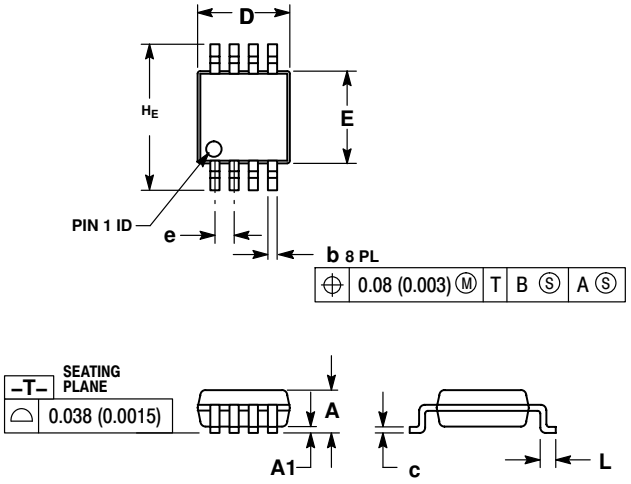
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| PCA9617ADMR2G | Micro−8<br>(Pb−Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

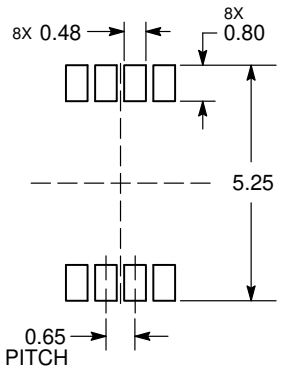
**Micro8™**
CASE 846A–02
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A–01 OBSOLETE, NEW STANDARD 846A–02.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | –– | –– | 1.10 | –– | –– | 0.043 |
| A1 | 0.05 | 0.08 | 0.15 | 0.002 | 0.003 | 0.006 |
| b | 0.25 | 0.33 | 0.40 | 0.010 | 0.013 | 0.016 |
| c | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.40 | 0.55 | 0.70 | 0.016 | 0.021 | 0.028 |
| $H_E$ | 4.75 | 4.90 | 5.05 | 0.187 | 0.193 | 0.199 |

## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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