



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





PCA9617A

Level translating Fm+ I²C-bus repeater

Rev. 1 — 20 March 2013

Product data sheet

1. General description

The PCA9617A is a CMOS integrated circuit that provides level shifting between low voltage (0.8 V to 5.5 V) and higher voltage (2.2 V to 5.5 V) Fast-mode Plus (Fm+) I²C-bus or SMBus applications. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 540 pF at 1 MHz or up to 4000 pF at lower speeds. Using the PCA9617A enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high-impedance when the PCA9617A is unpowered.

The 2.2 V to 5.5 V bus port B drivers have the static level offset, while the adjustable voltage bus port A drivers eliminate the static offset voltage. This results in a LOW on the port B translating into a nearly 0 V LOW on the port A which accommodates the smaller voltage swings of lower voltage logic.

The static offset design of the port B PCA9617A I/O drivers prevents them from being connected to the static or incremented offset of other bus buffers. Port A of two or more PCA9617As can be connected together, however, to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or incremented offset outputs. Multiple PCA9617As can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider.

The PCA9617A drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.2 V. The EN pin is referenced to $V_{CC(B)}$ and can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the port B internal buffer LOW is set for approximately 0.55 V, while the input threshold of the internal buffer is set about 90 mV lower (0.45 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a latching condition from occurring. The output pull-down on port A drives a hard LOW and the input level is set at $0.35V_{CC(A)}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.8 V.

2. Features and benefits

- 2 channel, bidirectional buffer isolates capacitance and allows 540 pF on either side of the device at 1 MHz and up to 4000 pF at lower speeds
- Voltage level translation from 0.8 V to 5.5 V and from 2.2 V to 5.5 V
- Footprint and functional replacement for PCA9517A at Fast-mode speeds
- Port A operating supply voltage range of 0.8 V to 5.5 V with normal levels



- Port B operating supply voltage range of 2.2 V to 5.5 V with static offset level
- 5 V tolerant I²C-bus and enable pins
- 0 Hz to 1000 kHz clock frequency (the maximum system operating frequency may be less than 1000 kHz because of the delays added by the repeater)
- Active HIGH repeater enable input referenced to V_{CC(B)}
- Open-drain input/outputs
- Latching free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode, Fast-mode and Fast-mode Plus I²C-bus devices, SMBus (standard and high power mode), PMBus and multiple masters
- Powered-off high-impedance I²C-bus pins
- ESD protection exceeds 5500 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8 and HWSO8

3. Ordering information

Table 1. Ordering information

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$.

Type number	Topside mark	Package		
		Name	Description	Version
PCA9617ADP	P617A	TSSOP8 ^[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9617ATP	P7A	HWSO8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm	SOT1069-2

[1] Also known as MSOP8.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9617ADP	PCA9617ADPJ	TSSOP8	Reel 13" Q1/T1 *standard mark SMD	2500	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$
PCA9617ATP	PCA9617ATPZ	HWSO8	Reel 7" Q2/T3 *standard mark	4000	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

4. Functional diagram

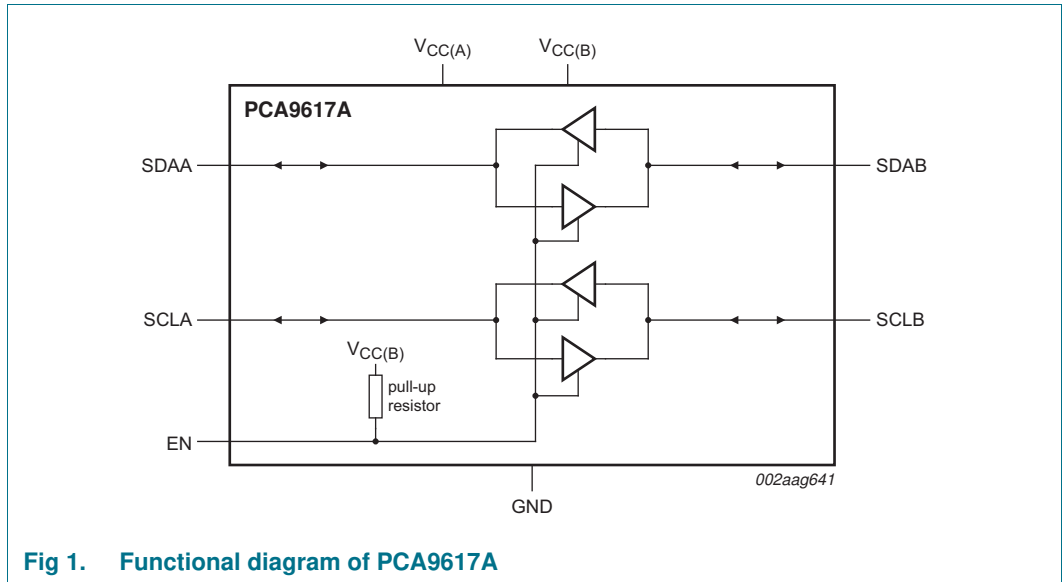


Fig 1. Functional diagram of PCA9617A

5. Pinning information

5.1 Pinning

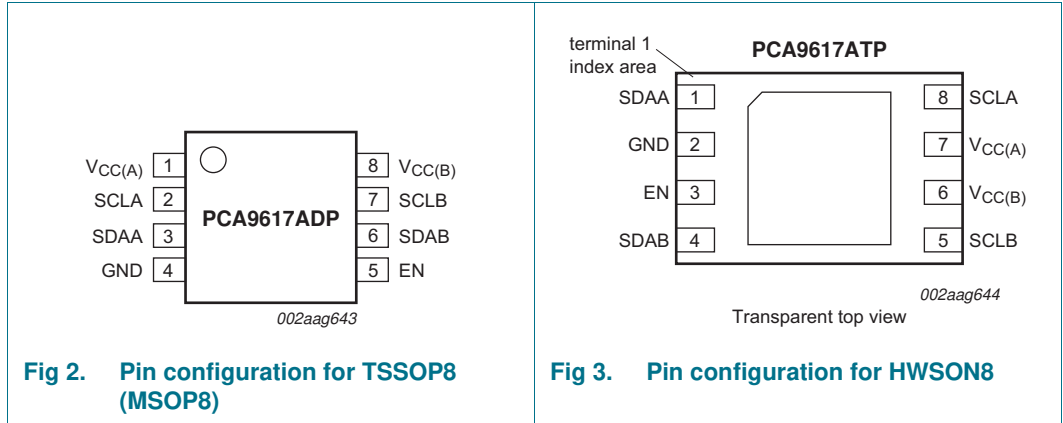


Fig 2. Pin configuration for TSSOP8 (MSOP8)

Fig 3. Pin configuration for HWSO8

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP8	HWSO8	
V _{CC(A)}	1	7	port A supply voltage (0.8 V to 5.5 V)
SCLA	2	8	serial clock port A bus
SDAA	3	1	serial data port A bus
GND	4	2 ^[1]	supply ground (0 V)
EN	5	3	active HIGH repeater enable input
SDAB	6	4	serial data port B bus
SCLB	7	5	serial clock port B bus
V _{CC(B)}	8	6	port B supply voltage (2.2 V to 5.5 V)

[1] HWSO8 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6. Functional description

Refer to [Figure 1 “Functional diagram of PCA9617A”](#).

The PCA9617A enables I²C-bus or SMBus translation down to $V_{CC(A)}$ as low as 0.8 V without degradation of system performance. The PCA9617A contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.8 V) and a 2.5 V, 3.3 V or 5 V I²C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered ($V_{CC(B)}$ and/or $V_{CC(A)} = 0$ V). The PCA9617A includes a power-up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.2 V and until after the internal reference circuits have settled ~ 400 μ s, and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port A (below $0.3V_{CC(A)}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.55 V. When port A rises above $0.3V_{CC(A)}$, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4 V, the port A driver is turned on and port A pulls down to ~ 0 V. The port A pull-down is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage goes below 0.4 V, the port B pull-down driver is enabled and port B will only be able to rise to 0.55 V until port A rises above $0.3V_{CC(A)}$, then port B will continue to rise being pulled up by the external pull-up resistor. The $V_{CC(A)}$ is only used to provide the $0.35V_{CC(A)}$ reference to the port A input comparators and for the power good detect circuit. The PCA9617A includes a $V_{CC(A)}$ overvoltage disable that turns the channel off if $0.4V_{CC(A)} + 0.8$ V > $V_{CC(B)}$. The PCA9617A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

6.1 Enable

The EN pin is active HIGH with thresholds referenced to $V_{CC(B)}$ and an internal pull-up to $V_{CC(B)}$ that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled. The enable does not switch the internal reference circuits so the ~ 400 μ s delay is only seen when $V_{CC(B)}$ comes up.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

6.2 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I²C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 30 mA at 5 V drive strength, then lower value pull-up resistors can be used. The

B-side RC should not be less than 67.5 ns because shorter RCs increase the turnaround bounce when the B-side transitions from being externally driven to pulled down by its offset buffer.

Please see Application Note AN255, “I²C/SMBus Repeaters, Hubs and Expanders” for additional information on sizing resistors and precautions when using more than one PCA9617A in a system or using the PCA9617A in conjunction with other bus buffers.

7. Application design-in information

A typical application is shown in Figure 4. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 1.2 V bus. Both buses run at 1000 kHz. Master devices can be placed on either bus.

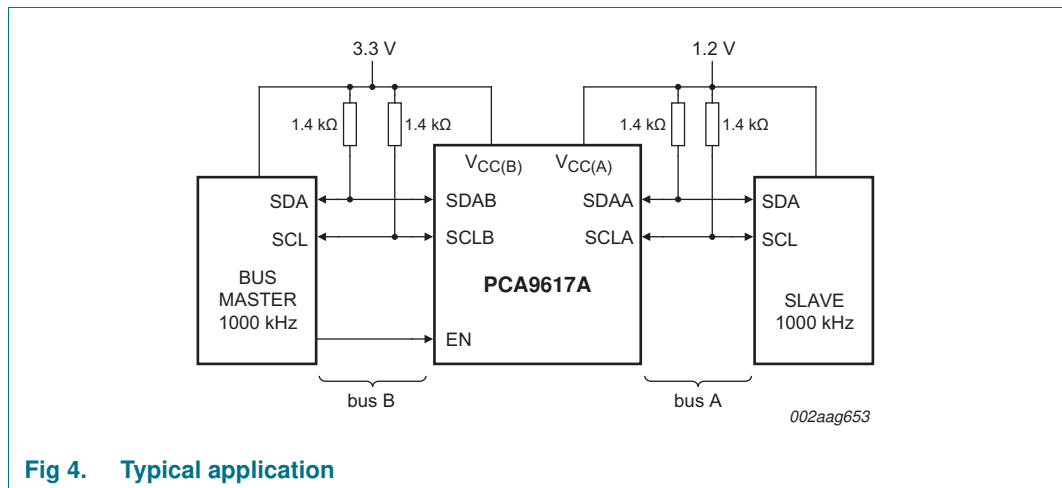


Fig 4. Typical application

The PCA9617A is 5 V tolerant, so it does not require any additional circuitry to translate between 0.8 V to 5.5 V bus voltages and 2.2 V to 5.5 V bus voltages.

When port A of the PCA9617A is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9617A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 8 and Figure 9. If the bus master in Figure 4 were to write to the slave through the PCA9617A, waveforms shown in Figure 8 would be observed on the A bus. This looks like a normal I²C-bus transmission except that the HIGH level may be as low as 0.8 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

The internal comparator requires that $0.4 \times V_{CC(A)}$ be less than or equal to $V_{CC(B)} - 0.8 V$ for the device to operate. Since A port is 5 V tolerant, the $V_{CC(A)}$ can be lowered to support device spectrum while still supporting 5 V signals on the A port.

On the B bus side of the PCA9617A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9617A. After the eighth clock pulse, the data line will be pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9617A for a short delay while the A bus side rises above $0.3V_{CC(A)}$ then it continues

HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9617A (V_{IL}) be at or below 0.4 V to be recognized by the PCA9617A and then transmitted to the A bus side.

Multiple PCA9617A port A sides can be connected in a star configuration (Figure 5), allowing all nodes to communicate with each other.

Multiple PCA9617As can be connected in series (Figure 6) as long as port A is connected to port B. I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

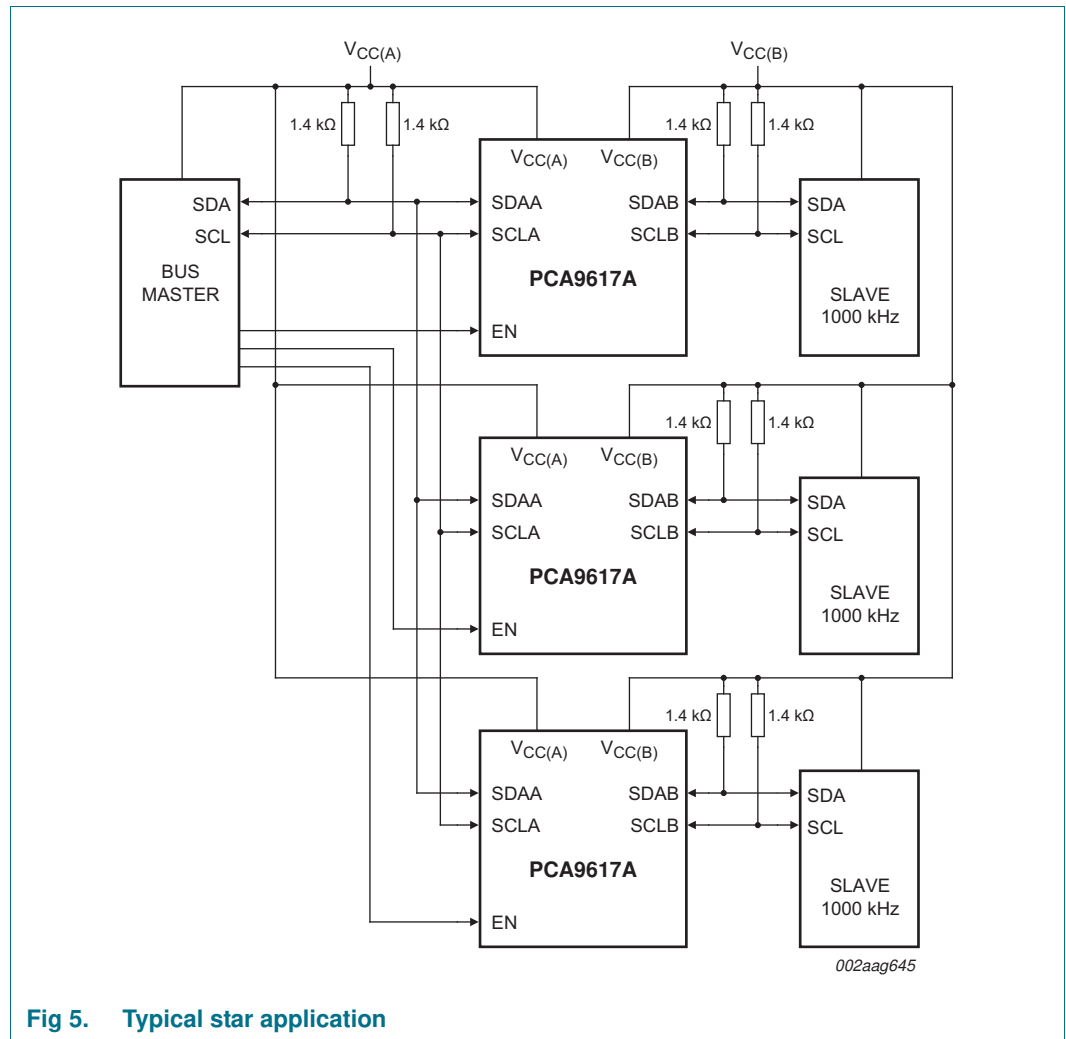
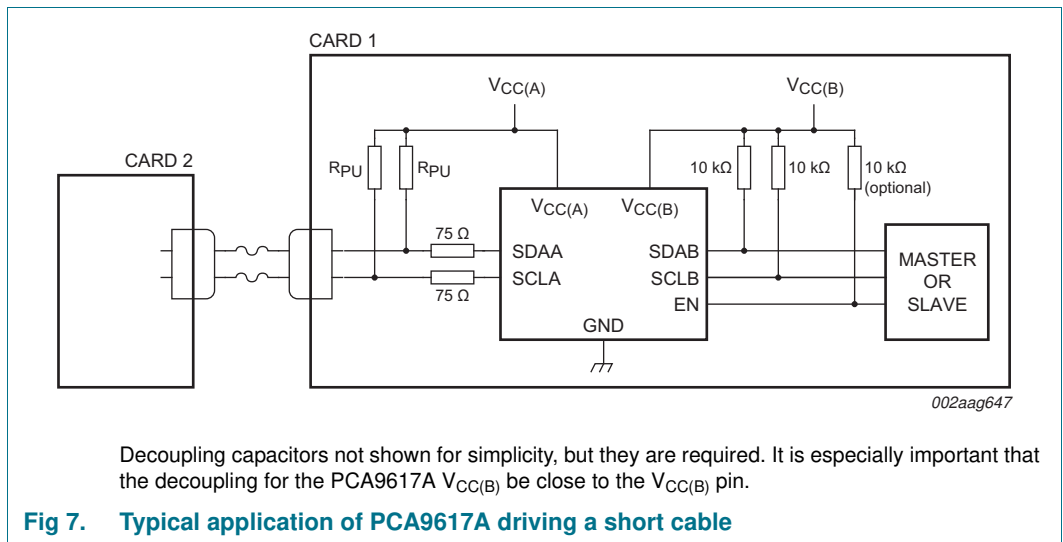
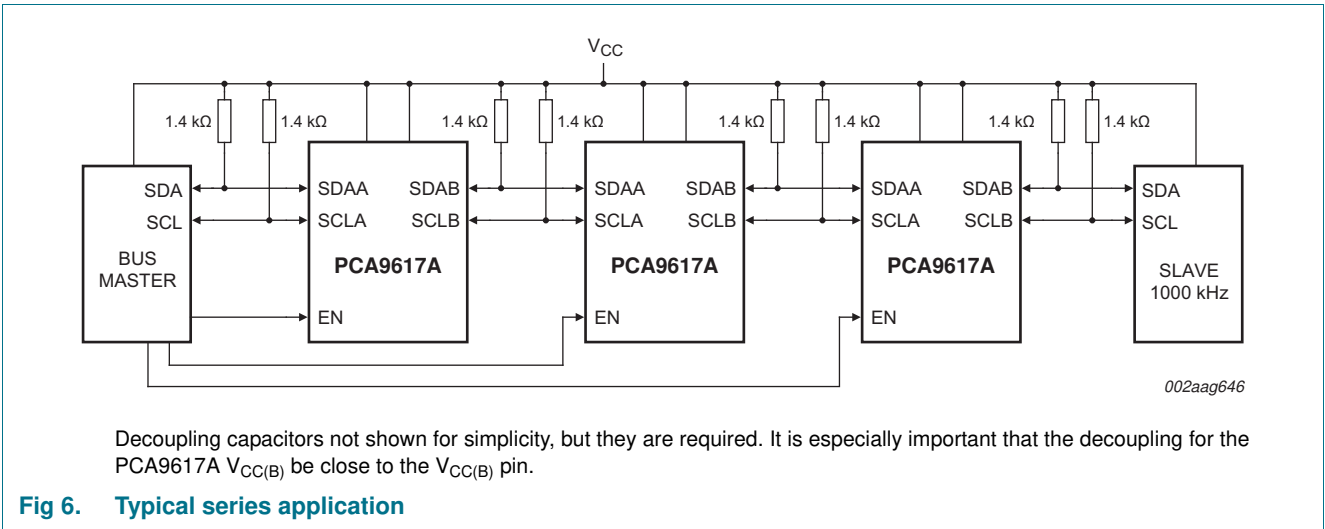


Fig 5. Typical star application



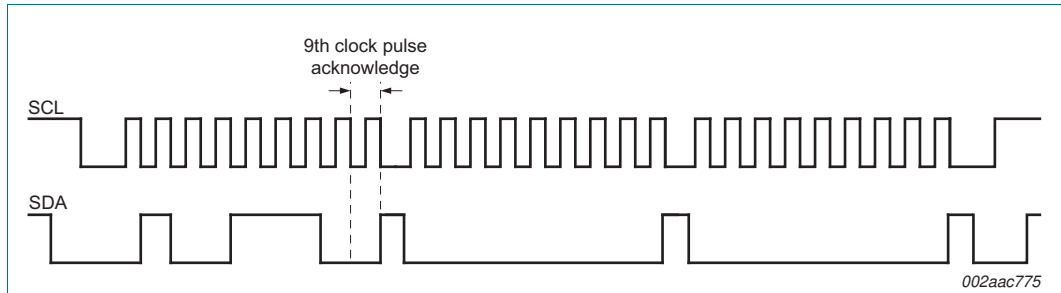


Fig 8. Bus A (0.8 V to 5.5 V bus) waveform

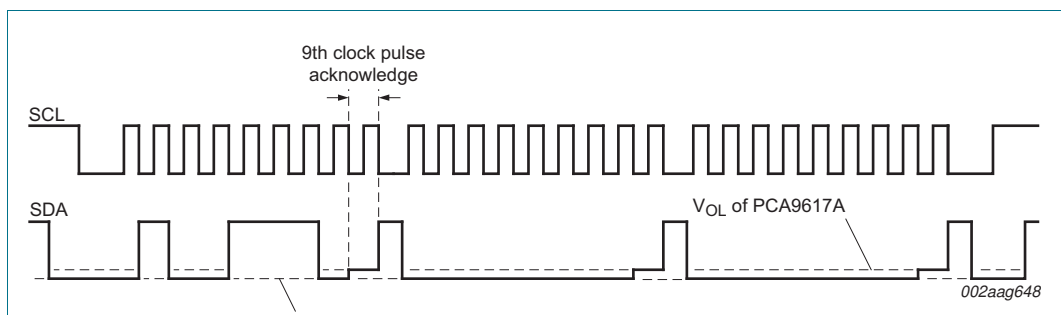


Fig 9. Bus B (2.2 V to 5.5 V) waveform

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(B)}	supply voltage port B		-0.5	+7	V
V _{CC(A)}	supply voltage port A	adjustable	-0.5	+7	V
V _{I/O}	voltage on an input/output pin	port A and port B; enable pin (EN)	-0.5	+7	V
I _{I/O}	input/output current	port A; port B	-	50	mA
I _I	input current	EN, V _{CC(A)} , V _{CC(B)} , GND	-	50	mA
P _{tot}	total power dissipation		-	100	mW
T _{stg}	storage temperature		-55	+125	°C
T _{amb}	ambient temperature	operating in free air	-40	+85	°C
T _j	junction temperature		-	+125	°C

9. Static characteristics

Table 5. Static characteristics

$V_{CC(A)} = 0.8\text{ V to }5.5\text{ V}$ ^[1]; $V_{CC(B)} = 2.2\text{ V to }5.5\text{ V}$; $GND = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified.
Typical values measured with $V_{CC(A)} = 0.95\text{ V}$ and $V_{CC(B)} = 2.5\text{ V}$ at 25 °C , unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{CC(B)}$	supply voltage port B		2.2	-	5.5	V
$V_{CC(A)}$	supply voltage port A		^[2] 0.8	-	5.5	V
$I_{CC(A)}$	supply current port A	$V_{CC(A)} = 0.95\text{ V}$	-	-	8	μA
		$V_{CC(A)} = 5.5\text{ V}$	-	-	50	μA
$I_{CH(B)}$	port B HIGH-level supply current	$V_{CC(B)} = 5.5\text{ V}$; $SDAn = SCLn = V_{CC(n)}$	-	1.5	2.5	mA
$I_{CL(B)}$	port B LOW-level supply current	$V_{CC(B)} = 5.5\text{ V}$; one SDA and one SCL = GND; other SDA and SCL open (with pull-up resistors)	-	1.7	2.9	mA
Input and output SDAB and SCLB						
V_{IH}	HIGH-level input voltage		$0.7V_{CC(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage		-0.5	-	+0.4	V
V_{IK}	input clamping voltage	$I_I = -18\text{ mA}$	-1.2	-	-0.3	V
I_{LI}	input leakage current	$V_I = 5.5\text{ V}$	-	-	± 1	μA
I_{IL}	LOW-level input current	SDA, SCL; $V_I = 0.2\text{ V}$	-	-	10	μA
V_{OL}	LOW-level output voltage	$I_{OL} = 150\text{ }\mu\text{A}$ at $V_{CC(B)} = 2.2\text{ V}$	^[3] 0.47	-	-	V
		$I_{OL} = 13\text{ mA}$ at $V_{CC(B)} = 2.2\text{ V}$	^[4] -	0.54	0.60	V
$V_{OL}-V_{IL}$	difference between LOW-level output and LOW-level input voltage	V_{OL} at $I_{OL} = 1\text{ mA}$; guaranteed by design	60	90	160	mV
C_{io}	input/output capacitance	$V_I = 3\text{ V}$ or 0 V ; $V_{CC(B)} = 3.3\text{ V}$; $EN = \text{LOW}$	-	7	10	pF
		$V_I = 3\text{ V}$ or 0 V ; $V_{CC} = 0\text{ V}$	-	7	10	pF
Input and output SDAA and SCLA						
V_{IH}	HIGH-level input voltage		$0.7V_{CC(A)}$	-	5.5	V
V_{IL}	LOW-level input voltage		^[5] -0.5	-	$+0.25V_{CC(A)}$ ^[6]	V
V_{IK}	input clamping voltage	$I_I = -18\text{ mA}$	-1.2	-	-0.3	V
I_{LI}	input leakage current	$V_I = 5.5\text{ V}$	-	-	± 1	μA
I_{IL}	LOW-level input current	SDA, SCL; $V_I = 0.2\text{ V}$	-	-	10	μA
V_{OL}	LOW-level output voltage	$I_{OL} = 13\text{ mA}$; $V_{CC(B)} = 2.2\text{ V}$	-	0.1	0.2	V
C_{io}	input/output capacitance	$V_I = 3\text{ V}$ or 0 V ; $V_{CC} = 3.3\text{ V}$; $EN = \text{LOW}$	-	7	10	pF
		$V_I = 3\text{ V}$ or 0 V ; $V_{CC} = 0\text{ V}$	-	7	10	pF
Enable						
V_{IL}	LOW-level input voltage		-0.5	-	$+0.3V_{CC(B)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC(B)}$	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	$V_I = 0.2\text{ V}$, EN; $V_{CC(B)} = 2.2\text{ V}$	-18	-7	-4	μA

Table 5. Static characteristics ...continued

$V_{CC(A)} = 0.8\text{ V to }5.5\text{ V}$ [1]; $V_{CC(B)} = 2.2\text{ V to }5.5\text{ V}$; $GND = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified. Typical values measured with $V_{CC(A)} = 0.95\text{ V}$ and $V_{CC(B)} = 2.5\text{ V}$ at $25\text{ }^{\circ}\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current		-1	-	+1	μA
C_i	input capacitance	$V_I = V_{CC(B)}$	-	6	7	pF

- [1] $V_{CC(A)}$ may be as high as 5.5 V for overvoltage tolerance but $0.4V_{CC(A)} + 0.8\text{ V} \leq V_{CC(B)}$ for the channels to be enabled and functional normally.
- [2] For part to function, $0.4 \times V_{CC(A)}$ must be equal or less than $V_{CC(B)} - 0.8\text{ V}$. The voltage on the A port can still be up to 5.5 V without damage to the pins.
- [3] Pull-up should result in $I_{OL} \geq 150\text{ }\mu\text{A}$.
- [4] Guaranteed by design and characterization.
- [5] V_{IL} for port A with envelope noise must be below $0.3V_{CC(A)}$ for stable performance.
- [6] When $V_{CC(A)}$ is less than 1 V, care is required to make certain that the system ground offset and noise are minimized such that there is reasonable difference between the V_{IL} present at the PCA9617A A-side input and the $0.25V_{CC(A)}$ input threshold.
- [7] Power supply decoupling capacitors need to be present for both $V_{CC(A)}$ and $V_{CC(B)}$ and the $0.1\text{ }\mu\text{F}$ decoupling for $V_{CC(B)}$ needs to be located near the $V_{CC(B)}$ pin.

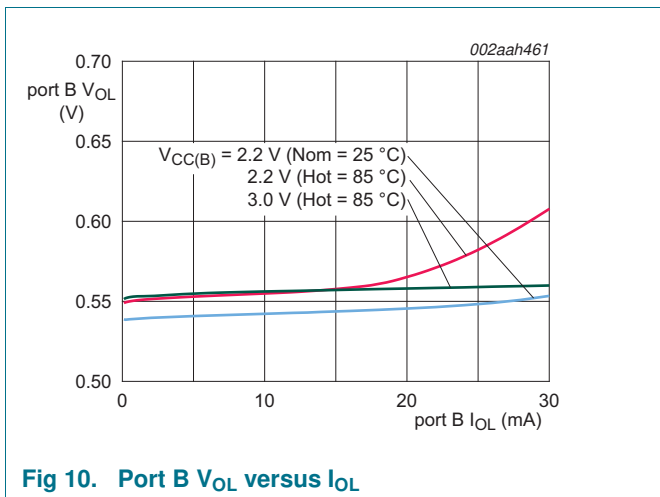


Fig 10. Port B V_{OL} versus I_{OL}

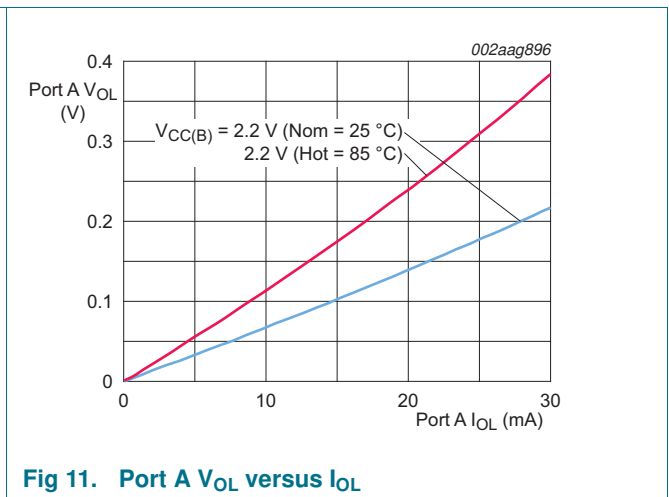
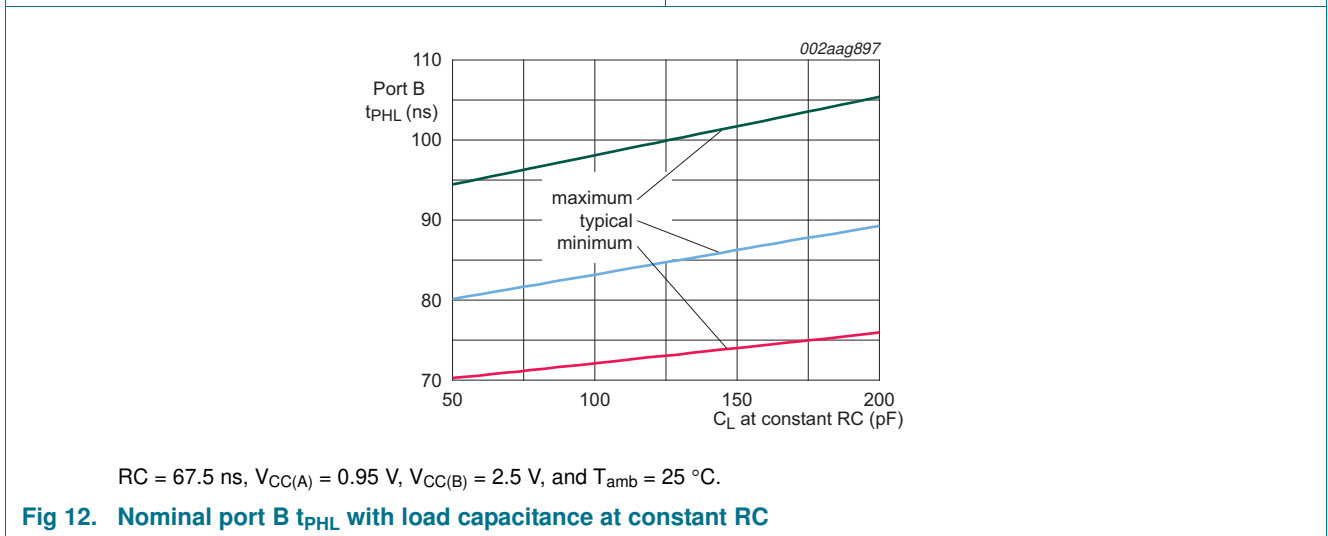


Fig 11. Port A V_{OL} versus I_{OL}



$RC = 67.5\text{ ns}$, $V_{CC(A)} = 0.95\text{ V}$, $V_{CC(B)} = 2.5\text{ V}$, and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig 12. Nominal port B t_{PHL} with load capacitance at constant RC

10. Dynamic characteristics

Table 6. Dynamic characteristics

$V_{CC(A)} = 0.8\text{ V to }5.5\text{ V}$ ^[1]; $V_{CC(B)} = 2.2\text{ V to }5.5\text{ V}$; $GND = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified.^{[2][3]}

Symbol	Parameter	Conditions	Min	Typ ^[4]	Max	Unit
t _{PLH}	LOW to HIGH propagation delay	port B to port A; Figure 15	-42	-65	-103	ns
t _{PLH2}	LOW to HIGH propagation delay 2	port B to port A; Figure 15	^[5] 67	94	130	ns
t _{PHL}	HIGH to LOW propagation delay	port B to port A; Figure 13	46	76	152	ns
t _{TLH}	LOW to HIGH output transition time	port A; Figure 13	^[6] -	60	-	ns
SR _f	falling slew rate	port A; 0.7V _{CC(A)} to 0.3V _{CC(A)}	0.022	0.037	0.11	V/ns
t _{PLH}	LOW to HIGH propagation delay	port A to port B; Figure 14	^[7] 40	60	102	ns
t _{PHL}	HIGH to LOW propagation delay	port A to port B; Figure 14	^[7] 63	80	173	ns
t _{TLH}	LOW to HIGH output transition time	port B; Figure 14	^[6] -	60	-	ns
SR _f	falling slew rate	port B; 0.7V _{CC(B)} to 0.3 V _{CC(B)}	0.029	0.056	0.09	V/ns
t _{en}	enable time	quiescent - 0.3 V; EN HIGH to enable; Figure 16	^[8] -	-	100	ns
t _{dis}	disable time	quiescent + 0.3 V; EN LOW to disable; Figure 16	^[8] -	-	100	ns

[1] $0.4V_{CC(A)} + 0.8\text{ V} \leq V_{CC(B)}$ for the channels to be enabled and function normally.

[2] Times are specified with loads of 1.35 kΩ pull-up resistance and 50 pF load capacitance on port A and port B, and a falling edge slew rate of 0.05 V/ns input signals.

[3] Pull-up voltages are V_{CC(A)} on port A and V_{CC(B)} on port B.

[4] Typical values were measured with V_{CC(A)} = 0.95 V, V_{CC(B)} = 2.5 V at T_{amb} = 25 °C, unless otherwise noted.

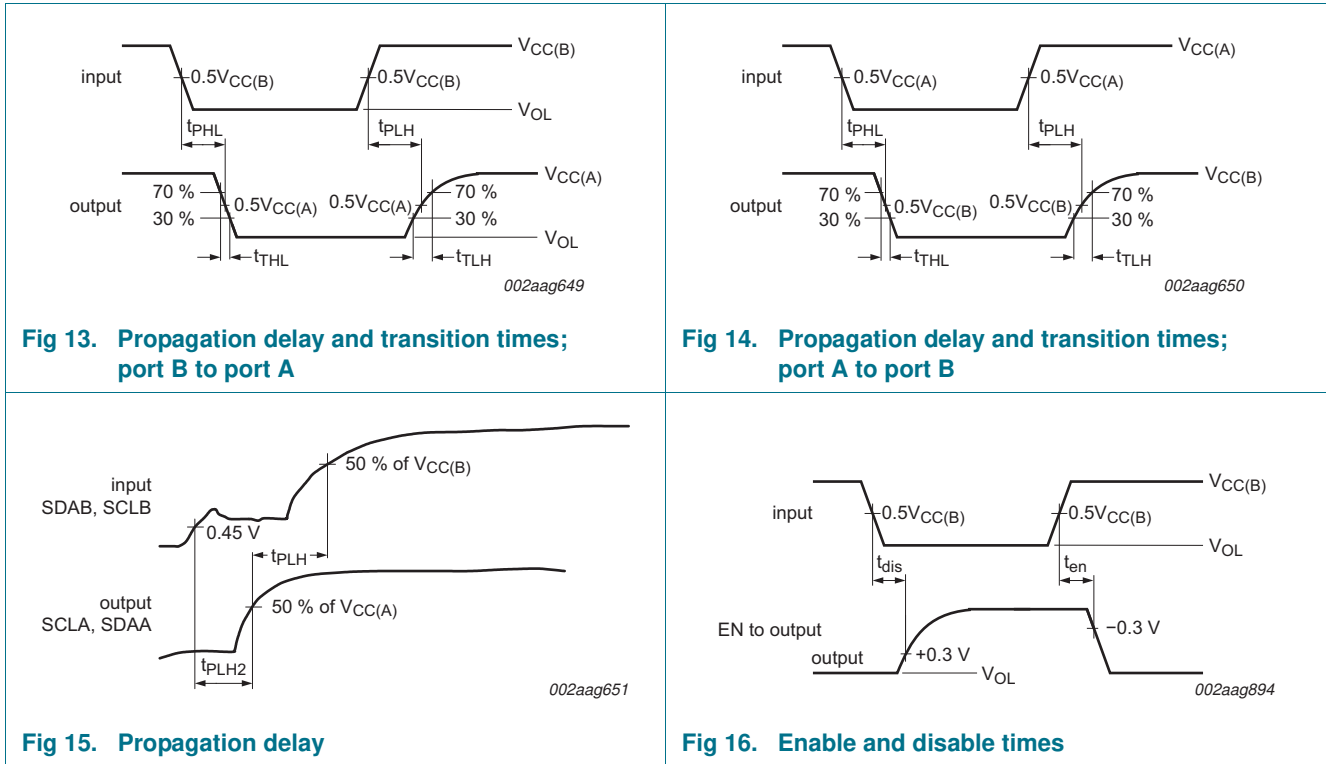
[5] The t_{PLH2} delay data from port B to port A is measured at 0.45 V on port B to 0.5V_{CC(A)} on port A.

[6] The t_{TLH} of the bus is determined by the pull-up resistance (1.35 kΩ) and the total capacitance (50 pF).

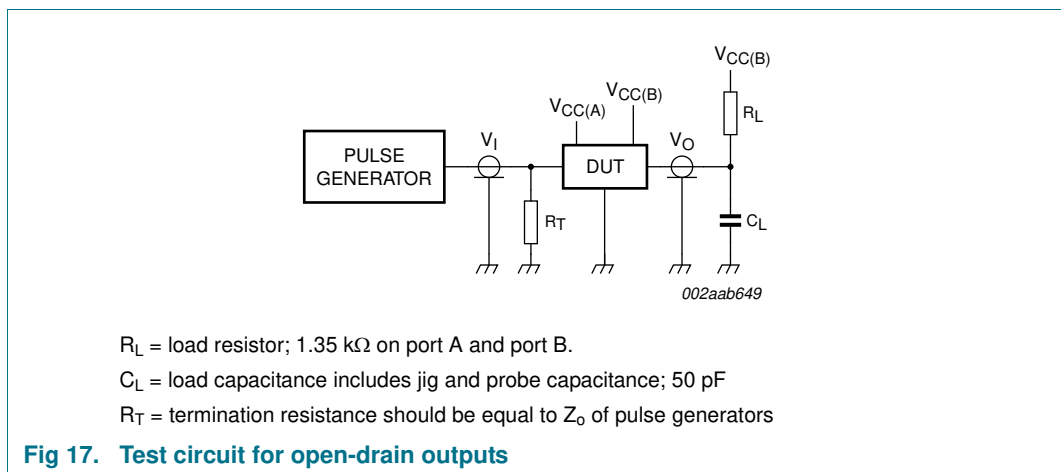
[7] The proportional delay data from port A to port B is measured at 0.5V_{CC(A)} on port A to 0.5V_{CC(B)} on port B.

[8] The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

10.1 AC waveforms



11. Test information



12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

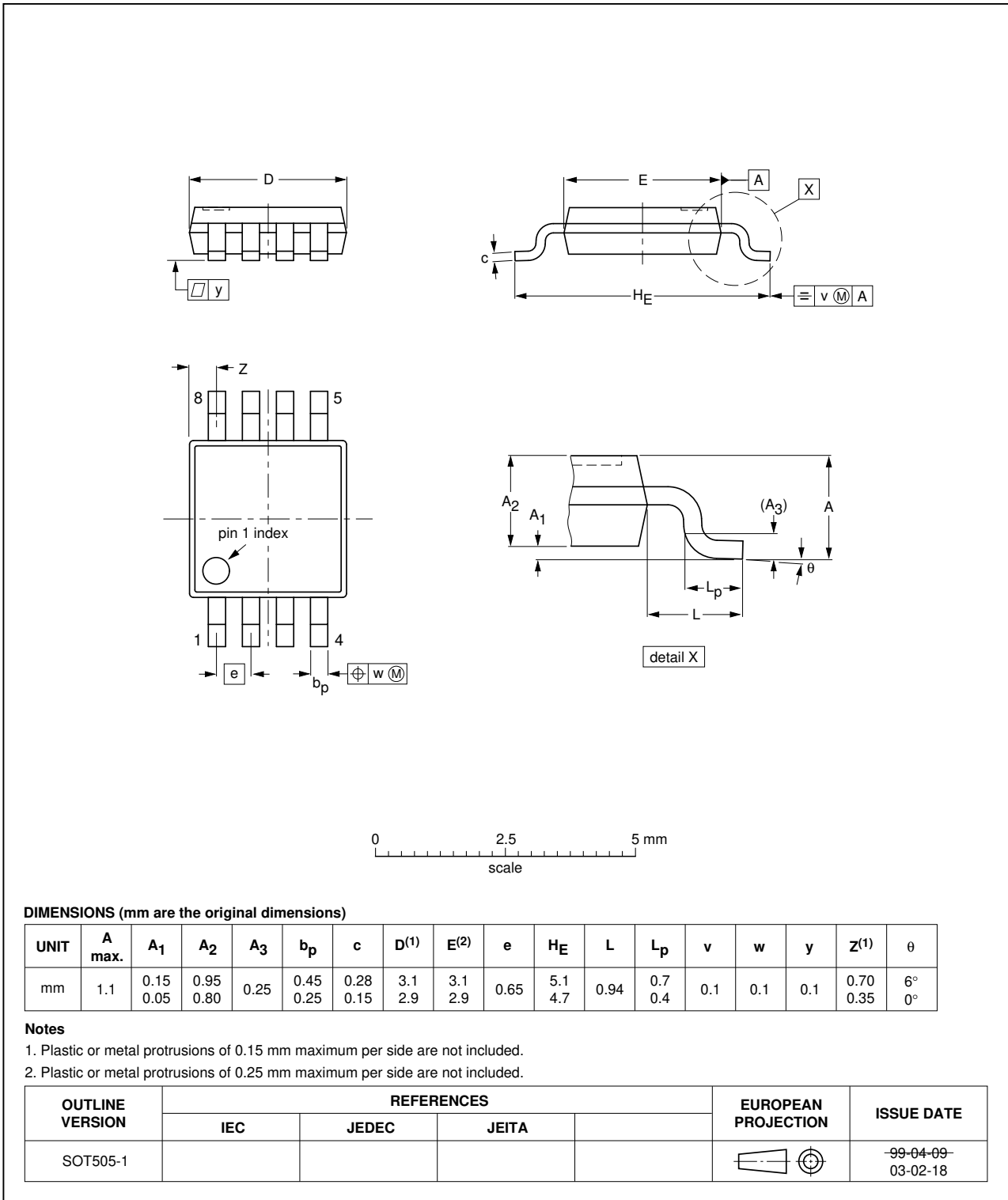


Fig 18. Package outline SOT505-1 (TSSOP8)

HWSON8: plastic thermal enhanced very very thin small outline package; no leads;
8 terminals; body 2 x 3 x 0.75 mm

SOT1069-2

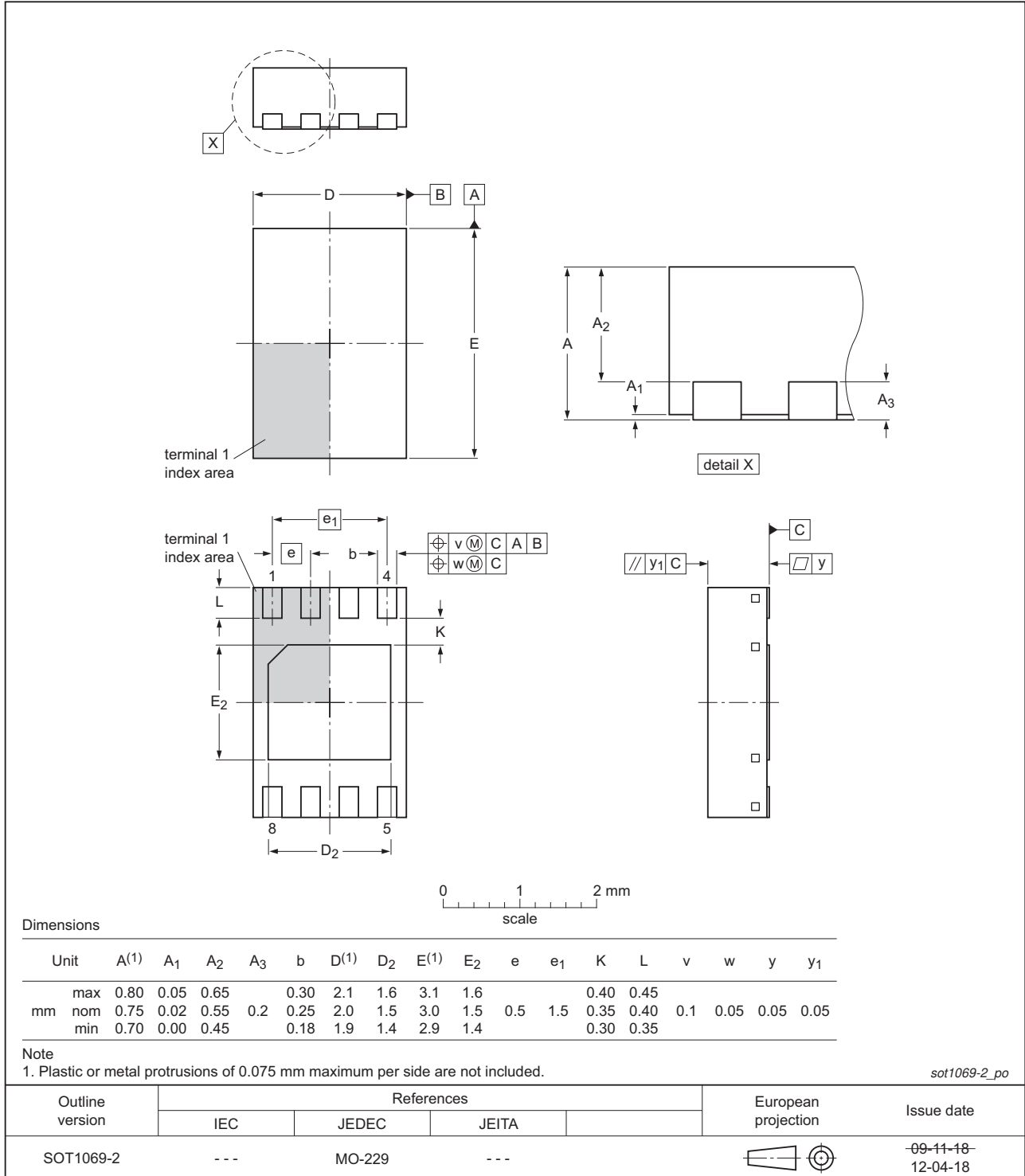


Fig 19. Package outline SOT1069-2 (HWSON8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 20](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 7](#) and [8](#)

Table 7. SnPb eutectic process (from J-STD-020D)

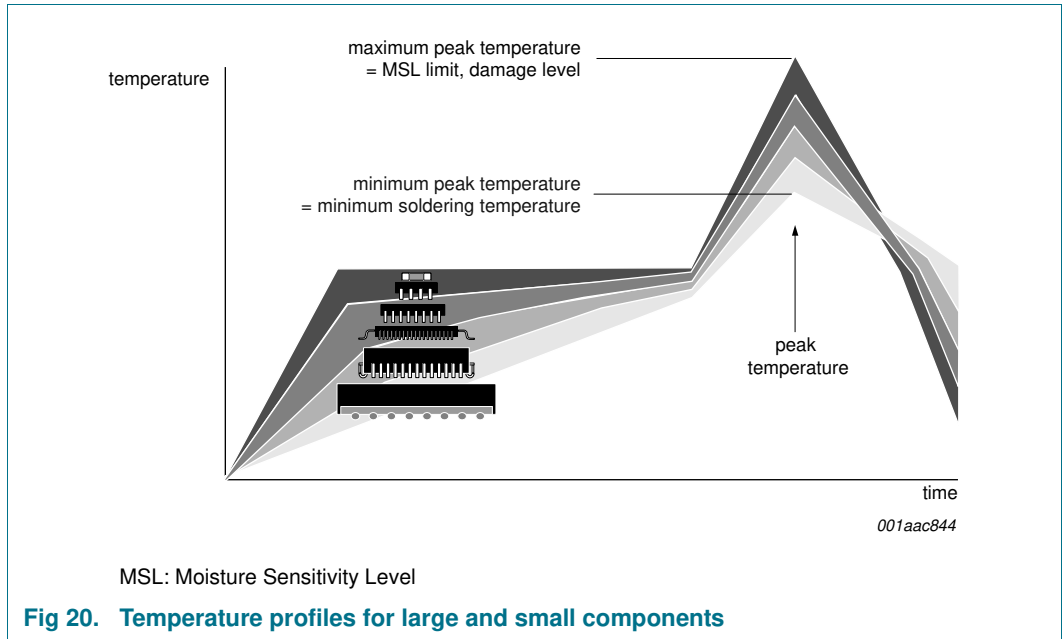
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

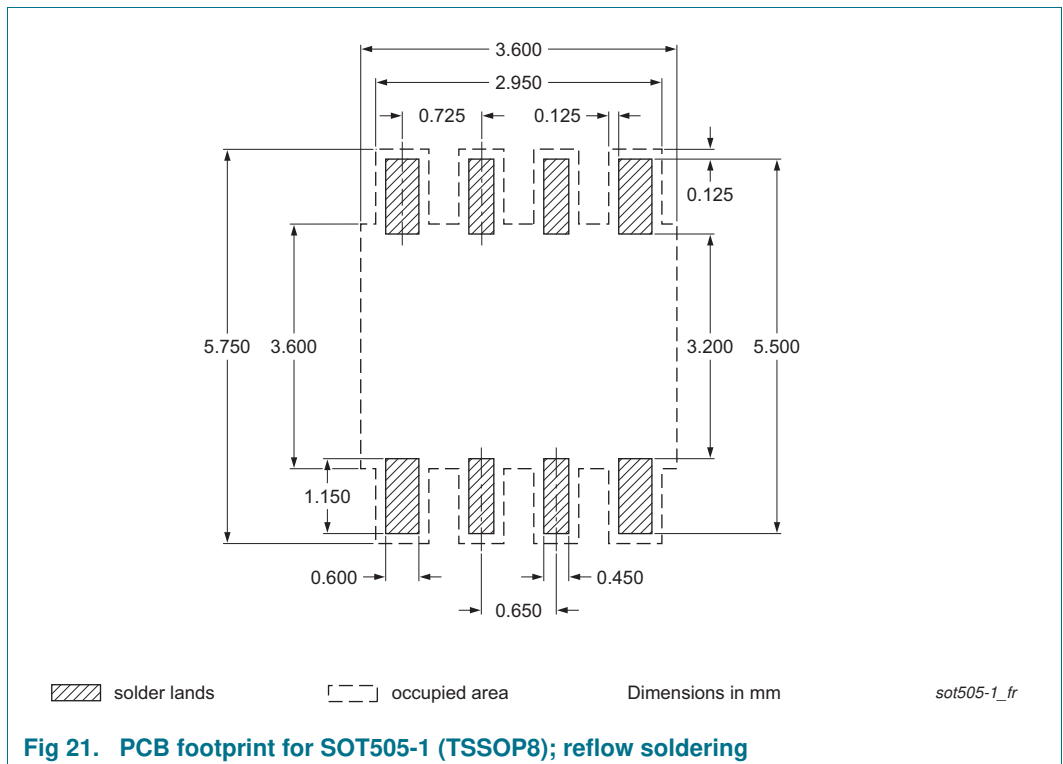
Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 20](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

14. Soldering: PCB footprints



Footprint information for reflow soldering of HWSO8 package

SOT1069-2

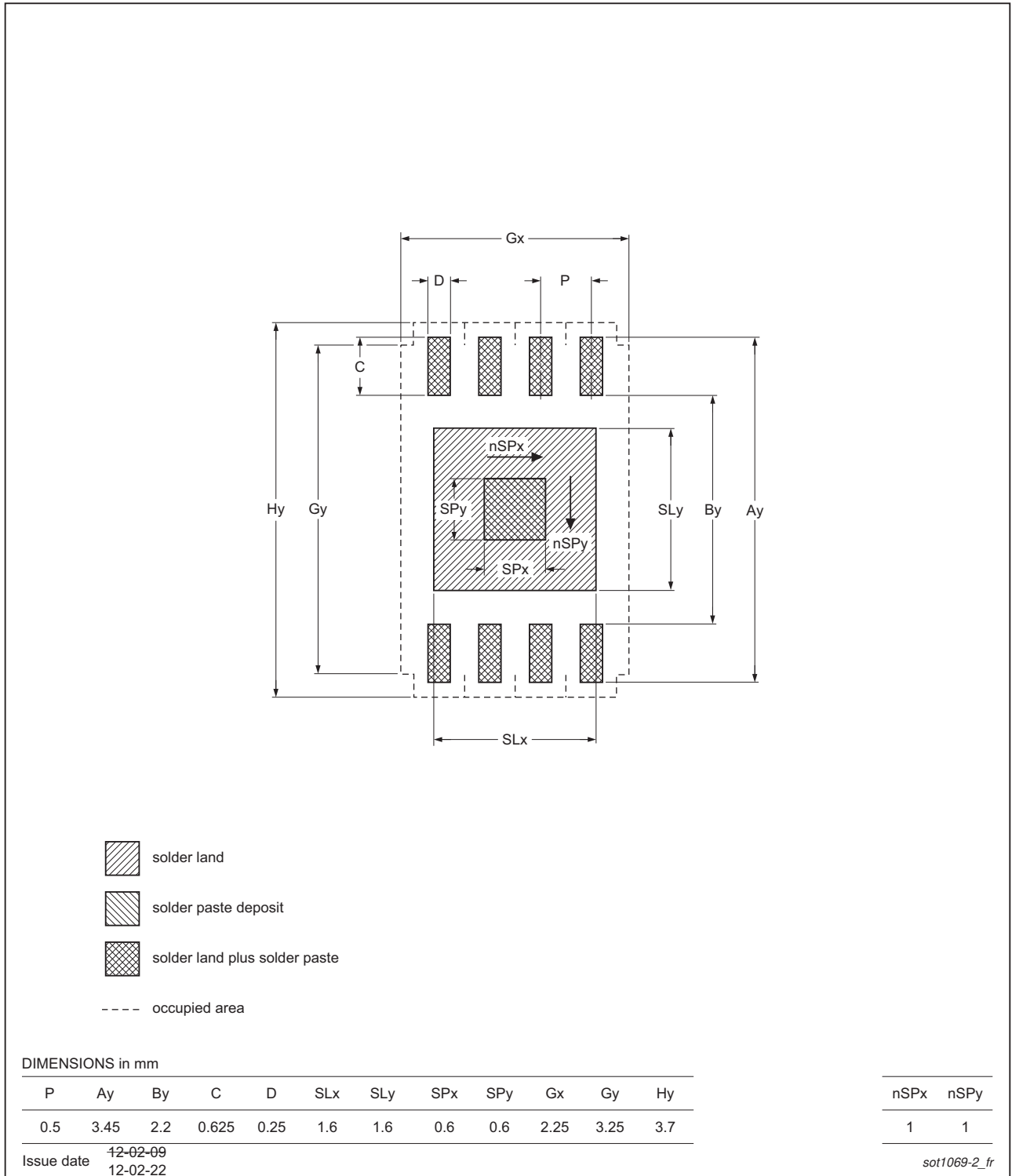


Fig 22. PCB footprint for SOT1069-2 (HWSO8); reflow soldering

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I ² C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
PMBus	Power Management Bus
RC	Resistor-Capacitor network
SMBus	System Management Bus

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9617A v.1	20130320	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

19. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
3.1	Ordering options	2
4	Functional diagram	3
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
6.1	Enable	5
6.2	I ² C-bus systems	5
7	Application design-in information	6
8	Limiting values	9
9	Static characteristics	10
10	Dynamic characteristics	12
10.1	AC waveforms	13
11	Test information	13
12	Package outline	14
13	Soldering of SMD packages	16
13.1	Introduction to soldering	16
13.2	Wave and reflow soldering	16
13.3	Wave soldering	16
13.4	Reflow soldering	17
14	Soldering: PCB footprints	18
15	Abbreviations	20
16	Revision history	20
17	Legal information	21
17.1	Data sheet status	21
17.2	Definitions	21
17.3	Disclaimers	21
17.4	Trademarks	22
18	Contact information	22
19	Contents	23

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 March 2013

Document identifier: PCA9617A