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PCA9620

60 x 8 LCD high-drive segment driver for automotive and industrial

Rev. 4 — 8 April 2015 Product data sheet

1. General description

The PCA9620 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to eight backplanes, 60 segments, and up to 480 elements. The PCA9620 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized using a display RAM with auto-incremented addressing and display memory switching. The PCA9620 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltages.

For a selection of NXP LCD segment drivers, see Table 44 on page 74.

2. Features and benefits

- AEC Q100 grade 2 compliant for automotive applications
- Low power consumption
- Extended operating temperature range from –40 °C to +105 °C
- 60 segments and 8 backplanes allowing to drive:
  - up to 60 7-segment alphanumeric characters
  - up to 30 14-segment alphanumeric characters
  - any graphics of up to 480 elements
- 480-bit RAM for display data storage
- Selectable backplane drive configuration: static, 2, 4, 6, or 8 backplane multiplexing
- Programmable internal charge pump for on-chip LCD voltage generation up to $3 \times V_{DD2}$
- 400 kHz I^2C-bus interface
- Selectable linear temperature compensation of V_{LCD}
- Selectable display bias configuration
- Wide range for digital and analog power supply: from 2.5 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 9.0 V for high threshold (automobile) twisted nematic LCDs
- Display memory bank switching in static, duplex, and quadruplex drive modes
- Programmable frame frequency in steps of 10 Hz in the range of 60 Hz to 300 Hz; factory calibrated with a tolerance of ±15 % covering the whole temperature and voltage range
- Selectable inversion scheme for LCD driving waveforms: frame or line inversion

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21 on page 76.

- Integrated temperature sensor with temperature readout
- On chip calibration of internal oscillator frequency and V_{LCD}

3. Applications

- Automotive
    - Instrument cluster
    - Car radio
    - Climate control units
- Industrial
    - Machine control systems
    - Measuring equipment
- Signage
    - Information boards
    - Panels

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA9620H	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
PCA9620U	bare die	80 bonding pads	PCA9620U

4.1 Ordering options

Table 2. Ordering options

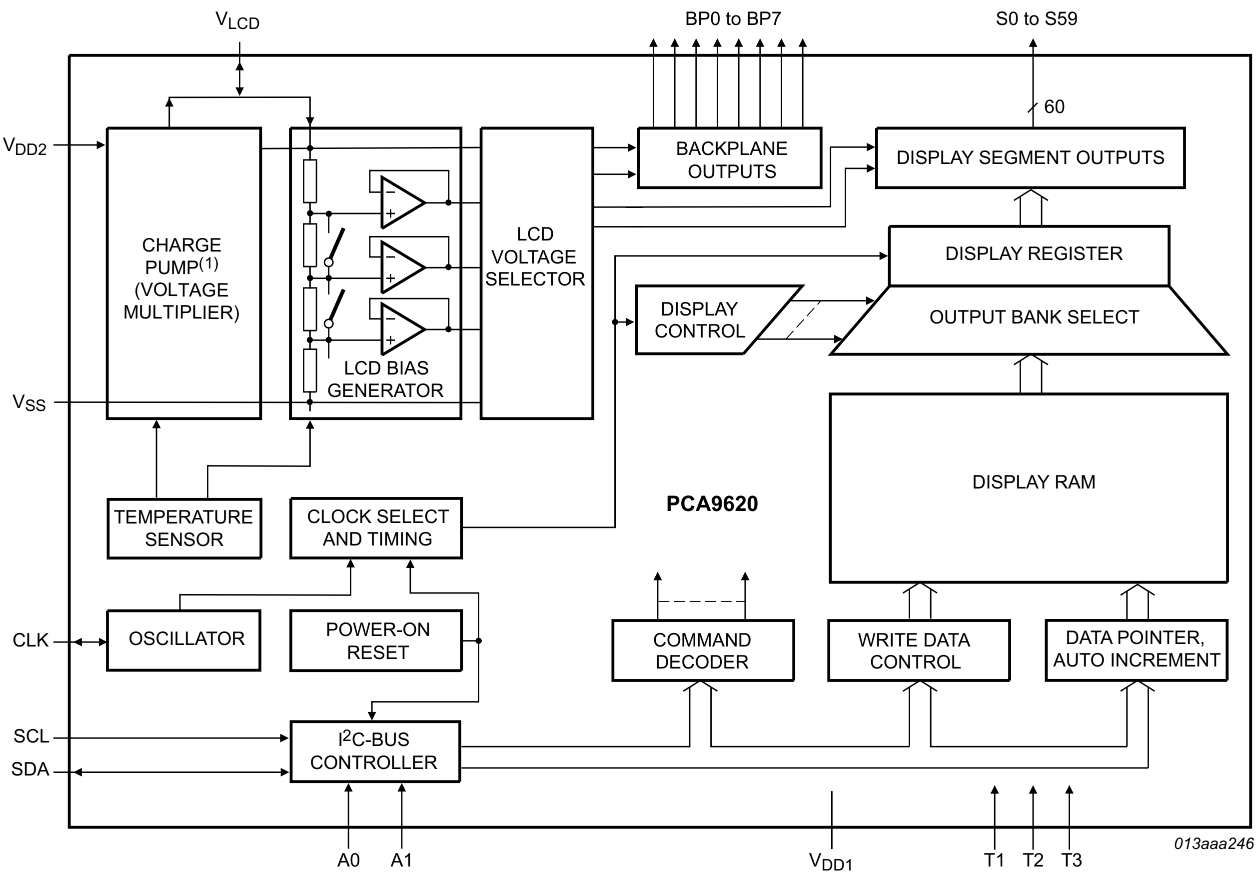
Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA9620H/Q900/1	935291899518	PCA9620H/Q900/1,51	1	tape and reel, 13 inch, dry pack
PCA9620U/5GA/Q1	935295801015	PCA9620U/5GA/Q1,01	1	wafer, unsawn

5. Marking

Table 3. Marking codes

Type number	Marking code
PCA9620H	PCA9620H/Q900
PCA9620U	PC9620-1

6. Block diagram

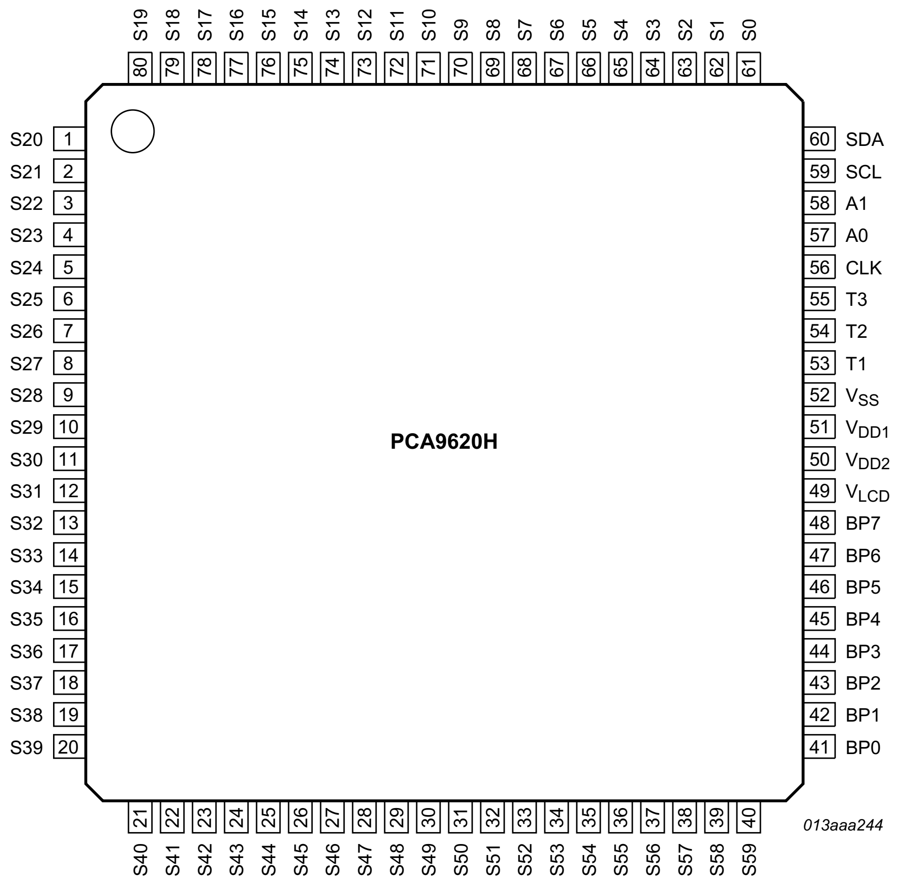


(1) The charge pump can generate a maximum output voltage of 3 × V_{DD2}.

Fig 1. Block diagram of PCA9620

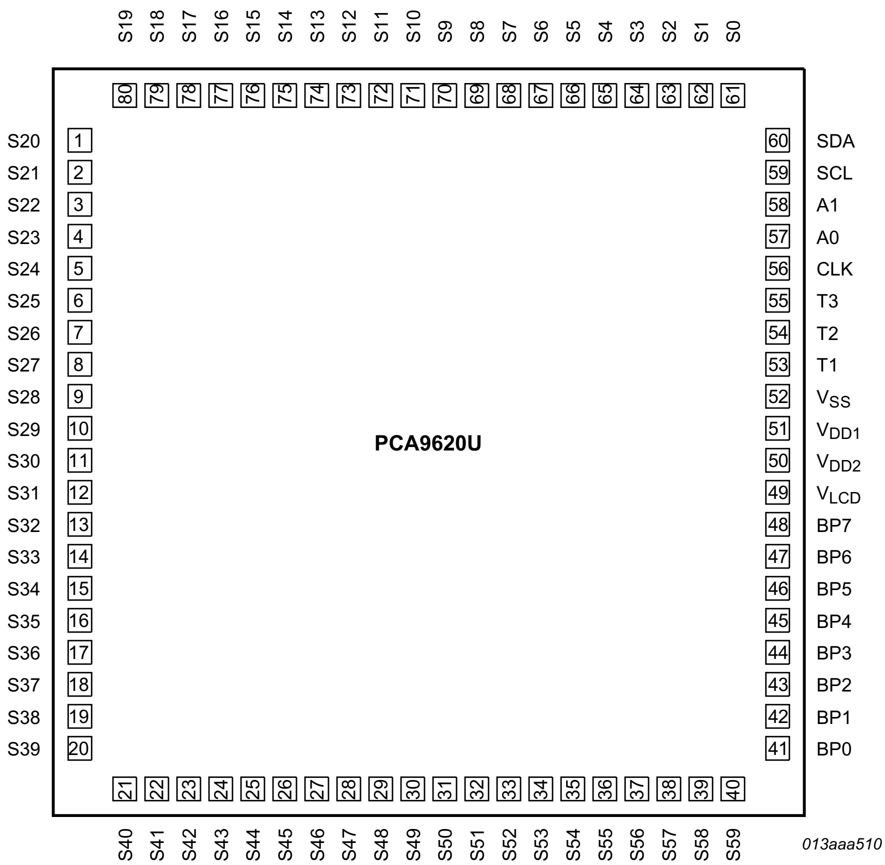
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 58 on page 64.

Fig 2. Pin configuration for LQFP80 (PCA9620H)



Viewed from active side. For mechanical details, see Figure 59 on page 65.

Fig 3. Pin configuration for PCA9620U (bare die)

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
S0 to S59	61 to 80 and 1 to 40	output	LCD segment
BP0 to BP7	41 to 48	output	LCD backplane
V_{LCD}	49	supply/output[1]	LCD supply voltage
V_{DD2}	50	supply	supply voltage 2 (charge pump)
V_{DD1}	51	supply	supply voltage 1 (analog and digital)
V_{SS}	52	supply	ground supply voltage
T1 to T3	53 to 55	input	test pins; must be tied to V_{SS} in applications
CLK	56	input/output	internal oscillator output, external oscillator input
A0, A1	57, 58	input	I^2C-bus slave address selection bit
SCL	59	input	I^2C-bus serial clock
SDA	60	input/output	I^2C-bus serial data

[1] When the internal V_{LCD} generation is used, this pin drives the V_{LCD} voltage. In this case pin V_{LCD} is an output. When the external supply is requested, then pin V_{LCD} is an input and V_{LCD} can be supplied to it. In this case, the internal charge pump must be disabled (see Table 9 on page 10).

8. Functional description

The PCA9620 is a versatile peripheral device designed to interface any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 480 elements.

8.1 Commands of PCA9620

The PCA9620 is controlled by 22 commands, which are defined in Table 5. Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCA9620.

Table 5. Commands of PCA9620

Command name	Bits								Reference
	7	6	5	4	3	2	1	0	
initialize	0	0	1	1	1	0	1	0	Section 8.1.1
OTP-refresh	1	1	0	1	0	0	0	0	Section 8.1.2
oscillator-ctrl	1	1	0	0	1	1	COE	OSC	Section 8.1.3
charge-pump-ctrl	1	1	0	0	0	0	CPE	CPC	Section 8.1.4
temp-msr-ctrl	1	1	0	0	1	0	TCE	TME	Section 8.1.5
temp-comp-SLA	0	0	0	1	1	SLA[2:0]			Table 30
temp-comp-SLB	0	0	1	0	0	SLB[2:0]			
temp-comp-SLC	0	0	1	0	1	SLC[2:0]			
temp-comp-SLD	0	0	1	1	0	SLD[2:0]			
set-VPR-MSB	0	1	0	0	VPR[7:4]				Section 8.1.6
set-VPR-LSB	0	1	0	1	VPR[3:0]				
display-enable	0	0	1	1	1	0	0	E	Section 8.1.7
set-MUX-mode	0	0	0	0	0	M[2:0]			Section 8.1.8
set-bias-mode	1	1	0	0	0	1	B[1:0]		Section 8.1.9
load-data-pointer	1	0	P[5:0]						Section 8.1.10
frame-frequency	0	1	1	F[4:0]					Section 8.1.11
input-bank-select	0	0	0	0	1	IB[2:0]			Section 8.1.12.1
output-bank-select	0	0	0	1	0	OB[2:0]			
write-RAM-data	B[7:0]								Section 8.1.13
temp-read	TD[7:0]								Section 8.1.14, Section 8.4.7
invmode_CPF_ctrl	1	1	0	1	0	1	LF	CPF	Section 8.1.15
temp-filter	1	1	0	1	0	0	1	TFE	Section 8.1.16

8.1.1 Command: initialize

This command generates a chip-wide reset which resets all command values to their default values (see Table 26 on page 18). It must be sent to the PCA9620 after power-on. After this command is sent, it is possible to send additional commands without the need to re-initialize the interface. Reset takes 100 ns to complete.

For further information, see Section 8.3 on page 17.

Table 6. Initialize - initialize command bit description

Bit	Symbol	Value	Description
7 to 0	-	00111010	fixed value

8.1.2 Command: OTP-refresh

In order to achieve the specified accuracy of V_{LCD}, the frame frequency, and the temperature measurement, each IC is calibrated during production and testing of the device. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. These cells are read by the device at power-on and every time when the initialize command or the OTP-refresh command is sent. This command will take approximately 10 ms to finish.

Table 7. OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
7 to 0	-	11010000	fixed value

8.1.3 Command: oscillator-ctrl

The oscillator-ctrl command switches between internal and external oscillator and enables or disables pin CLK.

Table 8. Oscillator-ctrl - oscillator control command bit description

For further information, see *Section 8.5 on page 41*.

Bit	Symbol	Value	Description
7 to 2	-	110011	fixed value
1	COE		control pin CLK
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state and may be left floating
		1	clock signal available on pin CLK
0	OSC		oscillator source
		0[1]	internal oscillator running
		1	external oscillator used; pin CLK becomes an input

[1] Default value.

8.1.4 Command: charge-pump-ctrl

The charge-pump-ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier setting.

Table 9. Charge-pump-ctrl - charge pump control command bit description

Bit	Symbol	Value	Description
7 to 2	-	110000	fixed value
1	CPE		charge pump switch
		0[1]	charge pump disabled; no internal V_{LCD} generation; external supply of V_{LCD}
		1	charge pump enabled
0	CPC		charge pump voltage multiplier setting
		0[1]	$V_{LCD} = 2 \times V_{DD2}$
		1	$V_{LCD} = 3 \times V_{DD2}$

[1] Default value.

8.1.5 Command: temp-msr-ctrl

The temp-msr-ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD}.

Table 10. Temp-msr-ctrl - temperature measurement control command bit description
For further information, see Section 8.4.8 on page 39.

Bit	Symbol	Value	Description
7 to 2	-	110010	fixed value
1	TCE		temperature compensation switch
		0	no temperature compensation of V_{LCD} possible
		1[1]	temperature compensation of V_{LCD} possible
0	TME		temperature measurement switch
		0	temperature measurement disabled; no temperature readout possible
		1[1]	temperature measurement enabled; temperature readout possible

[1] Default value.

8.1.6 Command: set-VPR-MSB and set-VPR-LSB

With these two instructions, it is possible to set the target V_{LCD} voltage for the internal charge pump, see Section 8.4.3 on page 34.

Table 11. Set-VPR-MSB - set VPR MSB command bit description

Bit	Symbol	Value	Description
7 to 4	-	0100	fixed value
3 to 0	VPR[7:4]	0000[1] to 1111	the four most significant bits of VPR[7:0]

[1] Default value.

Table 12. Set-VPR-LSB - set VPR LSB command bit description

Bit	Symbol	Value	Description
7 to 4	-	0101	fixed value
3 to 0	VPR[3:0]	0000[1] to 1111	the four least significant bits of VPR[7:0]

[1] Default value.

8.1.7 Command: display-enable

Table 13. Display-enable - display enable command bit description

Bit	Symbol	Value	Description
7 to 1	-	0011100	fixed value
0	E	0[1]	display disabled; backplane and segment outputs are internally connected to V_{SS}
		1	display enabled

[1] Default value.

8.1.8 Command: set-MUX-mode

Table 14. Set-MUX-mode - set multiplex drive mode command bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	fixed value
2 to 0	M[2:0]	000[1], 011, 110, 111	1:8 multiplex drive mode: 8 backplanes
		001	static drive mode: 1 backplane
		010	1:2 multiplex drive mode: 2 backplanes
		100	1:4 multiplex drive mode: 4 backplanes
		101	1:6 multiplex drive mode: 6 backplanes

[1] Default value.

8.1.9 Command: set-bias-mode

Table 15. Set-bias-mode - set bias mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	110001	fixed value
1 to 0	B[1:0]	00[1], 01	$\frac{1}{4}$ bias
		11	$\frac{1}{3}$ bias
		10	$\frac{1}{2}$ bias

[1] Default value.

8.1.10 Command: load-data-pointer

The load-data-pointer command defines one of the 60 display RAM addresses where the following display data will be sent to. For further information, see Section 8.9.1 on page 44.

Table 16. Load-data-pointer - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 6	-	10	fixed value
5 to 0	P[5:0]	000000 to 111111	6-bit binary value of 0 to 59

8.1.11 Command: frame-frequency

With the frame-frequency command, the frame frequency and the output clock frequency can be configured.

Table 17. Frame frequency - frame frequency and output clock frequency command bit description

Bit	Symbol	Value	Description
7 to 5	-	011	fixed value
4 to 0	F[4:0]	see Table 18	nominal frame frequency (Hz)

Table 18. Frame frequency values

F[4:0]	Nominal frame frequency, f_{fr} (Hz)[1]	Resultant oscillator frequency, f_{osc} (Hz)	Duty cycle (%)[2]
00000	60	2880	20 : 80
00001	70	3360	7 : 93
00010	80	3840	47 : 53
00011	91	4368	40 : 60
00100	100	4800	33 : 67
00101	109	5232	27 : 73
00110	120	5760	20 : 80
00111	129.7	6226	13 : 87
01000	141.2	6778	5 : 95
01001	150	7200	50 : 50
01010	160	7680	47 : 53
01011	171.4	8227	43 : 57
01100	177.8	8534	41 : 59
01101	192	9216	36 : 64
01110[3]	200	9600	33 : 67
01111	208.7	10018	30 : 70
10000	218.2	10474	27 : 73
10001	228.6	10973	23 : 77
10010	240	11520	20 : 80
10011	252.6	12125	16 : 84
10100, 10101	266.7	12802	10 : 90
10110, 10111	282.4	13555	5 : 95
11000 to 11111	300	14400	50 : 50

[1] Nominal frame frequency calculated for the default clock frequency of 9600 Hz.

[2] Duty cycle definition: % HIGH-level time : % LOW-level time.

[3] Default value.

8.1.12 Bank select commands

For multiplex drive modes 1:4, 1:2 and static drive mode, it is possible to write data to one area of the RAM while displaying from another. These areas are named as RAM banks. Input and output banks can be set independently from one another with the input-bank-select and the output-bank-select command. For further information, see Section 8.9.2 on page 49.

8.1.12.1 Command: input-bank-select

Table 19. Input-bank-select - input bank select command bit description[1]

Bit	Symbol	Value	Description		
7 to 3	-	00001	fixed value		
2 to 0	IB[2:0]		selects RAM bank to write to		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[2]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[1] Not applicable for multiplex drive mode 1:6 and 1:8.

[2] Default value.

8.1.12.2 Command: output-bank-select

Table 20. Output-bank-select - output bank select command bit description[1]

Bit	Symbol	Value	Description		
7 to 3	-	00010	fixed value		
2 to 0	OB[2:0]		selects RAM bank to read from to the LCD		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[2]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[1] Not applicable for multiplex drive mode 1:6 and 1:8.

[2] Default value.

8.1.13 Command: write-RAM-data

The write-RAM-data command writes data byte-wise to the RAM. After Power-On Reset (POR) the RAM content is random and should be brought to a defined status by clearing it (setting it logic 0).

Table 21. Write-RAM-data - write RAM data command bit description[1]

Bit	Symbol	Value	Description
7 to 0	B[7:0]	00000000 to 11111111	writing data byte-wise to RAM

[1] For this command bit RS of the control byte has to be set logic 1 (see Table 34 on page 55).

More information about the display RAM can be found in Section 8.9 on page 43.

8.1.14 Command: temp-read

The temp-read command allows reading out the temperature values measured by the internal temperature sensor.

Table 22. Temp-read - temperature readout command bit description[1]

For further information, see Table 10 on page 10 and Section 8.4.7 on page 38.

Bit	Symbol	Value	Description
7 to 0	TD[7:0]	00000000 to 11111111	readout representing the digital temperature

[1] For this command bit R/$\overline{W}$ of the I^2C-bus slave address byte has to be set logic 1 (see Table 33 on page 54).

8.1.15 Command: invmode_CPF_ctrl

The invmode_CPF_ctrl command allows changing the drive scheme inversion mode and the charge pump frequency.

The waveforms used to drive LCD displays inherently produce a DC voltage across the display cell. The PCA9620 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of compensation method is determined with the LF bit.

Table 23. Invmode_CPF_ctrl - inversion mode and charge pump frequency prescaler command bit description

Bit	Symbol	Value	Description
7 to 2	-	110101	fixed value
1	LF		set inversion mode
		0[1]	line inversion mode
		1	frame inversion mode
0	CPF		set charge pump oscillator frequency
		0[1]	$f_{osc(cp)}$ ~ 1 MHz
		1	$f_{osc(cp)}$ ~ 500 kHz

[1] Default value.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is possibility for flicker to occur.

The waveforms of Figure 16 on page 26 to Figure 22 on page 32 are showing line inversion mode. Figure 23 on page 33 shows one example of frame inversion.

8.1.16 Command: temp-filter

Table 24. Temp-filter - digital temperature filter command bit description

Bit	Symbol	Value	Description
7 to 1	-	1101001	fixed value
0	TFE		digital temperature filter switch
		0[1]	digital temperature filter disabled; the unfiltered digital value of TD[7:0] is immediately available for the readout and V_{LCD} compensation, see Section 8.4.7 on page 38
		1	digital temperature filter enabled

[1] Default value.

8.2 Possible display configurations

The PCA9620 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 4). It can directly drive any static or multiplexed LCD containing up to eight backplanes and up to 60 segments.

The display configurations possible with the PCA9620 depend on the number of active backplane outputs required. A selection of possible display configurations is given in Table 25.

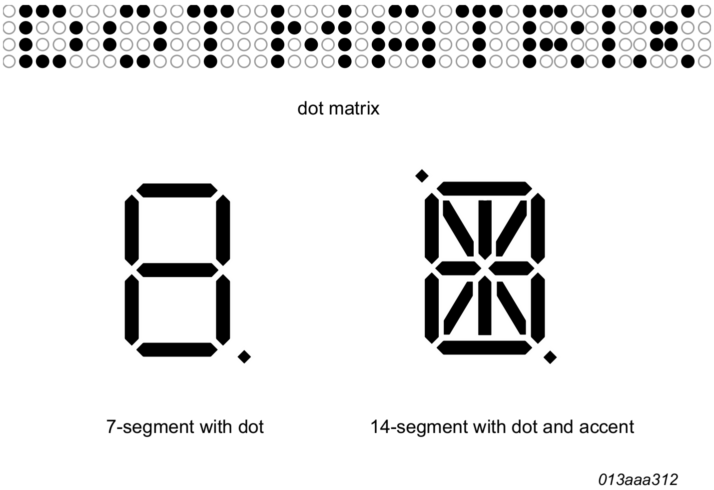
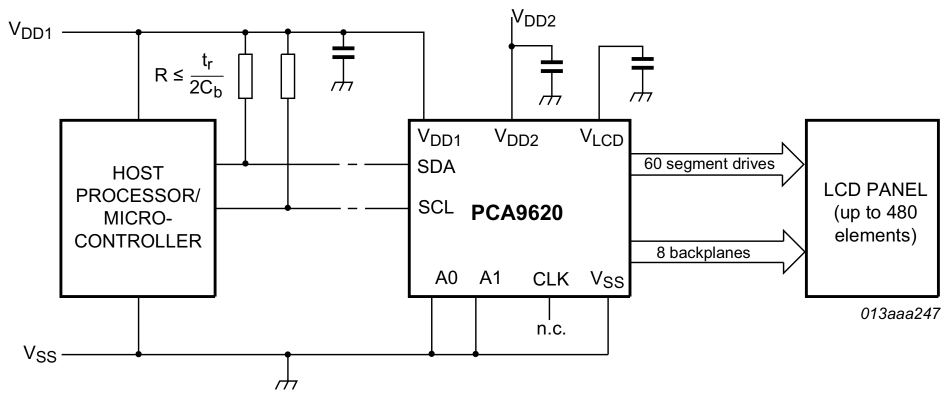


Fig 4. Example of displays suitable for PCA9620

Table 25. Selection of possible display configurations

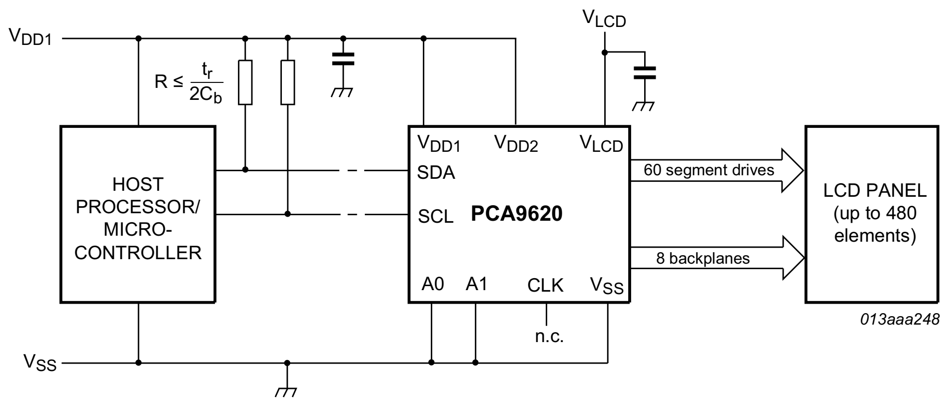
Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment	**14-segment**	
8	480	60	30	480 dots (8 × 60)
6	320	45	22	360 dots (6 × 60)
4	240	30	15	240 dots (4 × 60)
2	120	15	7	120 dots (2 × 60)
1	60	7	3	60 dots (1 × 60)

All of the display configurations in Table 25 can be implemented in the typical systems shown in Figure 5 (internal V_{LCD}) and in Figure 6 (external V_{LCD}).



V_{DD1} from 2.5 V to 5.5 V and V_{DD2} from 2.5 V to 5.5 V.

Fig 5. Typical system configuration when using the internal V_{LCD} generation



V_{DD1} from 2.5 V to 5.5 V, V_{DD2} from 2.5 V to 5.5 V and V_{LCD} from 2.5 V to 9.0 V.

Fig 6. Typical system configuration when using an external V_{LCD}

The host microcontroller maintains the two line I²C-bus communication channel with the PCA9620. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD1}, V_{DD2}, V_{SS}, V_{LCD}), the external capacitors, and the LCD panel selected for the application.

The minimum recommended values for external capacitors on V_{DD1}, V_{DD2}, and V_{LCD} are nominal 100 nF. When using bigger capacitors, especially on the V_{LCD}, the generated ripple will be consequently smaller. However it will take longer for the internal charge pump to reach the target V_{LCD} voltage first.

If V_{DD1} and V_{DD2} are connected externally, the capacitors on V_{DD1} and V_{DD2} can be replaced by a single capacitor with a minimum value of 200 nF.

Remark: In the case of insufficient decoupling, ripple of V_{DD1} and V_{DD2} will create additional V_{LCD} ripple. The ripple on V_{LCD} can be reduced by making the V_{SS} connection as low-ohmic as possible. Excessive ripple on V_{LCD} may cause flicker on the display.

8.3 Start-up and shut-down

8.3.1 Power-On Reset (POR)

At power-on, the PCA9620 resets to starting conditions as follows:

1. All backplane outputs are set to V_{SS}.
2. All segment outputs are set to V_{SS}.
3. Selected drive mode is: 1:8 with ¼ bias.
4. Input and output bank selectors are reset.
5. The I²C-bus interface is initialized.
6. The data pointer is cleared (set logic 0).
7. The Internal oscillator is running; no clock signal is available on pin CLK; pin CLK is in 3-state.
8. Temperature measurement is enabled.

9. Temperature filter is disabled.
10. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
11. The V_{LCD} temperature compensation is enabled.
12. The display is disabled.

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

The first command sent to the device after the power-on event must be the initialize command (see Section 8.1.1 on page 8).

After Power-On Reset (POR) and before enabling the display, the RAM content should be brought to a defined status

- by clearing it (setting it all logic 0) or
- by writing meaningful content (for example, a graphic)

otherwise unwanted display artifacts may appear on the display.

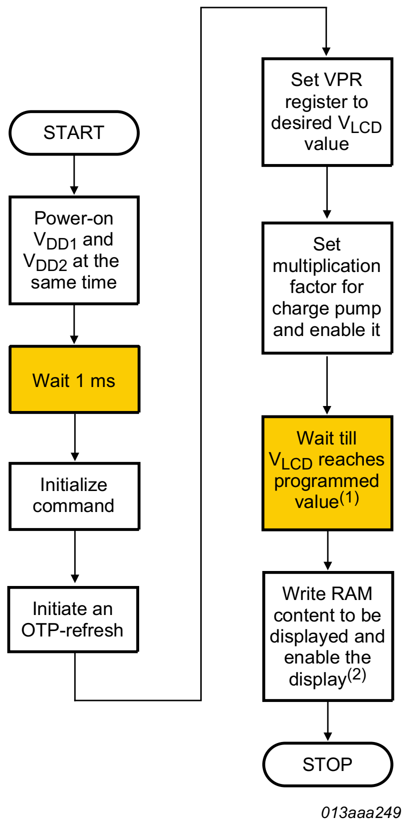
Table 26. Reset states

Bits labeled - are undefined at power-on.

Command name	Bits							
	7	6	5	4	3	2	1	0
initialize	0	0	1	1	1	0	1	0
OTP-refresh	1	1	0	1	0	0	0	0
oscillator-ctrl	1	1	0	0	1	1	0	0
charge-pump-ctrl	1	1	0	0	0	0	0	0
temp-msr-ctrl	1	1	0	0	1	0	1	1
temp-comp-SLA	0	0	0	1	1	0	0	0
temp-comp-SLB	0	0	1	0	0	0	0	0
temp-comp-SLC	0	0	1	0	1	0	0	0
temp-comp-SLD	0	0	1	1	0	0	0	0
set-VPR-MSB	0	1	0	0	0	0	0	0
set-VPR-LSB	0	1	0	1	0	0	0	0
display-enable	0	0	1	1	1	0	0	0
set-MUX-mode	0	0	0	0	0	0	0	0
set-bias-mode	1	1	0	0	0	1	0	0
load-data-pointer	1	0	0	0	0	0	0	0
frame-frequency	0	1	1	0	1	1	1	0
input-bank-select	0	0	0	0	1	0	0	0
output-bank-select	0	0	0	1	0	0	0	0
write-RAM-data	-	-	-	-	-	-	-	-
temp-read	0	1	0	0	0	0	0	0
invmode_CPF_ctrl	1	1	0	1	0	1	0	0
temp-filter	1	1	0	1	0	0	1	0

8.3.2 Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.



(1) This time depends on the external capacitor on pin V_{LCD}. For a capacitor of 100 nF a delay of 5 ms to 15 ms is expected.

When using the internal V_{LCD} generation, the display must not be enabled before the generation of V_{LCD} with the internal charge pump is completed. Otherwise unwanted display artifacts may appear on the display.

(2) RAM data may be written before or during the ramp-up of V_{LCD}.

Fig 7. Recommended start-up sequence when using the internal charge pump and the internal clock signal

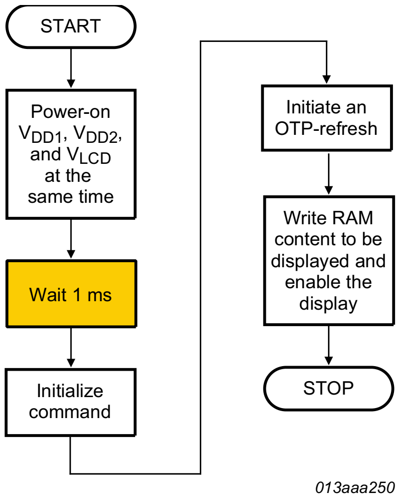
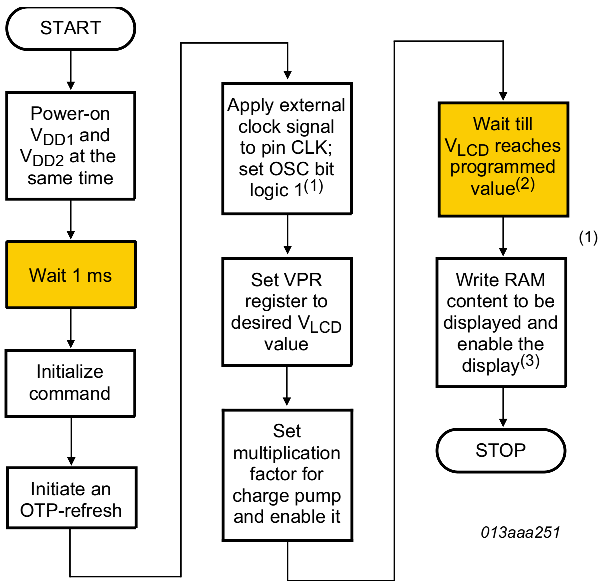


Fig 8. Recommended start-up sequence when using an external supplied V_{LCD} and the internal clock signal



(1) The external clock signal can be applied after the generation of the V_{LCD} voltage as well.

(2) This time depends on the external capacitor on pin V_{LCD}. For a capacitor of 100 nF a delay of 5 ms to 15 ms is expected.

(3) RAM data may be written before or during the ramp-up of V_{LCD}.

Fig 9. Recommended start-up sequence when using the internal charge pump and an external clock signal

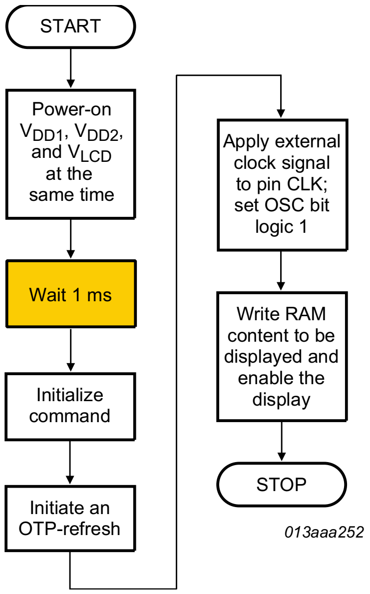


Fig 10. Recommended start-up sequence when using an external supplied V_{LCD} and an external clock signal

8.3.3 Recommended power-down sequences

With the following sequences, the PCA9620 can be set to a state of minimum power consumption, called power-down mode.

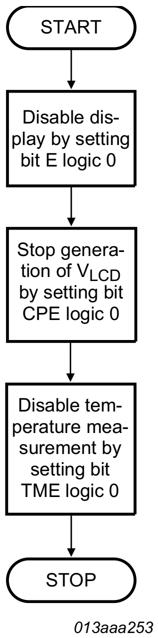


Fig 11. Recommended power-down sequence for minimum power-down current when using the internal charge pump and the internal clock signal

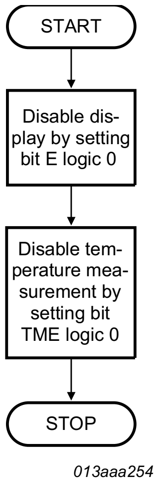


Fig 12. Recommended power-down sequence when using an external supplied V_{LCD} and the internal clock signal

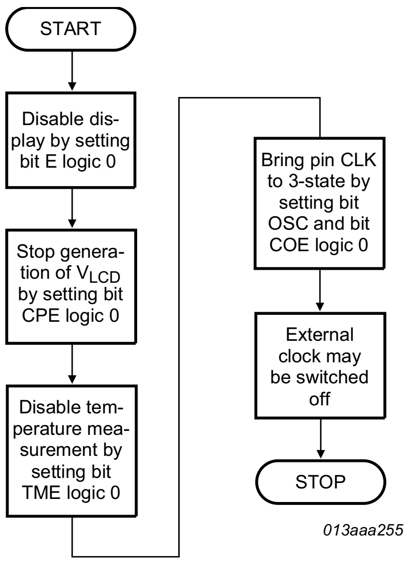


Fig 13. Recommended power-down sequence when using the internal charge pump and an external clock signal

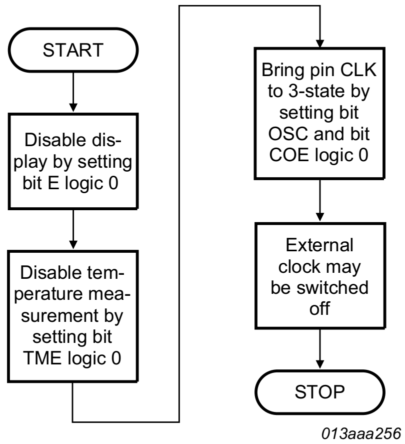


Fig 14. Recommended power-down sequence when using an external supplied V_{LCD} and an external clock signal

Remark: It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (refer to Section 10 on page 56). Otherwise it may cause unwanted display artifacts. The PCA9620 will not be damaged by uncontrolled removal of supply voltages

Remark: Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD1} or V_{DD2}) is off, or vice versa. It may cause unwanted display artifacts. To avoid such artifacts, external V_{LCD}, V_{DD1}, and V_{DD2} must be applied or removed together.

Remark: A clock signal must always be supplied to the device when the device is active; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. It is recommended to first disable the display and afterwards to remove the clock signal.

8.4 LCD voltage

8.4.1 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the set-bias-mode command (see Table 15 on page 11) and the set-MUX-mode command (see Table 14 on page 11).

Intermediate LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 27.

Discrimination is a term which is defined as the ratio of the $V_{on(RMS)}$ and $V_{off(RMS)}$ across a segment. It can be thought of as a measurement of contrast.

Table 27. LCD drive modes: summary of characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ [1]	V_{LCD}[2]
	Backplanes	Levels					
static	1	2	static	0	1	∞	$V_{on(RMS)}$
1:2 multiplex	2	3	½	0.354	0.791	2.236	2.828 × $V_{off(RMS)}$
1:2 multiplex	2	4	⅓	0.333	0.745	2.236	3.0 × $V_{off(RMS)}$
1:2 multiplex[3]	2	5	¼	0.395	0.729	1.845	2.529 × $V_{off(RMS)}$
1:4 multiplex[3]	4	3	½	0.433	0.661	1.527	2.309 × $V_{off(RMS)}$
1:4 multiplex	4	4	⅓	0.333	0.577	1.732	3.0 × $V_{off(RMS)}$
1:4 multiplex[3]	4	5	¼	0.331	0.545	1.646	3.024 × $V_{off(RMS)}$
1:6 multiplex[3]	6	3	½	0.456	0.612	1.341	2.191 × $V_{off(RMS)}$
1:6 multiplex	6	4	⅓	0.333	0.509	1.527	3.0 × $V_{off(RMS)}$
1:6 multiplex	6	5	¼	0.306	0.467	1.527	3.266 × $V_{off(RMS)}$
1:8 multiplex[3]	8	3	½	0.467	0.586	1.254	2.138 × $V_{off(RMS)}$
1:8 multiplex[3]	8	4	⅓	0.333	0.471	1.414	3.0 × $V_{off(RMS)}$
1:8 multiplex	8	5	¼	0.293	0.424	1.447	3.411 × $V_{off(RMS)}$

[1] Determined from Equation 3.

[2] Determined from Equation 2.

[3] In these examples the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a power saving from a reduction of the LCD voltage V_{LCD}.

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Bias is calculated by $\frac{1}{1 + a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

a = 3 for ¼ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (1)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 4 for 1:4 multiplex

n = 6 for 1:6 multiplex

n = 8 for 1:8 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$\frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (3)$$

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

8.4.1.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 15. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

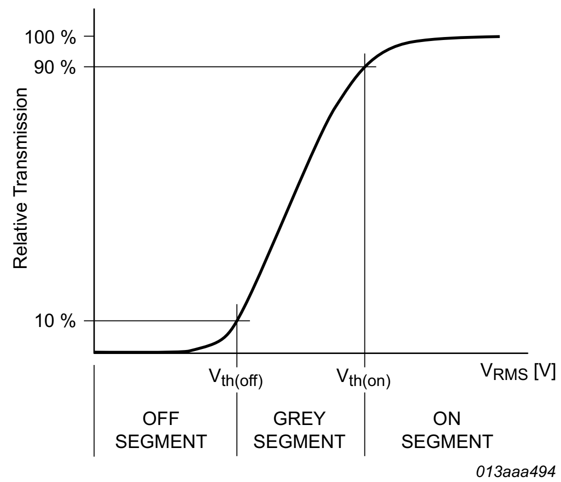


Fig 15. Electro-optical characteristic: relative transmission curve of the liquid