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PCA9625

16-bit Fm+ I²C-bus 100 mA 24 V LED driver

Rev. 02 — 15 January 2008   **Product data sheet**

1. General description

The PCA9625 is an I²C-bus controlled 16-bit LED driver optimized for voltage switch dimming and blinking 100 mA Red/Green/Blue/Amber (RGBA) LEDs. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCA9625 operates with a supply voltage range of 2.3 V to 5.5 V and the 100 mA open-drain outputs allow voltages up to 24 V.

The PCA9625 is one of the first LED controller devices in a new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and more densely populated bus operation (up to 4000 pF).

The active LOW Output Enable input pin ($\overline{OE}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCA9625 devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands. Seven hardware address pins allow up to 126 devices on the same bus.

The Software Reset (SWRST) Call allows the master to perform a reset of the PCA9625 through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the outputs to be set HIGH (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

The PCA9625 and PCA9635 software is identical and if the PCA9625 on-chip 100 mA NAND FETs do not provide enough current or voltage to drive the LEDs, then the PCA9635 with larger current or higher voltage external drivers can be used.

2. Features

- 16 LED drivers. Each output programmable at:
  - ◆ Off
  - ◆ On
  - ◆ Programmable LED brightness
  - ◆ Programmable group dimming/blinking mixed with individual LED brightness
- 1 MHz Fast-mode Plus compatible I^{2}C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 97 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 190 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 24 Hz to 10.73 s and duty cycle from 0 % to 99.6 %
- Sixteen open-drain outputs can sink between 0 mA to 100 mA and are tolerant to a maximum off state voltage of 24 V. No input function.
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs
- 7 hardware address pins allow 126 PCA9625 devices to be connected to the same I^{2}C-bus and to be individually programmed
- 4 software programmable I^{2}C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCA9625s on the I^{2}C-bus can be addressed at the same time and the second register used for three different addresses so that $\frac{1}{3}$ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for I^{2}C-bus address.
- Software Reset feature (SWRST Call) allows the device to be reset through the I^{2}C-bus
- 25 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage (V_{DD}) range of 2.3 V to 5.5 V; also requires $V_{DD(DRV)FET}$ supply voltage range of 10 V to 24 V
- 5.5 V tolerant inputs on non-LED pins
- −40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offered: SO32

3. Applications

- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1.   Ordering information

Type number	Topside mark	Package		
		Name	**Description**	**Version**
PCA9625D	PCA9625D	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

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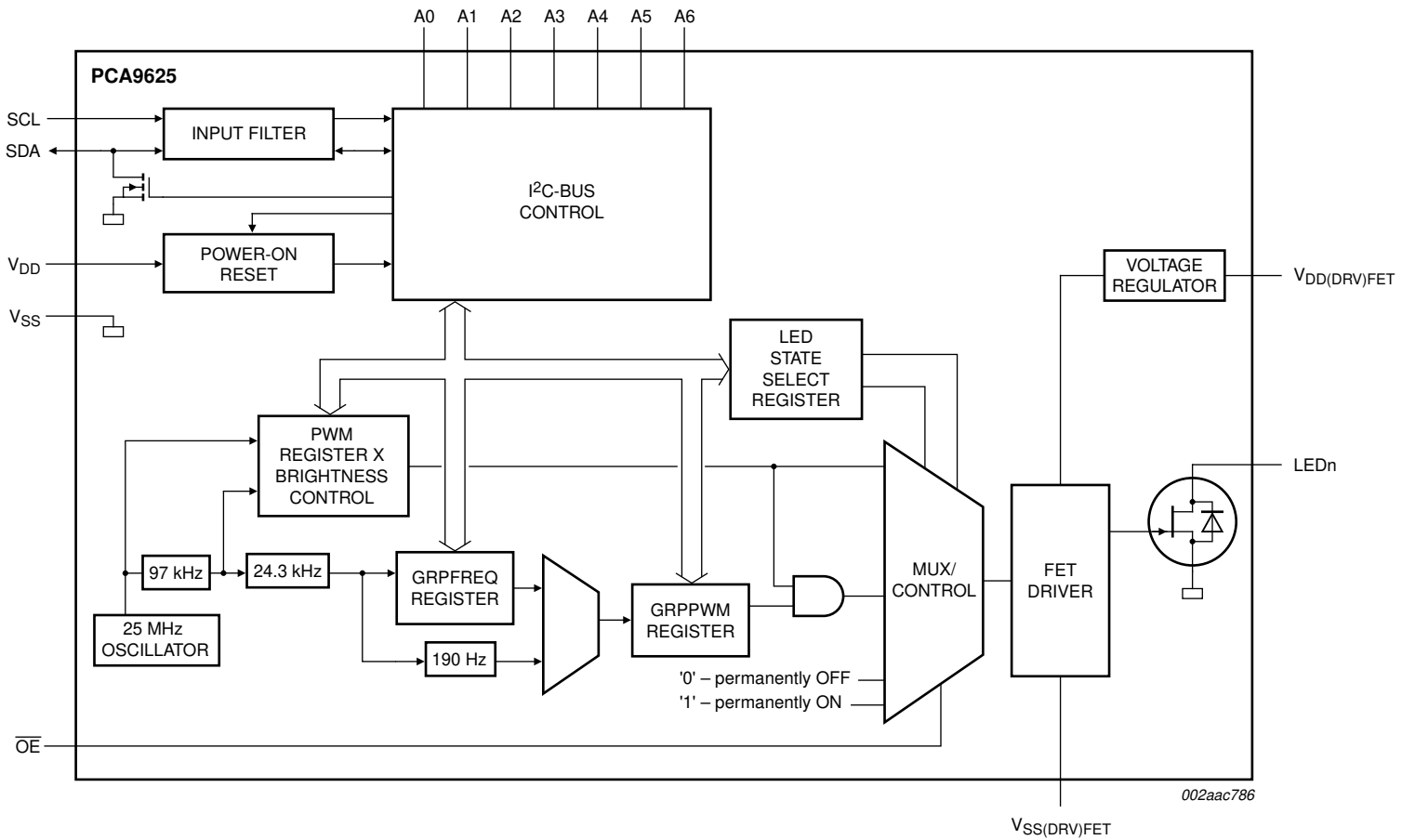
5. Block diagram

Remark: Only one LED output shown for clarity.

Fig 1. **Block diagram of PCA9625**
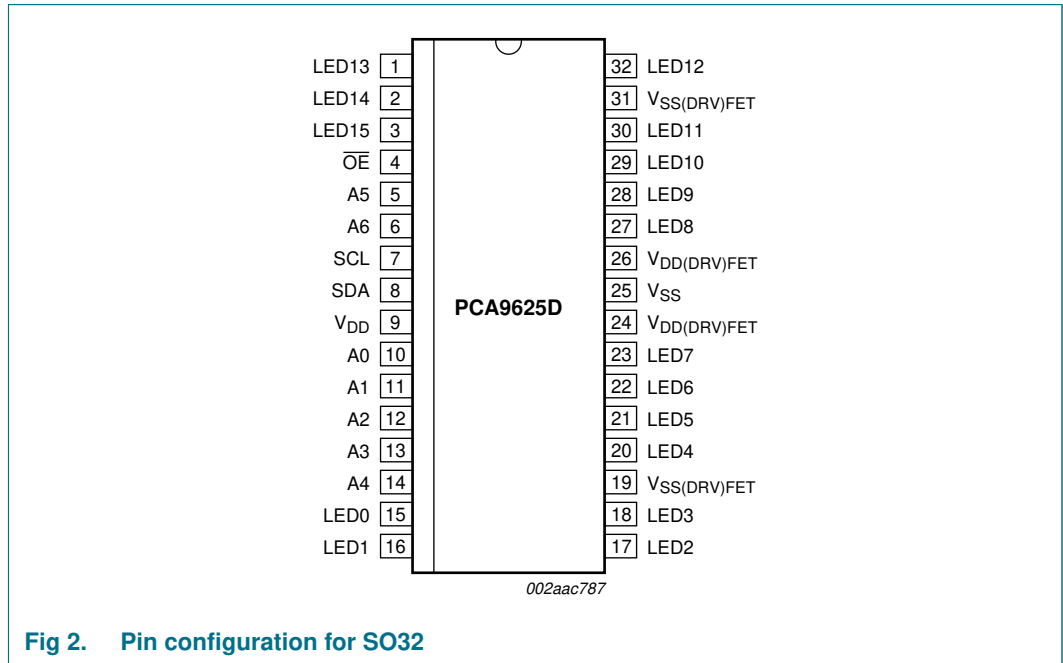
6. Pinning information

6.1 Pinning

LED13	1	32	LED12
LED14	2	31	V$_{SS(DRV)FET}$
LED15	3	30	LED11
$\overline{OE}$	4	29	LED10
A5	5	28	LED9
A6	6	27	LED8
SCL	7	26	V$_{DD(DRV)FET}$
SDA	8	25	V$_{SS}$
V$_{DD}$	9	24	V$_{DD(DRV)FET}$
A0	10	23	LED7
A1	11	22	LED6
A2	12	21	LED5
A3	13	20	LED4
A4	14	19	V$_{SS(DRV)FET}$
LED0	15	18	LED3
LED1	16	17	LED2

PCA9625D

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Fig 2. Pin configuration for SO32

6.2 Pin description

Table 2. Pin description for SO32

Symbol	Pin	Type	Description
LED13	1	O	LED driver 13
LED14	2	O	LED driver 14
LED15	3	O	LED driver 15
$\overline{OE}$	4	I	active LOW output enable
A5	5	I	address input 5
A6	6	I	address input 6
SCL	7	I	serial clock line
SDA	8	I/O	serial data line
V$_{DD}$	9	power supply	supply voltage
A0	10	I	address input 0
A1	11	I	address input 1
A2	12	I	address input 2
A3	13	I	address input 3
A4	14	I	address input 4
LED0	15	O	LED driver 0
LED1	16	O	LED driver 1
LED2	17	O	LED driver 2
LED3	18	O	LED driver 3

Table 2. **Pin description for SO32**

Symbol	Pin	Type	Description
$V_{SS(DRV)FET}$	19	power supply	FET driver supply ground
LED4	20	O	LED driver 4
LED5	21	O	LED driver 5
LED6	22	O	LED driver 6
LED7	23	O	LED driver 7
$V_{DD(DRV)FET}$	24	power supply	supply voltage for FET driver
V_{SS}	25	power supply	supply ground
$V_{DD(DRV)FET}$	26	power supply	supply voltage for FET driver
LED8	27	O	LED driver 8
LED9	28	O	LED driver 9
LED10	29	O	LED driver 10
LED11	30	O	LED driver 11
$V_{SS(DRV)FET}$	31	power supply	FET driver supply ground
LED12	32	O	LED driver 12

7. Functional description

Refer to Figure 1 "Block diagram of PCA9625".

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

There are a maximum of 128 possible programmable addresses using the 7 hardware address pins. Two of these addresses, Software Reset and LED All Call, cannot be used because their default power-up state is ON, leaving a maximum of 126 addresses. Using other reserved addresses, as well as any other Sub Call address, will reduce the total number of possible addresses even further.

7.1.1 Regular I2C-bus slave address

The I2C-bus slave address of the PCA9625 is shown in Figure 3. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

Remark: Reserved I2C-bus addresses must be used with caution since they can interfere with:

- 'reserved for future use' I2C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)
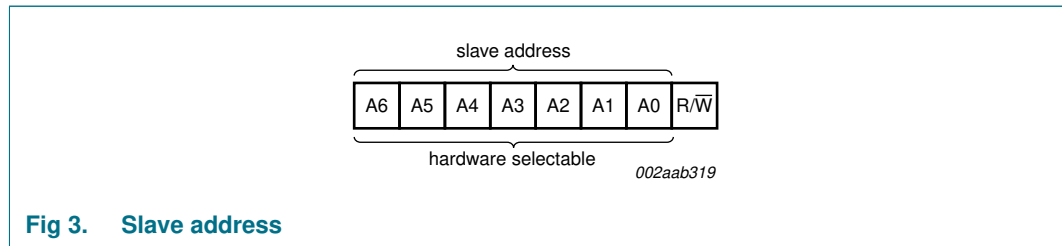
Fig 3. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I2C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000
- Programmable through I2C-bus (volatile programming)
- At power-up, LED All Call I2C-bus address is enabled. PCA9625 sends an ACK when E0h (R/$\overline{W}$ = 0) or E1h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.8 "ALLCALLADR, LED All Call I2C-bus address" for more detail.

Remark: The default LED All Call I2C-bus address (E0h or 1110 000) must not be used as a regular I2C-bus slave address since this address is enabled at power-up. All the PCA9625s on the I2C-bus will acknowledge the address if sent by the I2C-bus master.

7.1.3 LED Sub Call I2C-bus addresses

- 3 different I2C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: E2h or 1110 001
  - SUBADR2 register: E4h or 1110 010
  - SUBADR3 register: E8h or 1110 100
- Programmable through I2C-bus (volatile programming)
- At power-up, Sub Call I2C-bus addresses are disabled. PCA9625 does not send an ACK when E2h (R/$\overline{W}$ = 0) or E3h (R/$\overline{W}$ = 1), E4h (R/$\overline{W}$ = 0) or E5h (R/$\overline{W}$ = 1), or E8h (R/$\overline{W}$ = 0) or E9h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.7 "SUBADR1 to SUBADR3, I2C-bus subaddress 1 to 3" for more detail.

Remark: The default LED Sub Call I2C-bus addresses may be used as regular I2C-bus slave addresses as long as they are disabled.

7.1.4 Software Reset I2C-bus address

The address shown in Figure 4 is used when a reset of the PCA9625 needs to be performed by the master. The Software Reset address (SWRST Call) must be used with R/$\overline{W}$ = logic 0. If R/$\overline{W}$ = logic 1, the PCA9625 does not acknowledge the SWRST. See Section 7.6 "Software Reset" for more detail.
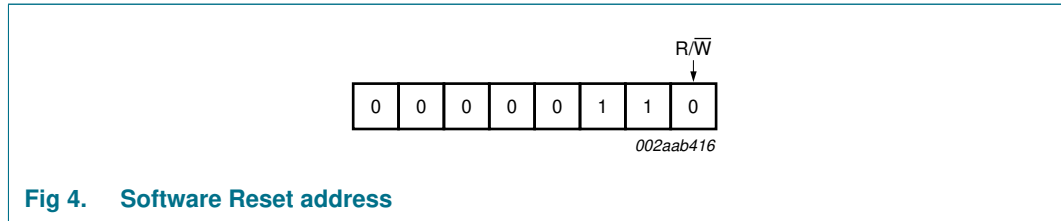
Fig 4.   Software Reset address

Remark: The Software Reset I²C-bus address is a reserved address and cannot be used as a regular I²C-bus slave address or as an LED All Call or LED Sub Call address.

7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCA9625, which will be stored in the Control register.

The lowest 5 bits are used as a pointer to determine which register will be accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).
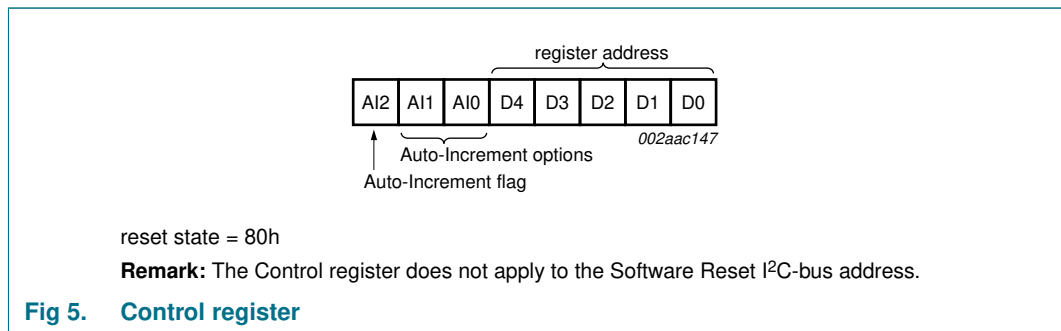

reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address.

Fig 5.   Control register

When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 3.   Auto-Increment options

AI2	AI1	AI0	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for all registers. D[4:0] roll over to '0 0000' after the last register (1 1011) is accessed.
1	0	1	Auto-Increment for individual brightness registers only. D[4:0] roll over to '0 0010' after the last register (1 0001) is accessed.
1	1	0	Auto-Increment for global control registers only. D[4:0] roll over to '1 0010' after the last register (1 0011) is accessed.
1	1	1	Auto-Increment for individual and global control registers only. D[4:0] roll over to '0 0010' after the last register (1 0011) is accessed.

Remark: Other combinations not shown in Table 3 (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

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AI[2:0] = 000 is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the 16 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I²C-bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individual and global changes must be performed during the same I²C-bus communication, for example, changing a color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 1011 (as defined in Table 4). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AI[2:0]. See Table 3 for rollover values. For example, if the Control register = 1111 0100 (F4h), then the register addressing sequence will be (in hex): 14 → … → 1B → 00 → … → 13 → 02 → … → 13 → 02 → … → 13 → 02 → … as long as the master keeps sending or reading data.

7.3 Register definitions

Table 4.   Register summary[1][2]

Register number (hex)	D4	D3	D2	D1	D0	Name	Type	Function
00	0	0	0	0	0	MODE1	read/write	Mode register 1
01	0	0	0	0	1	MODE2	read/write	Mode register 2
02	0	0	0	1	0	PWM0	read/write	brightness control LED0
03	0	0	0	1	1	PWM1	read/write	brightness control LED1
04	0	0	1	0	0	PWM2	read/write	brightness control LED2
05	0	0	1	0	1	PWM3	read/write	brightness control LED3
06	0	0	1	1	0	PWM4	read/write	brightness control LED4
07	0	0	1	1	1	PWM5	read/write	brightness control LED5
08	0	1	0	0	0	PWM6	read/write	brightness control LED6
09	0	1	0	0	1	PWM7	read/write	brightness control LED7
0A	0	1	0	1	0	PWM8	read/write	brightness control LED8
0B	0	1	0	1	1	PWM9	read/write	brightness control LED9
0C	0	1	1	0	0	PWM10	read/write	brightness control LED10
0D	0	1	1	0	1	PWM11	read/write	brightness control LED11
0E	0	1	1	1	0	PWM12	read/write	brightness control LED12

Table 4.   Register summary[1][2] *…continued*

Register number (hex)	D4	D3	D2	D1	D0	Name	Type	Function
0F	0	1	1	1	1	PWM13	read/write	brightness control LED13
10	1	0	0	0	0	PWM14	read/write	brightness control LED14
11	1	0	0	0	1	PWM15	read/write	brightness control LED15
12	1	0	0	1	0	GRPPWM	read/write	group duty cycle control
13	1	0	0	1	1	GRPFREQ	read/write	group frequency
14	1	0	1	0	0	LEDOUT0	read/write	LED output state 0
15	1	0	1	0	1	LEDOUT1	read/write	LED output state 1
16	1	0	1	1	0	LEDOUT2	read/write	LED output state 2
17	1	0	1	1	1	LEDOUT3	read/write	LED output state 3
18	1	1	0	0	0	SUBADR1	read/write	I2C-bus subaddress 1
19	1	1	0	0	1	SUBADR2	read/write	I2C-bus subaddress 2
1A	1	1	0	1	0	SUBADR3	read/write	I2C-bus subaddress 3
1B	1	1	0	1	1	ALLCALLADR	read/write	LED All Call I2C-bus address

[1]   Only D[4:0] = 0 0000 to 1 1011 are allowed and will be acknowledged. D[4:0] = 1 1100 to 1 1111 are reserved and will not be acknowledged.

[2]   When writing to the Control register, bit 4 must be programmed with logic 0 for proper device operation.

7.3.1 Mode register 1, MODE1

Table 5.   MODE1 - Mode register 1 (address 00h) bit description
*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AI2	read only	0	Register Auto-Increment disabled.
			1*	Register Auto-Increment enabled.
6	AI1	read only	0*	Auto-Increment bit 1 = 0.
			1	Auto-Increment bit 1 = 1.
5	AI0	read only	0*	Auto-Increment bit 0 = 0.
			1	Auto-Increment bit 0 = 1.
4	SLEEP	R/W	0	Normal mode[1].
			1*	Low power mode. Oscillator off[2].
3	SUB1	R/W	0*	PCA9625 does not respond to I2C-bus subaddress 1.
			1	PCA9625 responds to I2C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9625 does not respond to I2C-bus subaddress 2.
			1	PCA9625 responds to I2C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9625 does not respond to I2C-bus subaddress 3.
			1	PCA9625 responds to I2C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9625 does not respond to LED All Call I2C-bus address.
			1*	PCA9625 responds to LED All Call I2C-bus address.

[1]   It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 1. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2]   No blinking or dimming is possible when the oscillator is off.

7.3.2 Mode register 2, MODE2

Table 6. **MODE2 - Mode register 2 (address 01h) bit description**
*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	read only	0*	reserved
5	DMBLNK	R/W	0*	group control = dimming.
			1	group control = blinking.
4	INVRT	R/W	0*	reserved; write must always be a logic 0
3	OCH	R/W	0*	outputs change on STOP command[1]
			1	outputs change on ACK
2	-	R/W	1*	reserved; write must always be a logic 1
1	-	R/W	0*	reserved; write must always be a logic 0
0	-	R/W	1*	reserved; write must always be a logic 1

[1] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCA9625. Applicable to registers from 02h (PWM0) to 08h (LEDOUT) only.

7.3.3 PWM0 to PWM15, individual brightness control

Table 7. **PWM0 to PWM15 - PWM registers 0 to 15 (address 02h to 11h) bit description**
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle
0Ah	PWM8	7:0	IDC8[7:0]	R/W	0000 0000*	PWM8 Individual Duty Cycle
0Bh	PWM9	7:0	IDC9[7:0]	R/W	0000 0000*	PWM9 Individual Duty Cycle
0Ch	PWM10	7:0	IDC10[7:0]	R/W	0000 0000*	PWM10 Individual Duty Cycle
0Dh	PWM11	7:0	IDC11[7:0]	R/W	0000 0000*	PWM11 Individual Duty Cycle
0Eh	PWM12	7:0	IDC12[7:0]	R/W	0000 0000*	PWM12 Individual Duty Cycle
0Fh	PWM13	7:0	IDC13[7:0]	R/W	0000 0000*	PWM13 Individual Duty Cycle
10h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000*	PWM14 Individual Duty Cycle
11h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000*	PWM15 Individual Duty Cycle

A 97 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle\ =\ \frac{IDCx[7:0]}{256} \tag{1}$$

7.3.4 GRPPWM, group duty cycle control

Table 8.   GRPPWM - Group brightness control register (address 12h) bit description
Legend: * default value

Address	Register	Bit	Symbol	Access	Value	Description
12h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190 Hz fixed frequency signal is superimposed with the 97 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 16 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle\ =\ \frac{GDC[7:0]}{256} \tag{2}$$

7.3.5 GRPFREQ, group frequency

Table 9.   GRPFREQ - Group Frequency register (address 13h) bit description
Legend: * default value.

Address	Register	Bit	Symbol	Access	Value	Description
13h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$global\ blinking\ period\ =\ \frac{GFRQ[7:0]+1}{24}(s) \tag{3}$$

7.3.6 LEDOUT0 to LEDOUT3, LED driver output state

Table 10. **LEDOUT0 to LEDOUT3 - LED driver output state register (address 14h to 17h) bit description**

Legend: * default value.

Address	Register	Bit	Symbol	Access	Value	Description
14h	LEDOUT0	7:6	LDR3	R/W	00*	LED3 output state control
		5:4	LDR2	R/W	00*	LED2 output state control
		3:2	LDR1	R/W	00*	LED1 output state control
		1:0	LDR0	R/W	00*	LED0 output state control
15h	LEDOUT1	7:6	LDR7	R/W	00*	LED7 output state control
		5:4	LDR6	R/W	00*	LED6 output state control
		3:2	LDR5	R/W	00*	LED5 output state control
		1:0	LDR4	R/W	00*	LED4 output state control
16h	LEDOUT2	7:6	LDR11	R/W	00*	LED11 output state control
		5:4	LDR10	R/W	00*	LED10 output state control
		3:2	LDR9	R/W	00*	LED9 output state control
		1:0	LDR8	R/W	00*	LED8 output state control
17h	LEDOUT3	7:6	LDR15	R/W	00*	LED15 output state control
		5:4	LDR14	R/W	00*	LED14 output state control
		3:2	LDR13	R/W	00*	LED13 output state control
		1:0	LDR12	R/W	00*	LED12 output state control

LDRx = 00 — LED driver x is off (default power-up state).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

7.3.7 SUBADR1 to SUBADR3, I2C-bus subaddress 1 to 3

Table 11. **SUBADR1 to SUBADR3 - I2C-bus subaddress registers 0 to 3 (address 18h to 1Ah) bit description**

Legend: * default value.

Address	Register	Bit	Symbol	Access	Value	Description
18h	SUBADR1	7:1	A1[7:1]	R/W	1110 001*	I2C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
19h	SUBADR2	7:1	A2[7:1]	R/W	1110 010*	I2C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
1Ah	SUBADR3	7:1	A3[7:1]	R/W	1110 100*	I2C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Subaddresses are programmable through the I2C-bus. Default power-up values are E2h, E4h, E8h, and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to their right values, SUBx bits need to be set to logic 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I2C-bus subaddress are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to logic 1, the corresponding I2C-bus subaddress can be used during either an I2C-bus read or write sequence.

7.3.8 ALLCALLADR, LED All Call I2C-bus address

Table 12.   ALLCALLADR - LED All Call I2C-bus address register (address 1Bh) bit description
Legend: * default value.

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I2C-bus address register
		0	AC[0]	R only	0*	reserved

The LED All Call I2C-bus address allows all the PCA9625s on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1 (power-up default state)). This address is programmable through the I2C-bus and can be used during either an I2C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I2C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

7.4 Active LOW output enable input

The active LOW output enable ($\overline{OE}$) pin, allows to enable or disable all the LED outputs at the same time.

- When a LOW level is applied to $\overline{OE}$ pin, all the LED outputs are enabled.
- When a HIGH level is applied to $\overline{OE}$ pin, all the LED outputs are high-impedance.

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCA9625 devices at the same time. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{OE}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use $\overline{OE}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use $\overline{OE}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

7.5 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9625 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9625 registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.6 Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The SWRST Call function is defined as the following:

1. A START command is sent by the I²C-bus master.

2. The reserved SWRST I²C-bus address '0000 011' with the R/$\overline{W}$ bit set to '0' (write) is sent by the I²C-bus master.

3. The PCA9625 device(s) acknowledge(s) after seeing the SWRST Call address '0000 0110' (06h) only. If the R/$\overline{W}$ bit is set to '1' (read), no acknowledge is returned to the I²C-bus master.

4. Once the SWRST Call address has been sent and acknowledged, the master sends 2 bytes with 2 specific values (SWRST data byte 1 and byte 2):

   a. Byte 1 = A5h: the PCA9625 acknowledges this value only. If byte 1 is not equal to A5h, the PCA9625 does not acknowledge it.

   b. Byte 2 = 5Ah: the PCA9625 acknowledges this value only. If byte 2 is not equal to 5Ah, then the PCA9625 does not acknowledge it.

   If more than 2 bytes of data are sent, the PCA9625 does not acknowledge any more.

5. Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a STOP command to end the SWRST Call: the PCA9625 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

The I²C-bus master must interpret a non-acknowledge from the PCA9625 (at any time) as a 'SWRST Call Abort'. The PCA9625 does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

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7.7 Individual brightness control with group dimming/blinking

A 97 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to $\frac{1}{10.73}$ Hz (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.

Minimum pulse width for LEDn Brightness Control is 40 ns.

Minimum pulse width for Group Dimming is 20.48 μs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 2 pulses of the LED Brightness Control signal (pulse width = N × 40 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 4 (8 pulses).

Fig 6.   Brightness + Group Dimming signals

8. Characteristics of the I2C-bus

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).
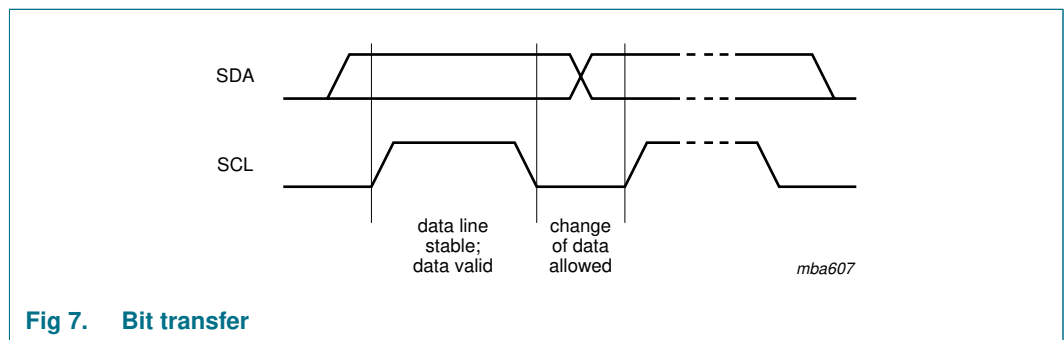
Fig 7.   **Bit transfer**

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 8).
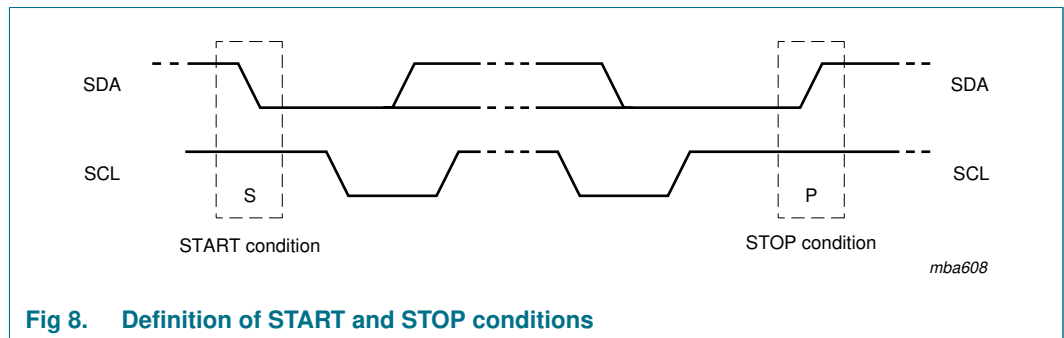

Fig 8.   **Definition of START and STOP conditions**

8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 9).
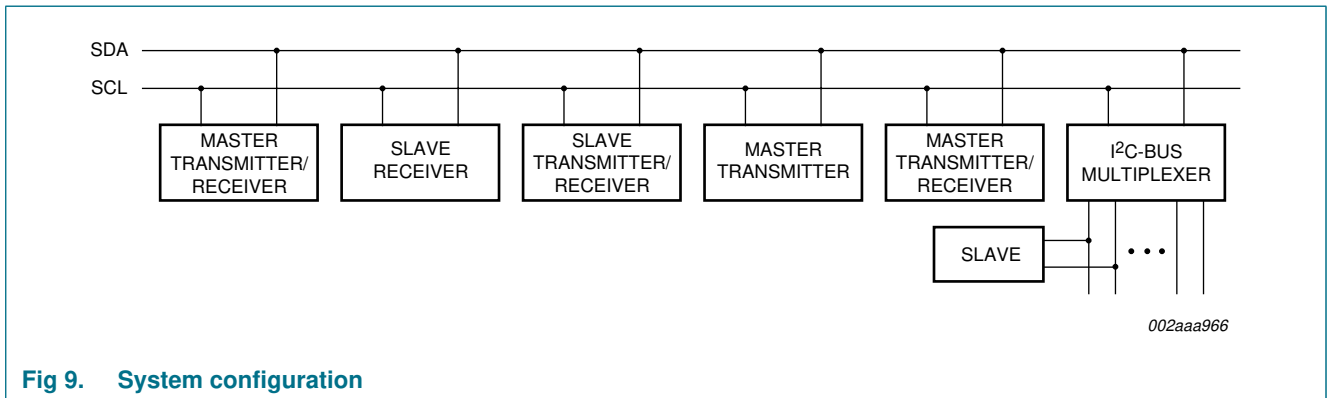
Fig 9. **System configuration**

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.
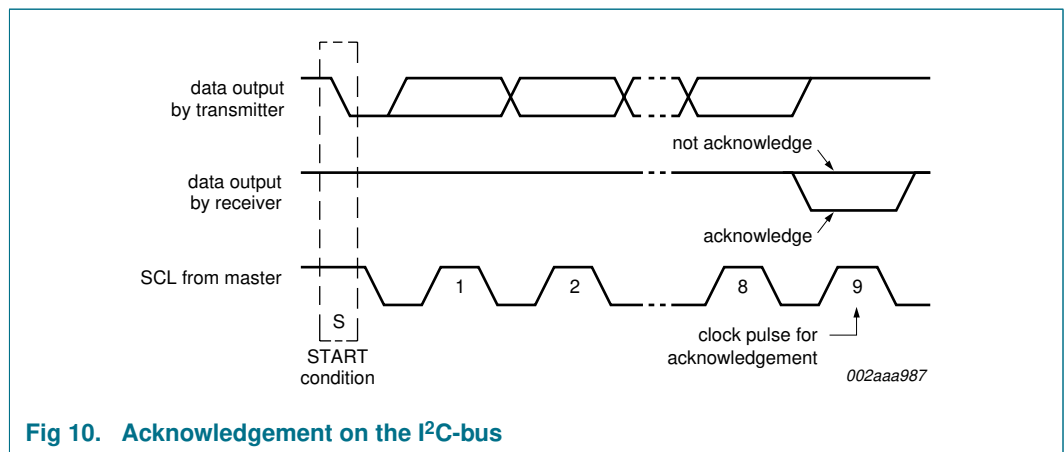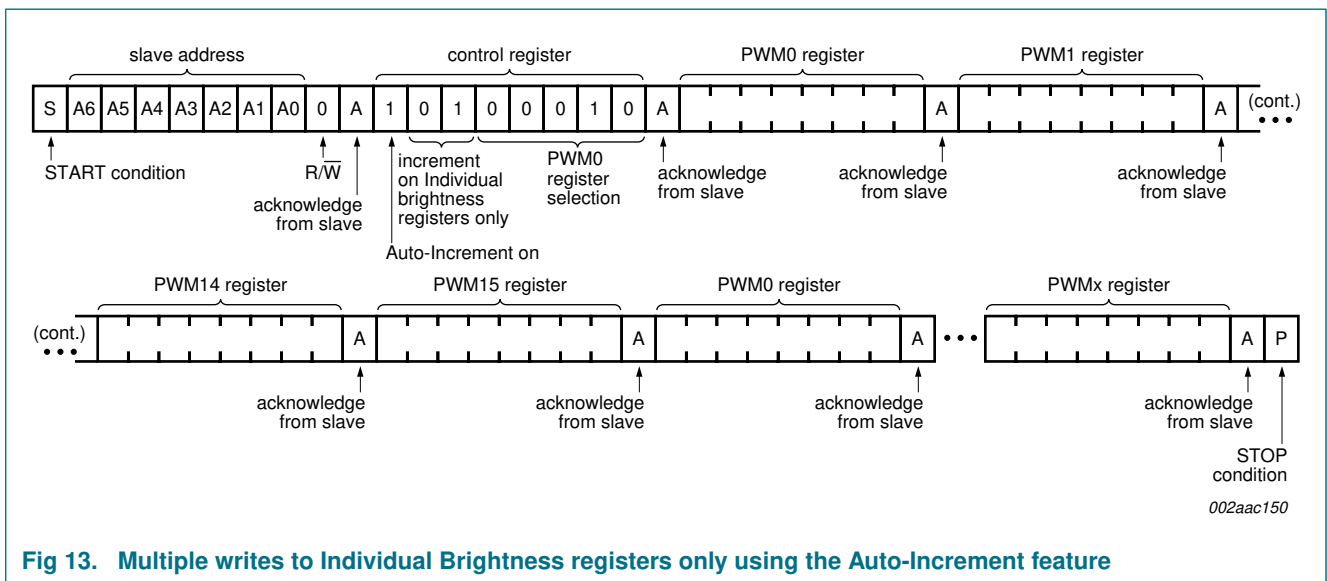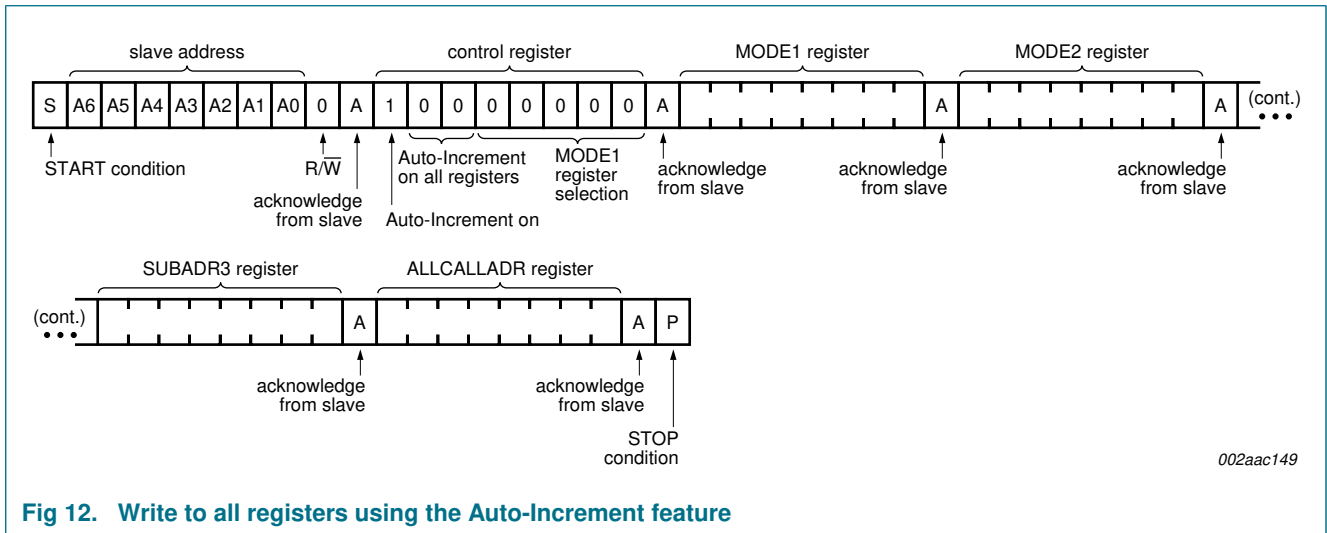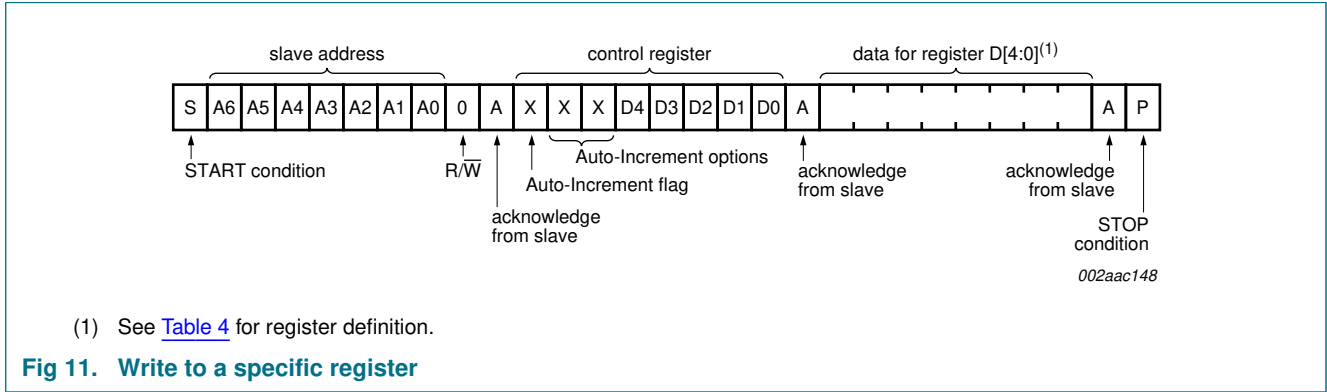

Fig 10. Acknowledgement on the I2C-bus

9. Bus transactions

(1) See Table 4 for register definition.

Fig 11. Write to a specific register

Fig 12. Write to all registers using the Auto-Increment feature

Fig 13. Multiple writes to Individual Brightness registers only using the Auto-Increment feature
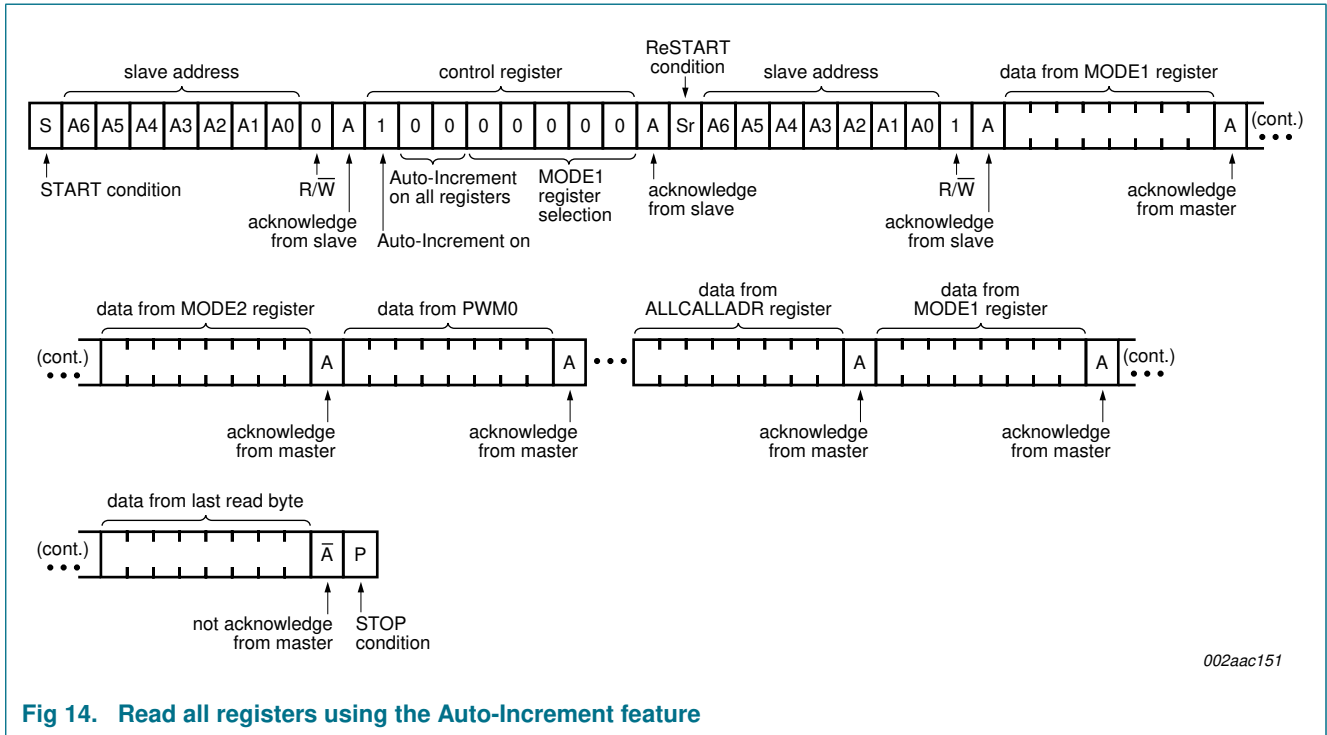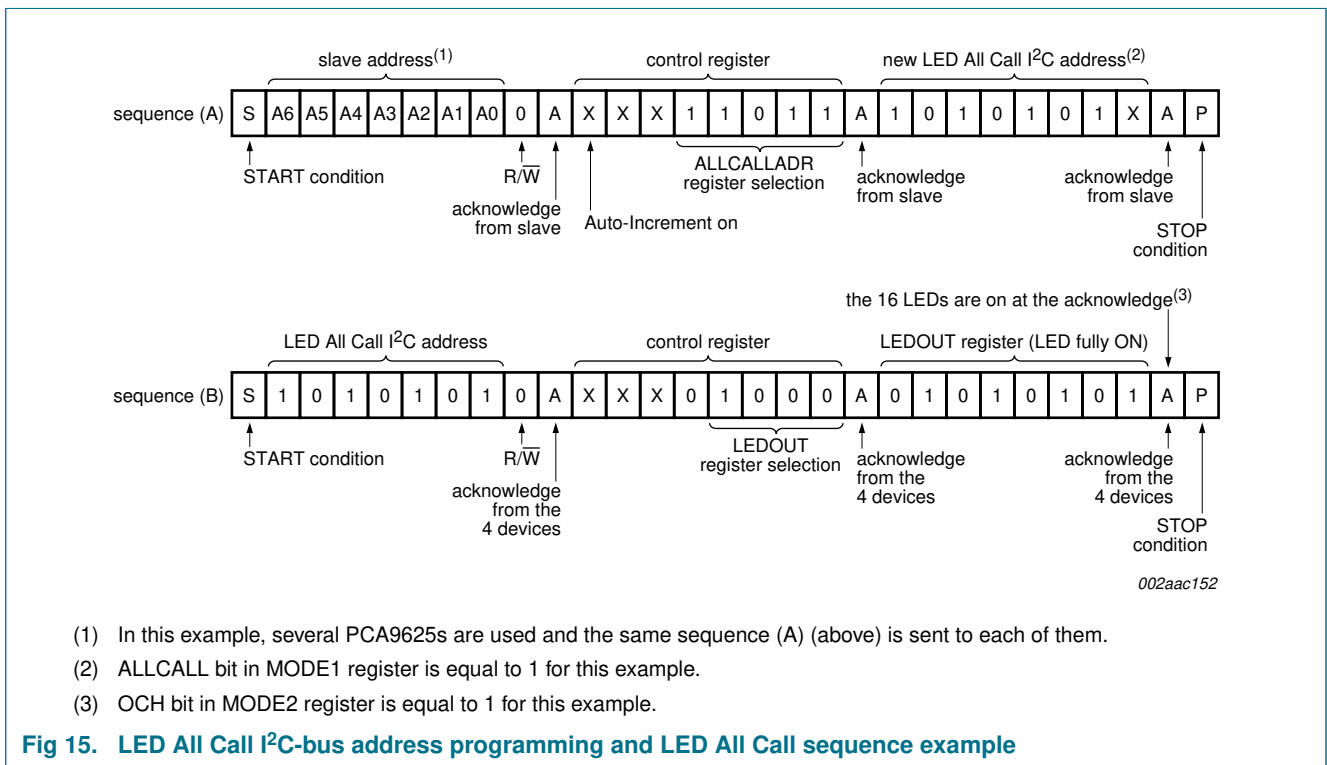
002aac151

Fig 14. Read all registers using the Auto-Increment feature

002aac152

(1) In this example, several PCA9625s are used and the same sequence (A) (above) is sent to each of them.

(2) ALLCALL bit in MODE1 register is equal to 1 for this example.

(3) OCH bit in MODE2 register is equal to 1 for this example.

Fig 15. LED All Call I2C-bus address programming and LED All Call sequence example

10. Application design-in information

(1) $\overline{OE}$ requires pull-up resistor if control signal from the master is open-drain.
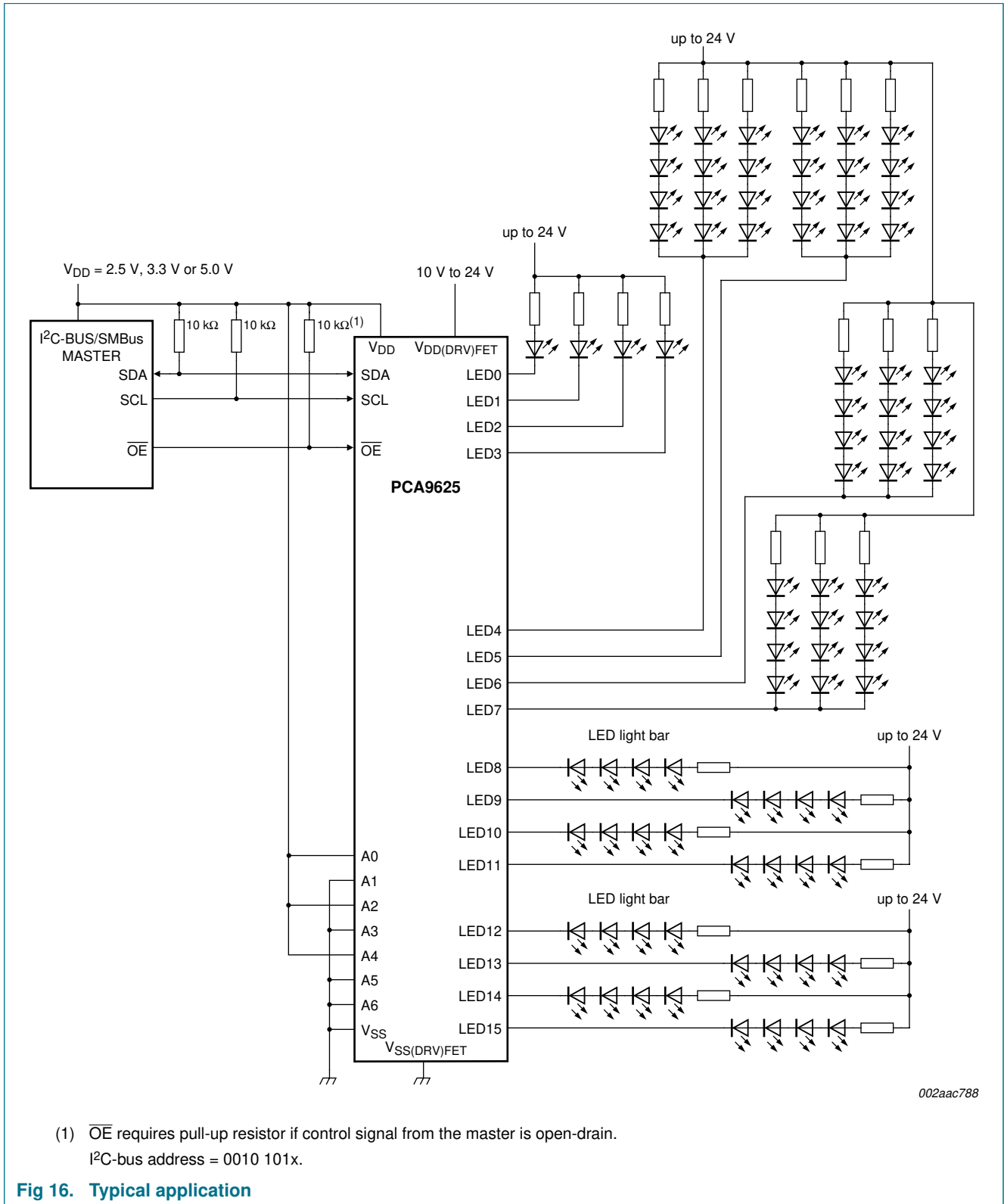
I²C-bus address = 0010 101x.

Fig 16. Typical application

11. Limiting values

Table 13.   Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		V_{SS} − 0.5	5.5	V
$V_{drv(LED)}$	LED driver voltage	[1]	V_{SS} − 0.5	24	V
$V_{DD(DRV)FET}$	FET driver supply voltage	[1]	V_{SS} − 0.5	24	V
$I_{O(LEDn)}$	output current on pin LEDn		-	100	mA
I_{SS}	ground supply current	per $V_{SS(DRV)FET}$ pin	-	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	1.8	W
		T_{amb} = 85 °C	-	0.72	W
P/ch	power dissipation per channel	T_{amb} = 25 °C	-	100	mW
		T_{amb} = 85 °C	-	45	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C

[1]   The $V_{drv(LED)}$ must always be less than or equal to $V_{DD(DRV)FET}$.

12. Thermal characteristics

Table 14.   Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO32	55	°C/W

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13. Static characteristics

Table 15.   Static characteristics
V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
$V_{DD(DRV)FET}$	FET driver supply voltage			10	-	24	V
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	on pin V_{DD} (pin 9); operating mode; no load; f_{SCL} = 1 MHz					
		V_{DD} = 2.3 V		-	2.5	10	mA
		V_{DD} = 3.3 V		-	2.5	10	mA
		V_{DD} = 5.5 V		-	2.5	10	mA
I_{stb}	standby current	on pin V_{DD} (pin 9); no load; f_{SCL} = 0 Hz; I/O = inputs; V_I = V_{DD}					
		V_{DD} = 2.3 V		-	1.3	5	µA
		V_{DD} = 3.3 V		-	1.4	6	µA
		V_{DD} = 5.5 V		-	1.5	7	µA
		on pin $V_{DD(DRV)FET}$ (pin 24 and pin 26)					
		$V_{DD(DRV)FET}$ = 18 V		-	400	1000	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[1]	-	1.70	2.0	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V		20	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V		30	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
LED driver outputs							
$V_{drv(LED)}$	LED driver voltage		[2]	0	-	24	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V	[3]	100	-	-	mA
$I_{OL(tot)}$	total LOW-level output current	V_{OL} = 0.5 V	[3]	1600	-	-	mA
R_{on}	ON-state resistance	$V_{DD(DRV)FET}$ = 10 V; V_{DD} = 2.3 V		-	2	5	Ω
C_o	output capacitance			-	2.5	5	pF
OE input							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance			-	3.7	5	pF

Table 15. Static characteristics *…continued*

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Address inputs						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.7	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] $V_{DD(DRV)FET}$ and $V_{drv(LED)}$ voltages are independent, but $V_{drv(LED)} \leq V_{DD(DRV)FET}$ at all times.

[3] Each bit must be limited to a maximum of 100 mA and the total package limited to 1600 mA due to internal busing limits.

14. Dynamic characteristics

Table 16. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I2C-bus		Fast-mode I2C-bus		Fast-mode Plus I2C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[2]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[3][4]	-	300	20 + 0.1C_b[5]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	20 + 0.1C_b[5]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	-	50	-	50	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[5] C_b = total capacitance of one bus line in pF.

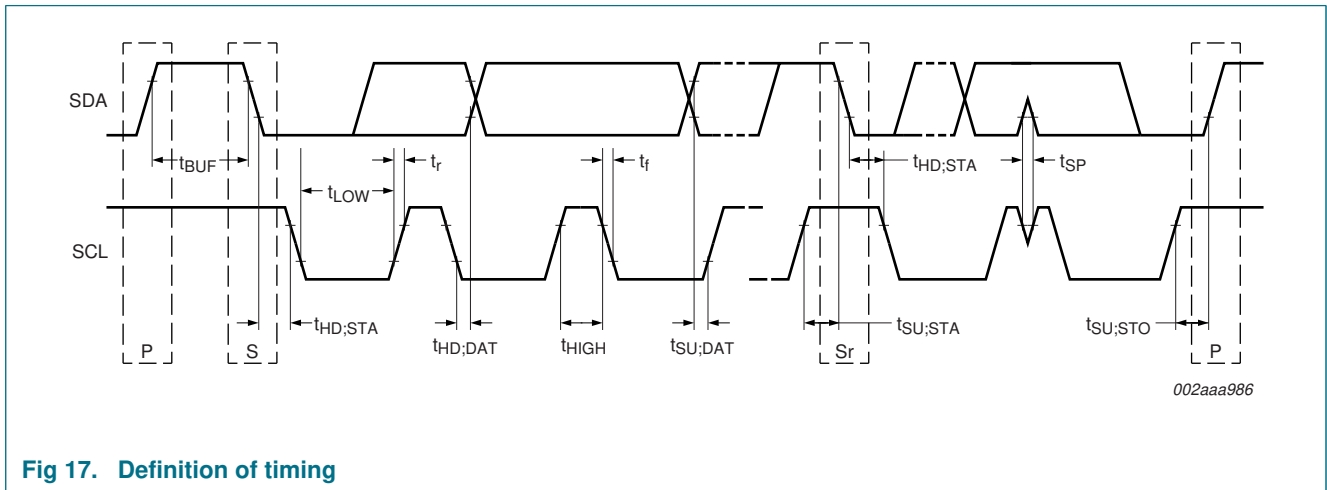[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.
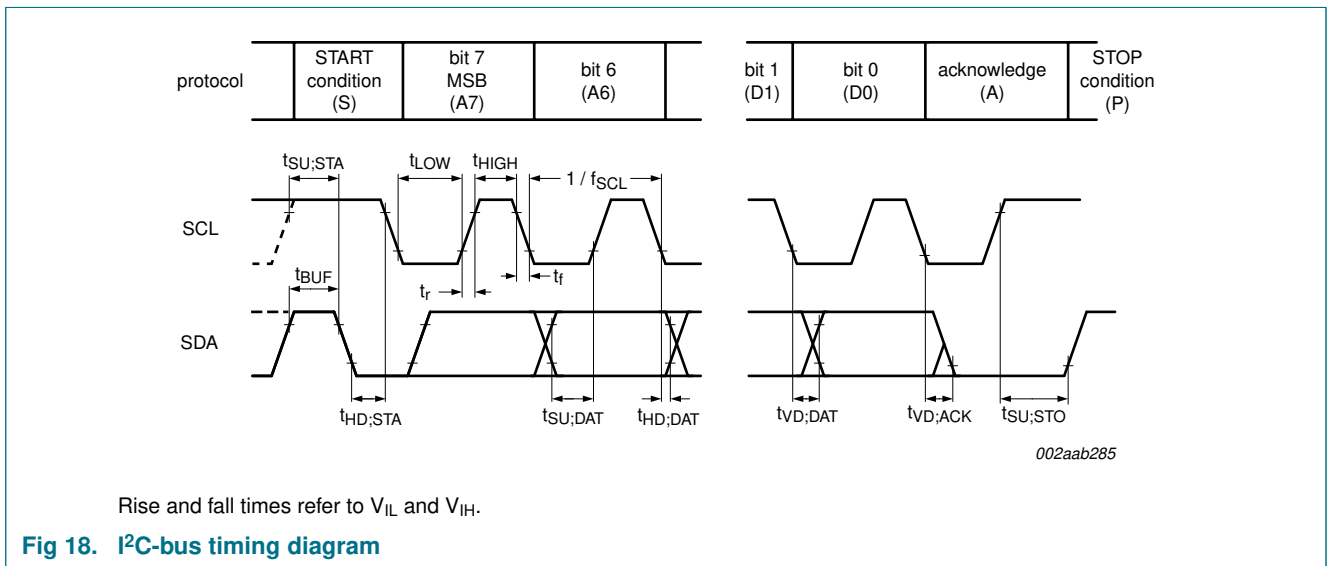

Fig 17. Definition of timing

Rise and fall times refer to V_{IL} and V_{IH}.

Fig 18. I2C-bus timing diagram