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PCA9674; PCA9674A

Remote 8-bit I/O expander for Fm+ I²C-bus with interrupt

Rev. 7 — 30 May 2013 Product data sheet

1. General description

The PCA9674/74A provides general-purpose remote I/O expansion via the two-wire bidirectional I²C-bus (serial clock (SCL), serial data (SDA)).

The devices consist of eight quasi-bidirectional ports, 1 MHz I²C-bus Fast-mode Plus (Fm+) family interface, with high speed data transfer it can support PWM dimming of LEDs, and higher I²C-bus drive 30 mA for more devices can be on the bus without the need for bus buffers. Three hardware address inputs and interrupt output operating between 2.3 V and 5.5 V. The quasi-bidirectional port can be independently assigned as an input to monitor interrupt status or keypads, or as an output to activate indicator devices such as LEDs. The system master can read from the input port or write to the output port through a single register.

The low current consumption of 4.5 μA (typical, static) is great for mobile applications and the latched output ports have 25 mA high current sink drive capability for directly driving LEDs.

The PCA9674 and PCA9674A are identical except for the different, non-overlapping slave address. The three hardware selectable address pins can be decode to 64 addresses for the PCA9674 and 62 addresses for the PCA9674A, so there can be up to 126 of these I/O expanders PCA9674/74A together on the same I²C-bus without the need for bus buffers, supporting up to 1008 I/Os (for example, 1008 LEDs).

The active LOW open-drain interrupt output ($\overline{INT}$) can be connected to the interrupt logic of the microcontroller and is activated when any input state differs from its corresponding input port register state. It is used to indicate to the microcontroller that an input state has changed and the device needs to be interrogated without the microcontroller continuously polling the input register via the I²C-bus.

The internal Power-On Reset (POR) initializes the I/Os as inputs with a weak internal pull-up 100 μA current source.

2. Features and benefits

- I²C-bus to parallel port expander
- 1 MHz I²C-bus interface (Fast-mode Plus I²C-bus)
- SDA with 30 mA sink capability for 4000 pF buses
- Operating supply voltage 2.3 V to 5.5 V with 5.5 V tolerant I/Os held to V_{DD} with 100 μA current source
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 200 mA

- Active LOW open-drain interrupt output
- Sixty-four programmable slave addresses using three address pins (PCA9674A - sixty-two)
- Readable device ID (manufacturer, device type, and revision)
- Software Reset pushes the device back to Power-On Reset state
- Low standby current (4.5 μA typical)
- −40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16, HVQFN16

3. Applications

- LED signs and displays
- Servers
- Key pads
- Industrial control
- Medical equipment
- PLCs
- Cellular telephones
- Mobile devices
- Gaming machines
- Instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9674BS	674	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9674ABS	74A			
PCA9674D	PCA9674D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9674AD	PCA9674AD			
PCA9674PW	PCA9674	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9674APW	9674A			

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9674BS	PCA9674BS,118	HVQFN16	Reel 13” Q1/T1 *standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCA9674ABS	PCA9674ABS,118	HVQFN16	Reel 13” Q1/T1 *standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCA9674D	PCA9674D,512	SO16	Standard marking * tube dry pack	1920	T_{amb} = −40 °C to +85 °C
	PCA9674D,518	SO16	Reel 13” Q1/T1 *standard mark SMD dry pack	1000	T_{amb} = −40 °C to +85 °C
PCA9674AD	PCA9674AD,512	SO16	Standard marking * tube dry pack	1920	T_{amb} = −40 °C to +85 °C
	PCA9674AD,518	SO16	Reel 13” Q1/T1 *standard mark SMD dry pack	1000	T_{amb} = −40 °C to +85 °C
PCA9674PW	PCA9674PW,112	TSSOP16	Standard marking * IC’s tube - DSC bulk pack	2400	T_{amb} = −40 °C to +85 °C
	PCA9674PW,118	TSSOP16	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9674APW	PCA9674APW,112	TSSOP16	Standard marking * IC’s tube - DSC bulk pack	2400	T_{amb} = −40 °C to +85 °C
	PCA9674APW,118	TSSOP16	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

5. Block diagram

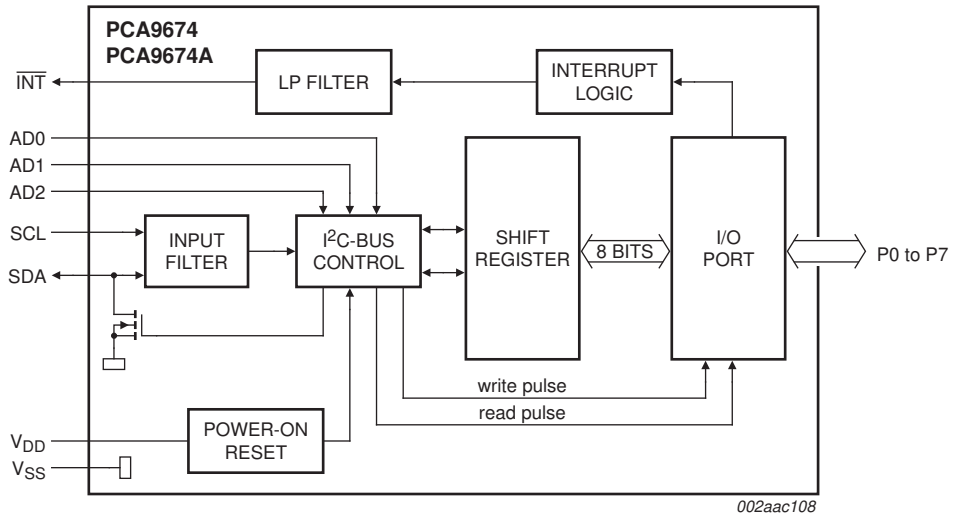


Fig 1. Block diagram of PCA9674; PCA9674A

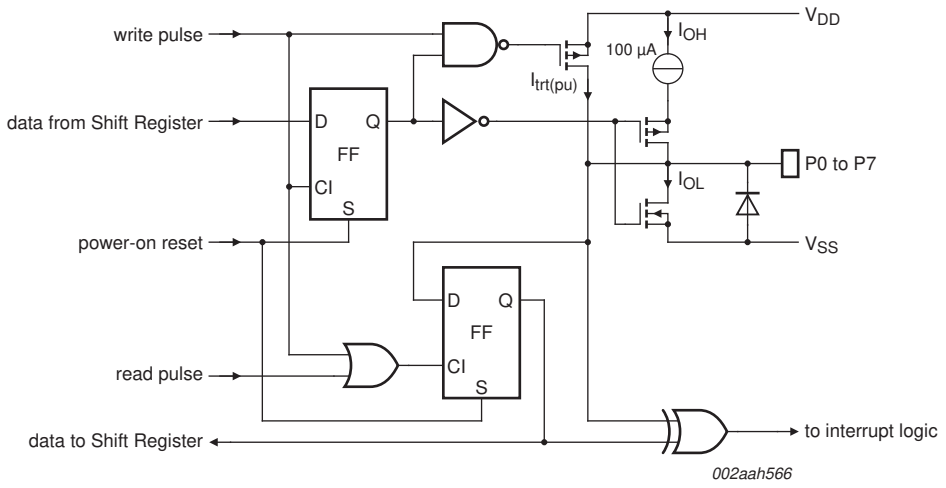


Fig 2. Simplified schematic diagram of P0 to P7

6. Pinning information

6.1 Pinning

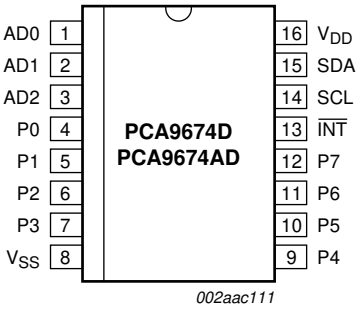


Fig 3. Pin configuration for SO16

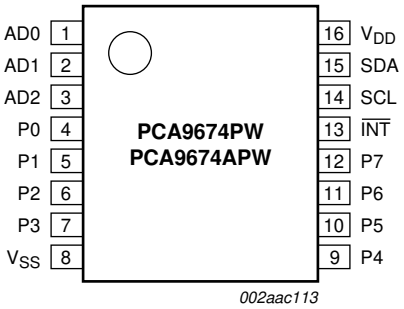


Fig 4. Pin configuration for TSSOP16

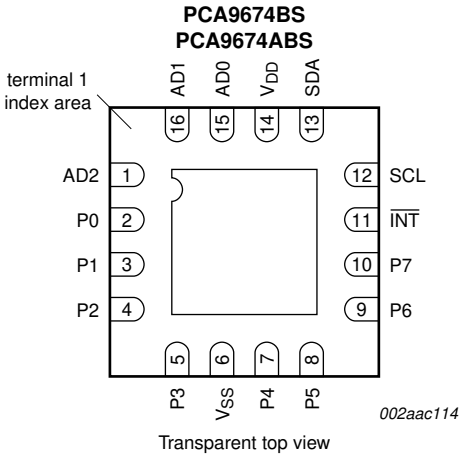


Fig 5. Pin configuration for HVQFN16

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
AD0	1	15	address input 0
AD1	2	16	address input 1
AD2	3	1	address input 2
P0	4	2	quasi-bidirectional I/O 0
P1	5	3	quasi-bidirectional I/O 1
P2	6	4	quasi-bidirectional I/O 2
P3	7	5	quasi-bidirectional I/O 3
V_{SS}	8	6[1]	supply ground
P4	9	7	quasi-bidirectional I/O 4

Table 3. Pin description *...continued*

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
P5	10	8	quasi-bidirectional I/O 5
P6	11	9	quasi-bidirectional I/O 6
P7	12	10	quasi-bidirectional I/O 7
$\overline{INT}$	13	11	interrupt output (active LOW)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V_{DD}	16	14	supply voltage

[1] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCA9674; PCA9674A”.

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address format of the PCA9674/PCA9674A is shown in Figure 6. Slave address pins AD2, AD1, and AD0 are used to choose 1 of 64 slave addresses. These devices can monitor the change in SDA or SCL in addition to the static levels of V_{DD} or V_{SS} to decode four states allowing a larger address range. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1 or AD0 so they must be externally connected to V_{DD}, V_{SS} directly or through resistors, or directly to SCL or SDA. The address values depending on AD2, AD1 and AD0 can be found in Table 4 “PCA9674 address map” and Table 5 “PCA9674A address map”.

Remark: When using the PCA9674A, the General Call address (0000 0000b) and the Device ID address (1111 100Xb) are reserved and cannot be used as device address. Failure to follow this requirement will cause the PCA9674A not to acknowledge.

Remark: When using the PCA9674 or the PCA9674A, reserved I²C-bus addresses must be used with caution since they can interfere with:

- “reserved for future use” I²C-bus addresses (0000 011, 1111 101, 1111 110, 1111 111)
- slave devices that use the 10-bit addressing scheme (1111 0xx)
- High speed mode (Hs-mode) master code (0000 1xx)

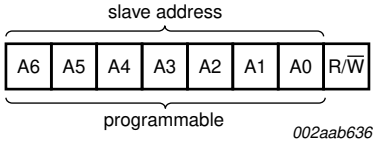


Fig 6. PCA9674; PCA9674A address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

When AD2, AD1 and AD0 are held to V_{DD} or V_{SS}, the same address as the PCF8574 or PCF8574A or the newer PCA8574 or PCA8574A is applied.

7.1.1 Address maps

The PCA9674 and PCA9674A are functionally the same, but have non-overlapping address ranges. This allows 64 of the PCA9674 devices and 62 of the PCA9674A devices to be on the same I²C-bus without address conflict.

Table 4. PCA9674 address map

Pin connectivity			Address of PCA9674								Address byte value		7-bit hexadecimal address without R/W
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
V_{SS}	SCL	V_{SS}	0	0	1	0	0	0	0	-	20h	21h	10h
V_{SS}	SCL	V_{DD}	0	0	1	0	0	0	1	-	22h	23h	11h
V_{SS}	SDA	V_{SS}	0	0	1	0	0	1	0	-	24h	25h	12h
V_{SS}	SDA	V_{DD}	0	0	1	0	0	1	1	-	26h	27h	13h
V_{DD}	SCL	V_{SS}	0	0	1	0	1	0	0	-	28h	29h	14h
V_{DD}	SCL	V_{DD}	0	0	1	0	1	0	1	-	2Ah	2Bh	15h
V_{DD}	SDA	V_{SS}	0	0	1	0	1	1	0	-	2Ch	2Dh	16h
V_{DD}	SDA	V_{DD}	0	0	1	0	1	1	1	-	2Eh	2Fh	17h
V_{SS}	SCL	SCL	0	0	1	1	0	0	0	-	30h	31h	18h
V_{SS}	SCL	SDA	0	0	1	1	0	0	1	-	32h	33h	19h
V_{SS}	SDA	SCL	0	0	1	1	0	1	0	-	34h	35h	1Ah
V_{SS}	SDA	SDA	0	0	1	1	0	1	1	-	36h	37h	1Bh
V_{DD}	SCL	SCL	0	0	1	1	1	0	0	-	38h	39h	1Ch
V_{DD}	SCL	SDA	0	0	1	1	1	0	1	-	3Ah	3Bh	1Dh
V_{DD}	SDA	SCL	0	0	1	1	1	1	0	-	3Ch	3Dh	1Eh
V_{DD}	SDA	SDA	0	0	1	1	1	1	1	-	3Eh	3Fh	1Fh
V_{SS}	V_{SS}	V_{SS}	0	1	0	0	0	0	0	-	40h	41h	20h
V_{SS}	V_{SS}	V_{DD}	0	1	0	0	0	0	1	-	42h	43h	21h
V_{SS}	V_{DD}	V_{SS}	0	1	0	0	0	1	0	-	44h	45h	22h
V_{SS}	V_{DD}	V_{DD}	0	1	0	0	0	1	1	-	46h	47h	23h
V_{DD}	V_{SS}	V_{SS}	0	1	0	0	1	0	0	-	48h	49h	24h
V_{DD}	V_{SS}	V_{DD}	0	1	0	0	1	0	1	-	4Ah	4Bh	25h
V_{DD}	V_{DD}	V_{SS}	0	1	0	0	1	1	0	-	4Ch	4Dh	26h

Table 4. PCA9674 address map *…continued*

Pin connectivity			Address of PCA9674								Address byte value		7-bit hexadecimal address without R/W
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
V_{DD}	V_{DD}	V_{DD}	0	1	0	0	1	1	1	-	4Eh	4Fh	27h
V_{SS}	V_{SS}	SCL	0	1	0	1	0	0	0	-	50h	51h	28h
V_{SS}	V_{SS}	SDA	0	1	0	1	0	0	1	-	52h	53h	29h
V_{SS}	V_{DD}	SCL	0	1	0	1	0	1	0	-	54h	55h	2Ah
V_{SS}	V_{DD}	SDA	0	1	0	1	0	1	1	-	56h	57h	2Bh
V_{DD}	V_{SS}	SCL	0	1	0	1	1	0	0	-	58h	59h	2Ch
V_{DD}	V_{SS}	SDA	0	1	0	1	1	0	1	-	5Ah	5Bh	2Dh
V_{DD}	V_{DD}	SCL	0	1	0	1	1	1	0	-	5Ch	5Dh	2Eh
V_{DD}	V_{DD}	SDA	0	1	0	1	1	1	1	-	5Eh	5Fh	2Fh
SCL	SCL	V_{SS}	1	0	1	0	0	0	0	-	A0h	A1h	50h
SCL	SCL	V_{DD}	1	0	1	0	0	0	1	-	A2h	A3h	51h
SCL	SDA	V_{SS}	1	0	1	0	0	1	0	-	A4h	A5h	52h
SCL	SDA	V_{DD}	1	0	1	0	0	1	1	-	A6h	A7h	53h
SDA	SCL	V_{SS}	1	0	1	0	1	0	0	-	A8h	A9h	54h
SDA	SCL	V_{DD}	1	0	1	0	1	0	1	-	AAh	ABh	55h
SDA	SDA	V_{SS}	1	0	1	0	1	1	0	-	ACh	ADh	56h
SDA	SDA	V_{DD}	1	0	1	0	1	1	1	-	AEh	AFh	57h
SCL	SCL	SCL	1	0	1	1	0	0	0	-	B0h	B1h	58h
SCL	SCL	SDA	1	0	1	1	0	0	1	-	B2h	B3h	59h
SCL	SDA	SCL	1	0	1	1	0	1	0	-	B4h	B5h	5Ah
SCL	SDA	SDA	1	0	1	1	0	1	1	-	B6h	B7h	5Bh
SDA	SCL	SCL	1	0	1	1	1	0	0	-	B8h	B9h	5Ch
SDA	SCL	SDA	1	0	1	1	1	0	1	-	BAh	BBh	5Dh
SDA	SDA	SCL	1	0	1	1	1	1	0	-	BCh	BDh	5Eh
SDA	SDA	SDA	1	0	1	1	1	1	1	-	BEh	BFh	5Fh
SCL	V_{SS}	V_{SS}	1	1	0	0	0	0	0	-	C0h	C1h	60h
SCL	V_{SS}	V_{DD}	1	1	0	0	0	0	1	-	C2h	C3h	61h
SCL	V_{DD}	V_{SS}	1	1	0	0	0	1	0	-	C4h	C5h	62h
SCL	V_{DD}	V_{DD}	1	1	0	0	0	1	1	-	C6h	C7h	63h
SDA	V_{SS}	V_{SS}	1	1	0	0	1	0	0	-	C8h	C9h	64h
SDA	V_{SS}	V_{DD}	1	1	0	0	1	0	1	-	CAh	CBh	65h
SDA	V_{DD}	V_{SS}	1	1	0	0	1	1	0	-	CCh	CDh	66h
SDA	V_{DD}	V_{DD}	1	1	0	0	1	1	1	-	CEh	CFh	67h
SCL	V_{SS}	SCL	1	1	1	0	0	0	0	-	E0h	E1h	70h
SCL	V_{SS}	SDA	1	1	1	0	0	0	1	-	E2h	E3h	71h
SCL	V_{DD}	SCL	1	1	1	0	0	1	0	-	E4h	E5h	72h
SCL	V_{DD}	SDA	1	1	1	0	0	1	1	-	E6h	E7h	73h
SDA	V_{SS}	SCL	1	1	1	0	1	0	0	-	E8h	E9h	74h

Table 4. PCA9674 address map *…continued*

Pin connectivity			Address of PCA9674								Address byte value		7-bit hexadecimal address without R/W
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
SDA	V_{SS}	SDA	1	1	1	0	1	0	1	-	EAh	EBh	75h
SDA	V_{DD}	SCL	1	1	1	0	1	1	0	-	ECh	EDh	76h
SDA	V_{DD}	SDA	1	1	1	0	1	1	1	-	EEh	EFh	77h

Table 5. PCA9674A address map

Pin connectivity			Address of PCA9674A								Address byte value		7-bit hexadecimal address without R/W
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
V_{SS}	SCL	V_{SS}	0	0	0	1	0	0	0	-	10h	11h	08h
V_{SS}	SCL	V_{DD}	0	0	0	1	0	0	1	-	12h	13h	09h
V_{SS}	SDA	V_{SS}	0	0	0	1	0	1	0	-	14h	15h	0Ah
V_{SS}	SDA	V_{DD}	0	0	0	1	0	1	1	-	16h	17h	0Bh
V_{DD}	SCL	V_{SS}	0	0	0	1	1	0	0	-	18h	19h	0Ch
V_{DD}	SCL	V_{DD}	0	0	0	1	1	0	1	-	1Ah	1Bh	0Dh
V_{DD}	SDA	V_{SS}	0	0	0	1	1	1	0	-	1Ch	1Dh	0Eh
V_{DD}	SDA	V_{DD}	0	0	0	1	1	1	1	-	1Eh	1Fh	0Fh
V_{SS}	SCL	SCL	0	1	1	0	0	0	0	-	60h	61h	30h
V_{SS}	SCL	SDA	0	1	1	0	0	0	1	-	62h	63h	31h
V_{SS}	SDA	SCL	0	1	1	0	0	1	0	-	64h	65h	32h
V_{SS}	SDA	SDA	0	1	1	0	0	1	1	-	66h	67h	33h
V_{DD}	SCL	SCL	0	1	1	0	1	0	0	-	68h	69h	34h
V_{DD}	SCL	SDA	0	1	1	0	1	0	1	-	6Ah	6Bh	35h
V_{DD}	SDA	SCL	0	1	1	0	1	1	0	-	6Ch	6Dh	36h
V_{DD}	SDA	SDA	0	1	1	0	1	1	1	-	6Eh	6Fh	37h
V_{SS}	V_{SS}	V_{SS}	0	1	1	1	0	0	0	-	70h	71h	38h
V_{SS}	V_{SS}	V_{DD}	0	1	1	1	0	0	1	-	72h	73h	39h
V_{SS}	V_{DD}	V_{SS}	0	1	1	1	0	1	0	-	74h	75h	3Ah
V_{SS}	V_{DD}	V_{DD}	0	1	1	1	0	1	1	-	76h	77h	3Bh
V_{DD}	V_{SS}	V_{SS}	0	1	1	1	1	0	0	-	78h	79h	3Ch
V_{DD}	V_{SS}	V_{DD}	0	1	1	1	1	0	1	-	7Ah	7Bh	3Dh
V_{DD}	V_{DD}	V_{SS}	0	1	1	1	1	1	0	-	7Ch	7Dh	3Eh
V_{DD}	V_{DD}	V_{DD}	0	1	1	1	1	1	1	-	7Eh	7Fh	3Fh
V_{SS}	V_{SS}	SCL	1	0	0	0	0	0	0	-	80h	81h	40h
V_{SS}	V_{SS}	SDA	1	0	0	0	0	0	1	-	82h	83h	41h
V_{SS}	V_{DD}	SCL	1	0	0	0	0	1	0	-	84h	85h	42h
V_{SS}	V_{DD}	SDA	1	0	0	0	0	1	1	-	86h	87h	43h
V_{DD}	V_{SS}	SCL	1	0	0	0	1	0	0	-	88h	89h	44h
V_{DD}	V_{SS}	SDA	1	0	0	0	1	0	1	-	8Ah	8Bh	45h

Table 5. PCA9674A address map *…continued*

Pin connectivity			Address of PCA9674A								Address byte value		7-bit hexadecimal address without R/W
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
V_{DD}	V_{DD}	SCL	1	0	0	0	1	1	0	-	8Ch	8Dh	46h
V_{DD}	V_{DD}	SDA	1	0	0	0	1	1	1	-	8Eh	8Fh	47h
SCL	SCL	V_{SS}	1	0	0	1	0	0	0	-	90h	91h	48h
SCL	SCL	V_{DD}	1	0	0	1	0	0	1	-	92h	93h	49h
SCL	SDA	V_{SS}	1	0	0	1	0	1	0	-	94h	95h	4Ah
SCL	SDA	V_{DD}	1	0	0	1	0	1	1	-	96h	97h	4Bh
SDA	SCL	V_{SS}	1	0	0	1	1	0	0	-	98h	99h	4Ch
SDA	SCL	V_{DD}	1	0	0	1	1	0	1	-	9Ah	9Bh	4Dh
SDA	SDA	V_{SS}	1	0	0	1	1	1	0	-	9Ch	9Dh	4Eh
SDA	SDA	V_{DD}	1	0	0	1	1	1	1	-	9Eh	9Fh	4Fh
SCL	SCL	SCL	1	1	0	1	0	0	0	-	D0h	D1h	68h
SCL	SCL	SDA	1	1	0	1	0	0	1	-	D2h	D3h	69h
SCL	SDA	SCL	1	1	0	1	0	1	0	-	D4h	D5h	6Ah
SCL	SDA	SDA	1	1	0	1	0	1	1	-	D6h	D7h	6Bh
SDA	SCL	SCL	1	1	0	1	1	0	0	-	D8h	D9h	6Ch
SDA	SCL	SDA	1	1	0	1	1	0	1	-	DAh	DBh	6Dh
SDA	SDA	SCL	1	1	0	1	1	1	0	-	DCh	DDh	6Eh
SDA	SDA	SDA	1	1	0	1	1	1	1	-	DEh	DFh	6Fh
SCL	V_{SS}	V_{SS}	1	1	1	1	0	0	0	-	F0h	F1h	78h
SCL	V_{SS}	V_{DD}	1	1	1	1	0	0	1	-	F2h	F3h	79h
SCL	V_{DD}	V_{SS}	1	1	1	1	0	1	0	-	F4h	F5h	7Ah
SCL	V_{DD}	V_{DD}	1	1	1	1	0	1	1	-	F6h	F7h	7Bh
SDA	V_{SS}	V_{SS}	1	1	1	1	1	0	0	-	F8h[1]	F9h[1]	7Ch[1]
SDA	V_{SS}	V_{DD}	1	1	1	1	1	0	1	-	FAh	FBh	7Dh
SDA	V_{DD}	V_{SS}	1	1	1	1	1	1	0	-	FCh	FDh	7Eh
SDA	V_{DD}	V_{DD}	1	1	1	1	1	1	1	-	FEh	FFh	7Fh
SCL	V_{SS}	SCL	0	0	0	0	0	0	0	-	00h[1]	01h[1]	00h[1]
SCL	V_{SS}	SDA	0	0	0	0	0	0	1	-	02h	03h	01h
SCL	V_{DD}	SCL	0	0	0	0	0	1	0	-	04h	05h	02h
SCL	V_{DD}	SDA	0	0	0	0	0	1	1	-	06h	07h	03h
SDA	V_{SS}	SCL	0	0	0	0	1	0	0	-	08h	09h	04h
SDA	V_{SS}	SDA	0	0	0	0	1	0	1	-	0Ah	0Bh	05h
SDA	V_{DD}	SCL	0	0	0	0	1	1	0	-	0Ch	0Dh	06h
SDA	V_{DD}	SDA	0	0	0	0	1	1	1	-	0Eh	0Fh	07h

[1] The PCA9674A does not acknowledge when AD2, AD1, AD0 follows this configuration.

7.2 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the PCA9674; PCA9674A.

- General Call address: allows to reset the PCA9674; PCA9674A through the I²C-bus upon reception of the right I²C-bus sequence. See Section 7.2.1 “Software Reset” for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See Section 7.2.2 “Device ID (PCA9674; PCA9674A ID field)” for more information.

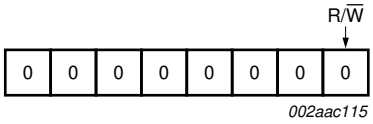


Fig 7. General Call address

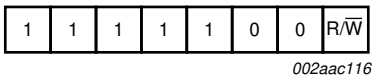


Fig 8. Device ID address

7.2.1 Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address ‘0000 000’ with the R/$\overline{W}$ bit set to 0 (write) is sent by the I²C-bus master.
3. The PCA9674; PCA9674A device(s) acknowledge(s) after seeing the General Call address ‘0000 0000’ (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The PCA9674; PCA9674A acknowledges this value only. If the byte is not equal to 06h, the PCA9674; PCA9674A does not acknowledge it.

   If more than 1 byte of data is sent, the PCA9674; PCA9674A does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the PCA9674; PCA9674A then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the PCA9674; PCA9674A (at any time) as a 'Software Reset Abort'. The PCA9674; PCA9674A does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 9.

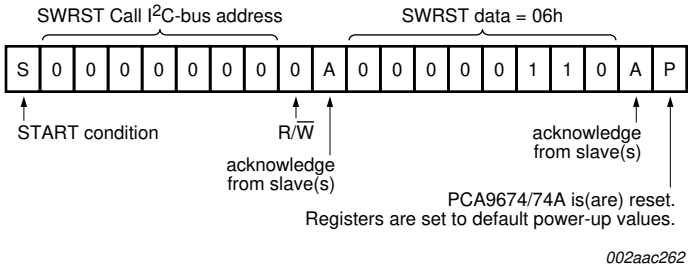


Fig 9. Software Reset sequence

Simple code for Software Reset:

<S> <00h> **<ACK>** <06h> **<ACK>** <P>

7.2.2 Device ID (PCA9674; PCA9674A ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I²C-bus address '1111 100' with the R/$\overline{W}$ bit set to 0 (write).
3. The master sends the I²C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
4. The master sends a Re-START command.

   Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed.

   Remark: A STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID read cannot be performed.
5. The master sends the Reserved Device ID I²C-bus address '1111 100' with the R/$\overline{W}$ bit set to 1 (read).
6. The device ID read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits and then the 3 die revision bits (3 LSB of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

Remark: If the master continues to ACK the bytes after the third byte, the PCA9674; PCA9674A rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCA9674; PCA9674A, the Device ID is as shown in Figure 10.

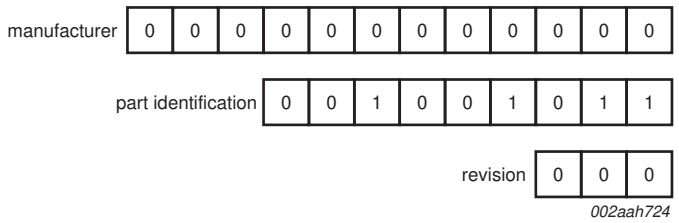
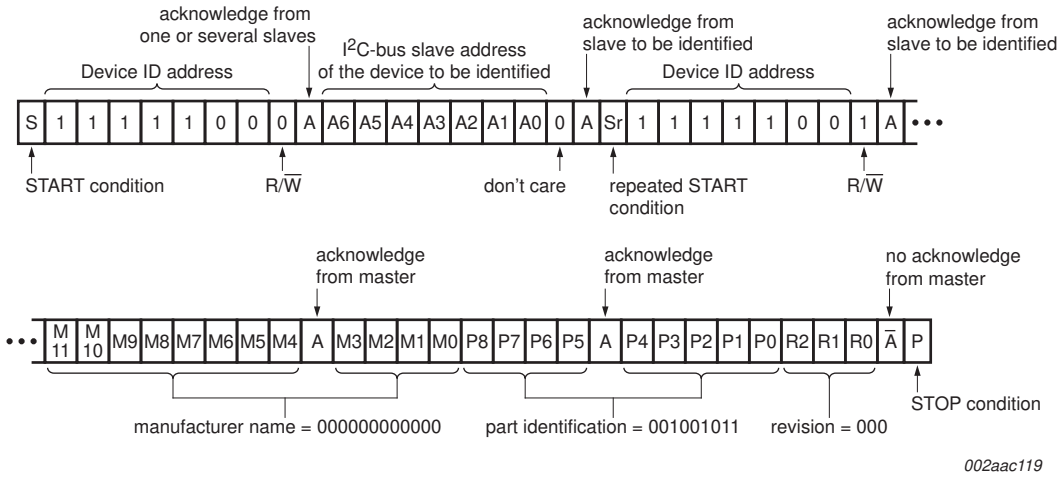


Fig 10. PCA9674; PCA9674A Device ID field



If more than 2 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 11. Device ID field reading

Simple code for reading Device ID:

<S> <F8h> **<ACK>** <slave address> **<ACK>** <SR> <F8h + R> **<ACK>** **<DATA1>** <ACK> **<DATA2>** <ACK> **<DATA3>** <NACK> <P>

8. I/O programming

8.1 Quasi-bidirectional I/Os

A quasi-bidirectional I/O is an input or output port without using a direction control register. Whenever the master reads the register, the value returned to master depends on the actual voltage or status of the pin. At power-on, all the ports are HIGH with a weak 100 μA internal pull-up to V_{DD}, but can be driven LOW by an internal transistor, or an external signal. The I/O ports are entirely independent of each other, but each I/O octal is controlled by the same read or write data byte.

Advantages of the quasi-bidirectional I/O over totem pole I/O include:

- Better for driving LEDs since the p-channel (transistor to V_{DD}) is small, which saves die size and therefore cost. LED drive only requires an internal transistor to ground, while the LED is connected to V_{DD} through a current-limiting resistor. Totem pole I/O have both n-channel and p-channel transistors, which allow solid HIGH and LOW output levels without a pull-up resistor — good for logic levels.
- Simpler architecture — only a single register and the I/O can be both input and output at the same time. Totem pole I/O have a direction register that specifies the port pin direction and it is always in that configuration unless the direction is explicitly changed.
- Does not require a command byte. The simplicity of one register (no need for the pointer register or, technically, the command byte) is an advantage in some embedded systems where every byte counts because of memory or bandwidth limitations.

There is only one register to control four possibilities of the port pin: Input HIGH, input LOW, output HIGH, or output LOW.

Input HIGH: The master needs to write 1 to the register to set the port as an input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin up to V_{DD} or drives logic 1, then the master will read the value of 1.

Input LOW: The master needs to write 1 to the register to set the port to input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin down to V_{SS} or drives logic 0, which sinks the weak 100 μA current source, then the master will read the value of 0.

Output HIGH: The master writes 1 to the register. There is an additional ‘accelerator’ or strong pull-up current when the master sets the port HIGH. The additional strong pull-up is only active during the HIGH time of the acknowledge clock cycle. This accelerator current helps the port’s 100 μA current source make a faster rising edge into a heavily loaded output, but only at the start of the acknowledge clock cycle to avoid bus contention if an external signal is pulling the port LOW to V_{SS}/driving the port with logic 0 at the same time. After the half clock cycle there is only the 100 μA current source to hold the port HIGH.

Output LOW: The master writes 0 to the register. There is a strong current sink transistor that holds the port pin LOW. A large current may flow into the port, which could potentially damage the part if the master writes a 0 to the register and an external source is pulling the port HIGH at the same time.

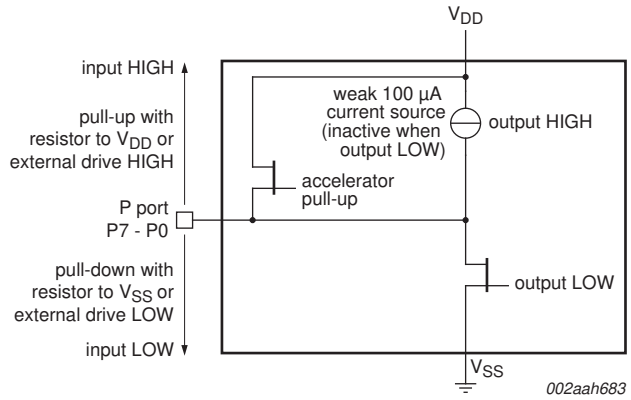


Fig 12. Simple quasi-bidirectional I/O

8.2 Writing to the port (Output mode)

The master (microcontroller) sends the START condition and slave address setting the last bit of the address byte to logic 0 for the write mode. The PCA9674/74A acknowledges and the master then sends the data byte for P7 to P0 to the port register. As the clock line goes HIGH, the 8-bit data is presented on the port lines after it has been acknowledged by the PCA9674/74A. If a LOW is written, the strong pull-down turns on and stays on. If a HIGH is written, the strong pull-up turns on for ½ of the clock cycle, then the line is held HIGH by the weak current source. The master can then send a STOP or ReSTART condition or continue sending data. The number of data bytes that can be sent successively is not limited and the previous data is overwritten every time a data byte has been sent and acknowledged.

Ensure a logic 1 is written for any port that is being used as an input to ensure the strong external pull-down is turned off.

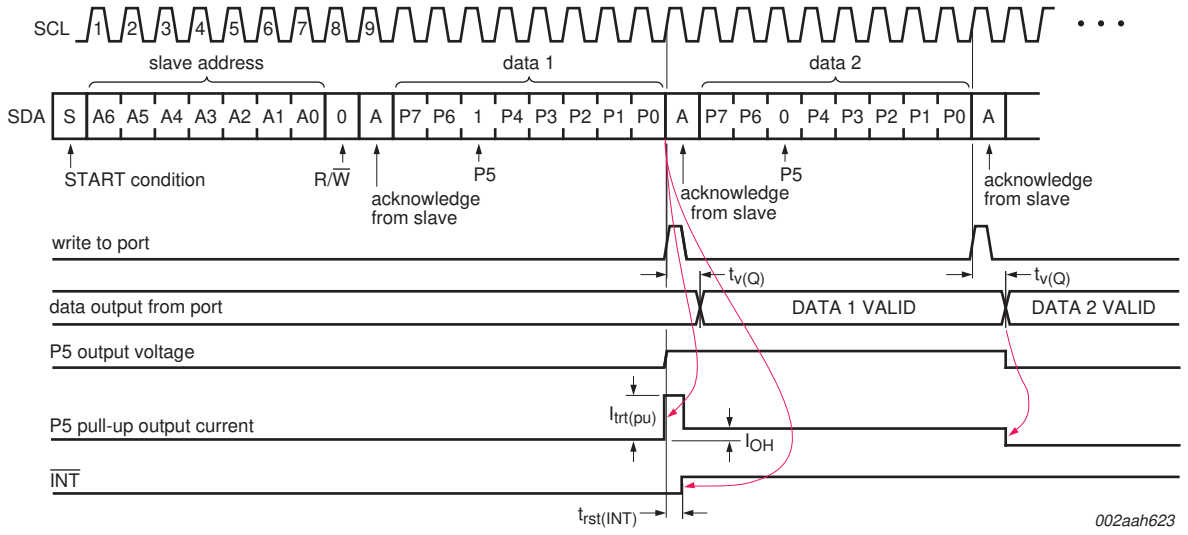


Fig 13. Write mode (output)

Simple code for Write cycle:

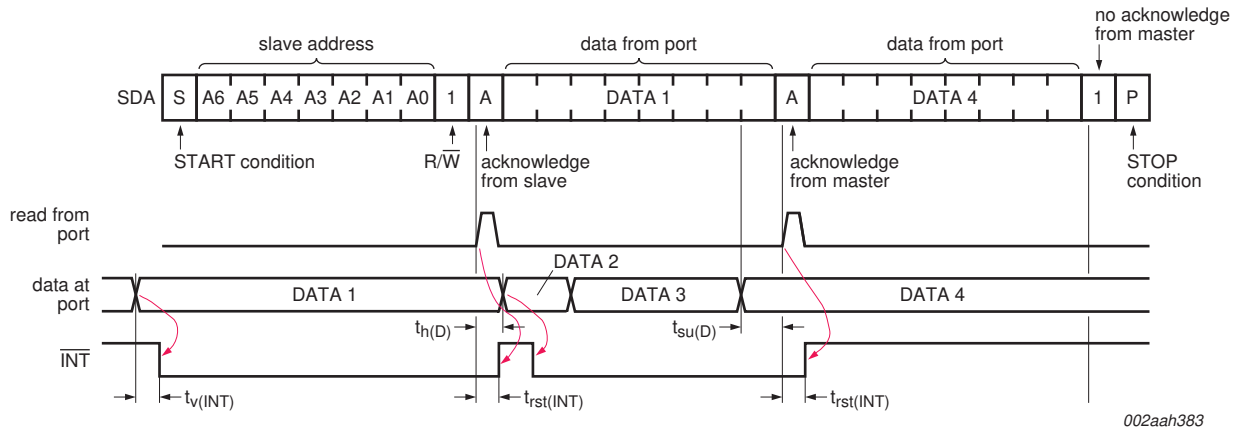
<S> <slave address + W> **<ACK>** <DATA1> **<ACK>** <DATA2> **<ACK>** <DATA1> ... <DATA2> **<ACK>** <P>

8.3 Reading from a port (Input mode)

The port must have been previously written to logic 1, which is the condition after power-on reset or software reset. To enter the Read mode the master (microcontroller) addresses the slave device and sets the last bit of the address byte to logic 1 (address byte read). The slave will acknowledge and then send the data byte to the master. The master will NACK and then send the STOP condition or ACK and read the input register again.

The read of any pin being used as an output will indicate HIGH or LOW depending on the actual state of the pin.

If the data on the input port changes faster than the master can read, this data may be lost. The DATA 2 and DATA 3 are lost because these data did not meet the set-up time and hold time (see Figure 14).



A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (Output mode). Input data is lost.

Fig 14. Read input port register

Simple code for Read cycle:

<S> <slave address + R> **<ACK>** **<DATA in>** <ACK> **<DATA in>** ... <NACK> <P>

8.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9674; PCA9674A in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9674; PCA9674A registers and I²C-bus/SMBus state machine will initialize to their default states of all I/O inputs with weak current source to V_{DD}. Thereafter V_{DD} must be lowered below V_{POR} and back up to the operation voltage for power-on reset cycle.

8.5 Interrupt output ($\overline{INT}$)

The PCA9674/74A provides an open-drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller (see Figure 15). As soon as a port input is changed, the $\overline{INT}$ will be active (LOW) and notify the microcontroller.

An interrupt is generated at any rising or falling edge of the port inputs. After time $t_{v(Q)}$, the signal $\overline{INT}$ is valid.

The interrupt will reset to HIGH when data on the port is changed to the original setting or data is read or written by the master.

In the Write mode, the interrupt may become de-activated (HIGH) on the rising edge of the acknowledge bit of the data byte and also on the rising edge of the write to port pulse. The interrupt will always be reset (HIGH) on the falling edge of the write to port pulse (see Figure 13).

The interrupt is reset (HIGH) in the Read mode on the rising edge of the acknowledge of slave address byte and on the rising edge of the read from port pulse (see Figure 14).

During the interrupt reset, any I/O change close to the read or write pulse may not generate an interrupt, or the interrupt will have a very short pulse. After the interrupt is reset, any change in I/Os will be detected and transmitted as an $\overline{INT}$.

At power-on reset all ports are in Input mode and the initial state of the ports is HIGH, therefore, for any port pin that is pulled LOW or driven LOW by external source, the interrupt output will be active (output LOW).

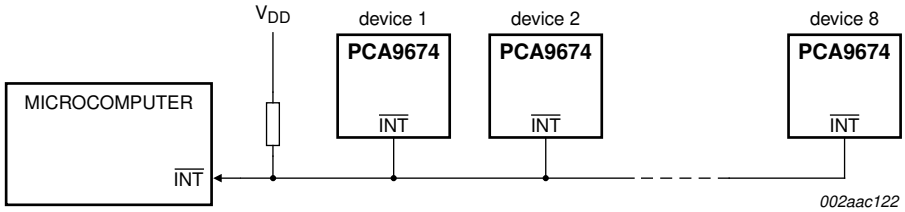


Fig 15. Application of multiple PCA9674s with interrupt

9. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 16).

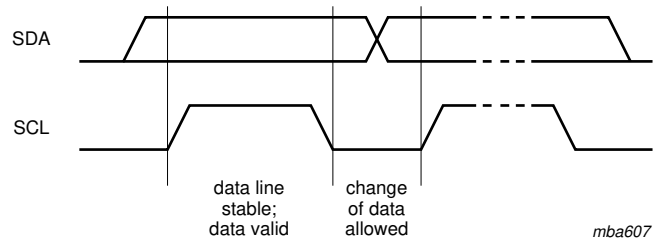


Fig 16. Bit transfer

9.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 17).

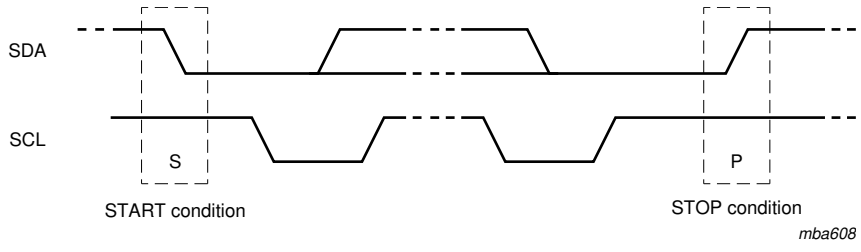


Fig 17. Definition of START and STOP conditions

9.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 18).

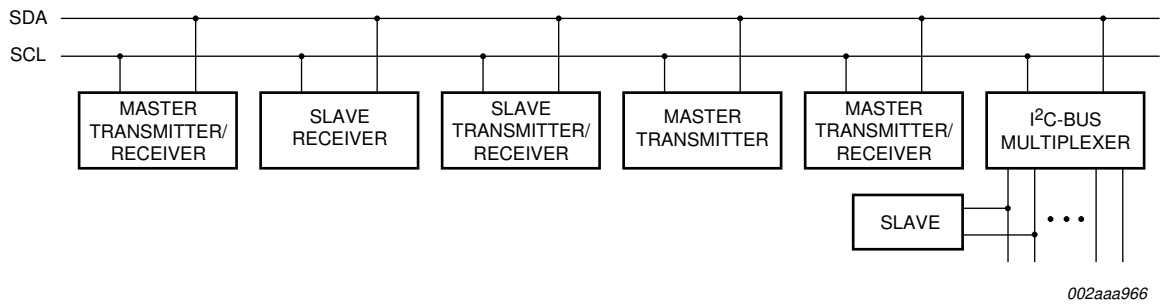


Fig 18. System configuration

9.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Figure 19). The acknowledge bit is an active LOW level (generated by the receiving device) that indicates to the transmitter that the data transfer was successful.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that wants to issue an acknowledge bit has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge bit related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

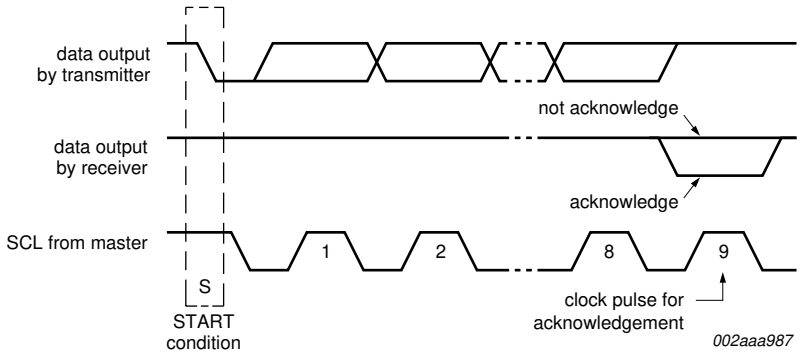


Fig 19. Acknowledgement on the I²C-bus

10. Application design-in information

10.1 Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in Figure 20, P0 and P1 are inputs, and P2 to P7 are outputs. When used in this configuration, during a write, **the input (P0 and P1) must be written as HIGH so the external devices fully control the input ports**. The desired HIGH or LOW logic levels may be written to the ports used as outputs (P2 to P7). If 10 μA internal output HIGH is not enough current source, the port needs external pull-up resistor. During a read, the logic levels of the external devices driving the input ports (P0 and P1) and the previous written logic level to the output ports (P2 to P7) will be read.

The GPIO also has an interrupt line ($\overline{INT}$) that can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there has been a change of data on its ports without having to communicate via the I²C-bus.

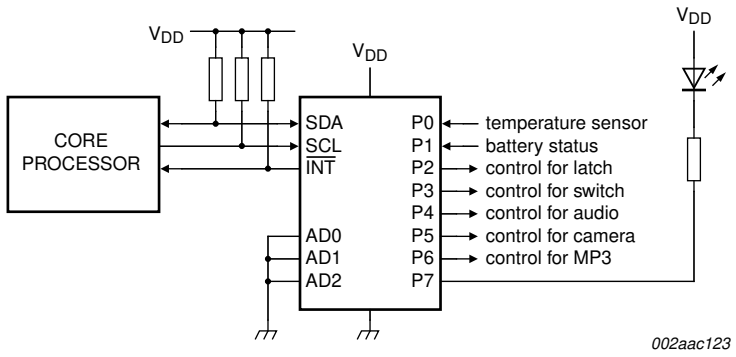


Fig 20. Bidirectional I/O expander application

10.2 How to read and write to I/O expander (example)

In the application example of PCA9674 shown in Figure 20, the microcontroller wants to control the P3 switch ON and the P7 LED ON when the temperature sensor P0 changes.

1. When the system powers on:

   Core Processor needs to issue an initial command to set P0 and P1 as inputs and P[7:2] as outputs with value 1010 00 (LED off, MP3 off, camera on, audio off, switch off and latch off).

2. Operation:

   When the temperature changes above the threshold, the temperature sensor signal will toggle from HIGH to LOW. The $\overline{INT}$ will be activated and notifies the 'core processor' that there have been changes on the input pins. Read the input register. If P0 = 0 (temperature sensor has changed), then turn on LED and turn on switch.

3. Software code:

```
//System Power on
// write to PCA9674 with data 1010 0011b to set P[7:2] outputs and P[1:0] inputs
<S> <0100 0000> <ACK> <1010 0011> <ACK> <P>//Initial setting for PCA9674
```

```
while (INT == 1);  //Monitor the interrupt pin. If INT = 1 do nothing
//When INT = 0 then read input ports
<S> <slave address read> <ACK> <1010 0010> <NACK> <P> //Read PCA9674 data
If (P0 == 0)  //Temperature sensor activated
{
     // write to PCA9674 with data 0010 1011b to turn on LED (P7), on Switch (P3)
      and keep P[1:0] as input ports.
     <S> <0100 0000> <ACK> <0010 1011> <ACK> <P> // Write to PCA9674
}
```

10.3 High current-drive load applications

The GPIO has a minimum guaranteed sinking current of 25 mA per bit at 5 V. In applications requiring additional drive, two port pins may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins can be connected together to drive 200 mA, which is the device recommended total limit. Each pin needs its own limiting resistor as shown in Figure 21 to prevent damage to the device should all ports not be turned on at the same time.

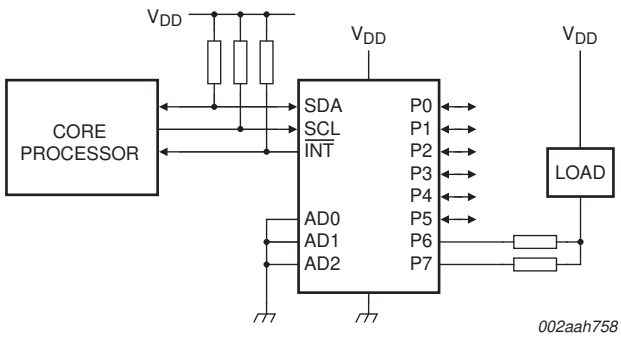


Fig 21. High current-drive load application

10.4 Migration path

NXP offers newer, more capable drop-in replacements for the PCF8574/74A in newer space-saving packages.

Table 6. Migration path

Type number	I²C-bus frequency	Voltage range	Number of addresses per device	Interrupt	Reset	Total package sink current
PCF8574/74A	100 kHz	2.5 V to 6 V	8	yes	no	80 mA
PCA8574/74A	400 kHz	2.3 V to 5.5 V	8	yes	no	200 mA
PCA9674/74A	1 MHz Fm+	2.3 V to 5.5 V	64	yes	no	200 mA
PCA9670	1 MHz Fm+	2.3 V to 5.5 V	64	no	yes	200 mA
PCA9672	1 MHz Fm+	2.3 V to 5.5 V	16	yes	yes	200 mA

PCA9670 replaces interrupt output of the PCA9674 with hardware reset input to retain the maximum number of addresses. PCA9672 replaces address A2 of the PCA9674 with hardware reset input to retain the interrupt, but limit the number of addresses.

11. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6	V
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±400	mA
V_I	input voltage		V_{SS} − 0.5	5.5	V
I_I	input current		-	±20	mA
I_O	output current	[1]	-	±50	mA
P_{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C
$T_{j(max)}$	maximum junction temperature		-	125	°C

[1] Total package (maximum) output current is 400 mA.

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVQFN16 package	40	°C/W
		SO16 package	115	°C/W
		TSSOP16 package	160	°C/W

13. Static characteristics

Table 9. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	Operating mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 1 MHz; AD0, AD1, AD2 = static H or L		-	200	500	μA
I_{stb}	standby current	Standby mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz		-	4.5	10	μA
V_{POR}	power-on reset voltage		[1]	-	1.8	2.0	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V		20	35	-	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V		25	44	-	mA
		V_{OL} = 0.4 V; V_{DD} = 4.5 V		30	57	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$		-	5	10	pF
I/Os; P0 to P7							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V	[2]	12	26	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[2]	17	33	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	25	40	-	mA
$I_{OL(tot)}$	total LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	-	-	200	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{SS}$		−30	−138	−300	μA
$I_{trt(pu)}$	transient boosted pull-up current	$V_{OH} = V_{SS}$; see Figure 13		−0.5	−1.0	-	mA
C_i	input capacitance		[3]	-	2.1	10	pF
C_o	output capacitance		[3]	-	2.1	10	pF
Interrupt $\overline{INT}$ (see Figure 14 and Figure 13)							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3.0	-	-	mA
C_o	output capacitance			-	3	5	pF
Inputs AD0, AD1, AD2							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	μA
C_i	input capacitance			-	3.5	5	pF

[1] The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 200 mA due to internal busing limits.

[3] The value is verified by characterization.

14. Dynamic characteristics

Table 10. Dynamic characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Standard mode I²C-bus		Fast mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	50	450	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[4][5]	-	300	$20 + 0.1C_b$[3]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$[3]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	-	50	-	50	ns
Port timing; $C_L \leq 100$ pF (see Figure 13 and Figure 14)									
$t_{v(Q)}$	data output valid time		-	4	-	4	-	4	µs
$t_{su(D)}$	data input set-up time		0	-	0	-	0	-	µs
$t_{h(D)}$	data input hold time		4	-	4	-	4	-	µs
Interrupt timing; $C_L \leq 100$ pF (see Figure 13 and Figure 14)									
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from port to $\overline{INT}$	-	4	-	4	-	4	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	4	-	4	-	4	µs

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

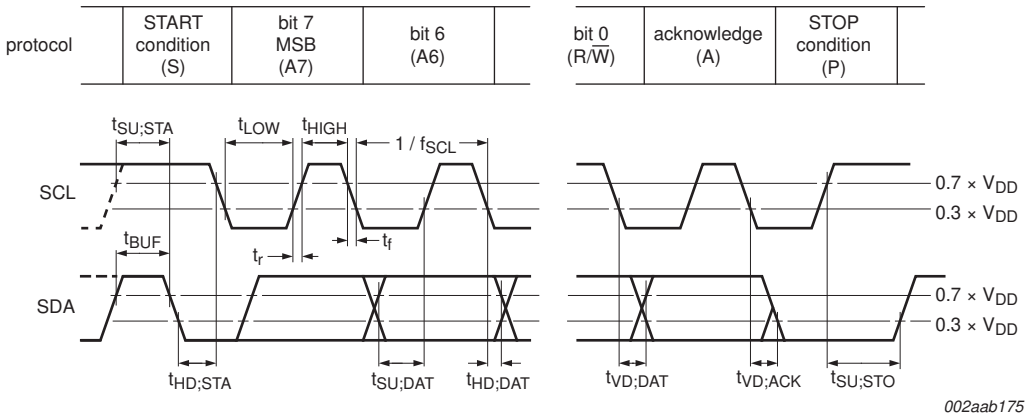
[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

[4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 22. I²C-bus timing diagram