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PCA9745B

16-channel SPI serial bus 57 mA/20 V constant current LED driver

Rev. 1 — 16 June 2016 | Product data sheet

1. General description

The PCA9745B is a daisy-chain SPI-compatible 4-wire serial bus controlled 16-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 100 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCA9745B operates with a supply voltage range of 3 V to 5.5 V and the constant current sink LED outputs allow up to 20 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 225 μA to 57 mA.

Gradation control for all current sources is achieved via the 4-wire serial bus interface and allows user to ramp current automatically without MCU intervention. 8-bit DACs are available to adjust brightness levels for each LED current source. There are four selectable gradation control groups and each group has independently four registers to control ramp-up and ramp-down rate, step time, hold ON/OFF time and final hold ON output current. Two gradation operation modes are available for each group, one is single shot mode (output pattern once) and the other is continuous mode (output pattern repeat). Each channel can be set to either gradation mode or normal mode and assigned to any one of these four gradation control groups.

This device has built-in open, short load and overtemperature detection circuitry. The error information from the corresponding register can be read via the 4-wire serial bus. Additionally, a thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCA9745B device is designed to use 4-wire read/write serial bus with higher data clock frequency (up to 25 MHz).

The active LOW output enable input pin ($\overline{OE}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

2. Features and benefits

- 16 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
  - Programmable LED output delay to reduce EMI and surge currents
- Gradation control for all channels
  - Each channel can assign to one of four gradation control groups
  - Programmable gradation time and rate for ramp-up and/or ramp-down operations
  - Programmable step time (6-bit) from 0.5 ms (minimum) to 512 ms (maximum)
  - Programmable hold-on time after ramp-up and hold-off time after ramp-down (3-bit) from 0 s to 6 s
  - Programmable final ramp-up and hold-on current
  - Programmable brightness current output adjustment, either linear or exponential curve
- 16 constant current output channels can sink up to 57 mA, tolerate up to 20 V when OFF
- Output current adjusted through an external resistor (REXT input)
- Output current accuracy
  - ±4 % between output channels
  - ±6 % between PCA9745B devices
- Open/short load/overtemperature detection mode to detect individual LED errors
- 4-wire serial bus interface with 25 MHz data clock rate
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness fully ON using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDI/SCLK inputs
- No glitch on LEDn outputs on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- –40 °C to +105 °C operation
- ESD protection exceeds 4 kV HBM per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: HTSSOP28

3. Applications

- Amusement products
- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices
- Fade-in and fade-out for breathlight control
- Automotive lighting (PCA9745BTW/Q900)

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9745BTW	PCA9745BTW	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-3
PCA9745BTW/Q900[1]	PCA9745BTW	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-3

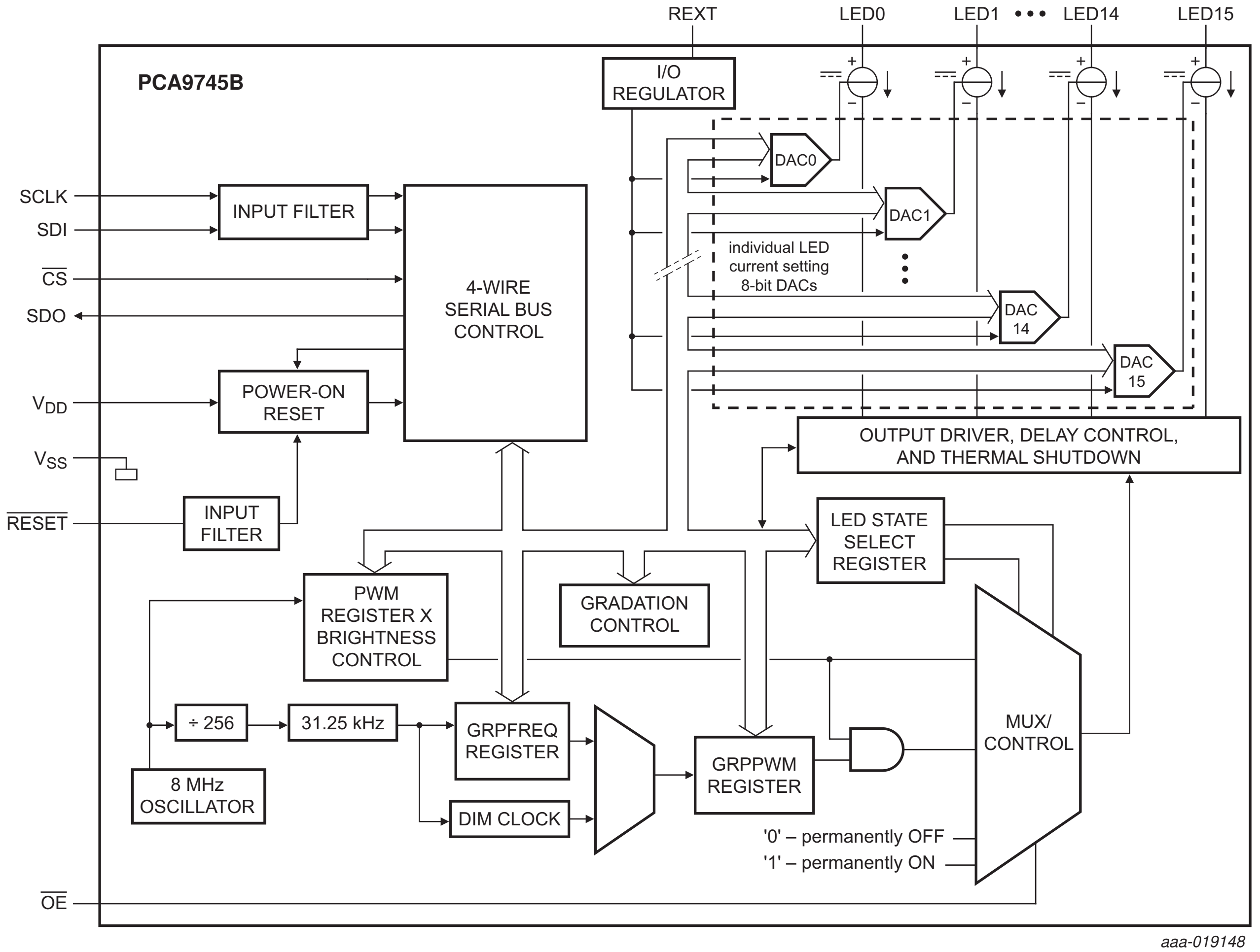
[1] AEC-Q100 compliant.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9745BTW	PCA9745BTWJ	HTSSOP28	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +105 °C
PCA9745BTW/Q900	PCA9745BTW/Q900J	HTSSOP28	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +105 °C

5. Block diagram



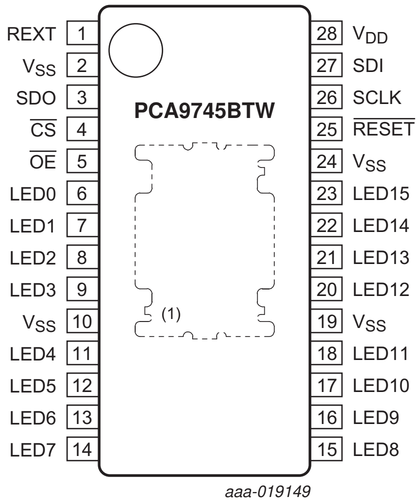
Dim repetition rate = 122 Hz

Blink repetition rate = 15 Hz to every 16.8 seconds

Fig 1. Block diagram of PCA9745B

6. Pinning information

6.1 Pinning



(1) Thermal pad; connected to V_{SS}.

Fig 2. Pin configuration for HTSSOP28

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
SDO	3	O	serial data output
$\overline{CS}$	4	I	active LOW chip select
$\overline{OE}$	5	I	active LOW output enable for LEDs
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	11	O	LED driver 4
LED5	12	O	LED driver 5
LED6	13	O	LED driver 6
LED7	14	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	18	O	LED driver 11
LED12	20	O	LED driver 12
LED13	21	O	LED driver 13

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
LED14	22	O	LED driver 14
LED15	23	O	LED driver 15
$\overline{\text{RESET}}$	25	I	active LOW reset input with external 10 kΩ pull-up resistor
SCLK	26	I	serial clock line
SDI	27	I	serial data input
V_{SS}	2, 10, 19, 24 [1]	ground	supply ground
V_{DD}	28	power supply	supply voltage

[1] HTSSOP28 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 1 "Block diagram of PCA9745B".

7.1 Register address and data

Following a chip select ($\overline{\text{CS}}$) asserted condition (from HIGH to LOW), the data transfers are (16 × n) bits wide (where 'n' is the number of slaves in the chain) with MSB transferred first. The first 7 bits are the address of the register to be accessed. The eighth bit indicates the types of access — read (= 1) or write (= 0). The second group of 8 bits consists of data as shown in Figure 3.

See Section 8 "Characteristics of the 4-wire SPI serial-bus interface" for more detail.

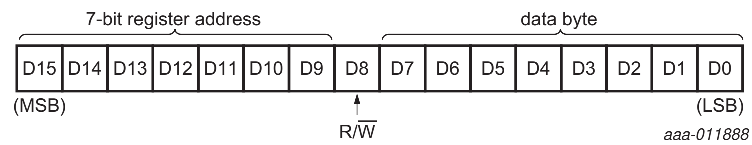


Fig 3. Register address and data format for each slave

7.2 Register definitions

Table 4. Register summary

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	0	0	0	1	0	LEDOUT0	read/write	LED output state 0
03h	0	0	0	0	0	1	1	LEDOUT1	read/write	LED output state 1
04h	0	0	0	0	1	0	0	LEDOUT2	read/write	LED output state 2
05h	0	0	0	0	1	0	1	LEDOUT3	read/write	LED output state 3

Table 4. Register summary *…continued*

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
06h	0	0	0	0	1	1	0	GRPPWM	read/write	group duty cycle control
07h	0	0	0	0	1	1	1	GRPFREQ	read/write	group frequency
08h	0	0	0	1	0	0	0	PWM0	read/write	brightness control LED0
09h	0	0	0	1	0	0	1	PWM1	read/write	brightness control LED1
0Ah	0	0	0	1	0	1	0	PWM2	read/write	brightness control LED2
0Bh	0	0	0	1	0	1	1	PWM3	read/write	brightness control LED3
0Ch	0	0	0	1	1	0	0	PWM4	read/write	brightness control LED4
0Dh	0	0	0	1	1	0	1	PWM5	read/write	brightness control LED5
0Eh	0	0	0	1	1	1	0	PWM6	read/write	brightness control LED6
0Fh	0	0	0	1	1	1	1	PWM7	read/write	brightness control LED7
10h	0	0	1	0	0	0	0	PWM8	read/write	brightness control LED8
11h	0	0	1	0	0	0	1	PWM9	read/write	brightness control LED9
12h	0	0	1	0	0	1	0	PWM10	read/write	brightness control LED10
13h	0	0	1	0	0	1	1	PWM11	read/write	brightness control LED11
14h	0	0	1	0	1	0	0	PWM12	read/write	brightness control LED12
15h	0	0	1	0	1	0	1	PWM13	read/write	brightness control LED13
16h	0	0	1	0	1	1	0	PWM14	read/write	brightness control LED14
17h	0	0	1	0	1	1	1	PWM15	read/write	brightness control LED15
18h	0	0	1	1	0	0	0	IREF0	read/write	output gain control register 0
19h	0	0	1	1	0	0	1	IREF1	read/write	output gain control register 1
1Ah	0	0	1	1	0	1	0	IREF2	read/write	output gain control register 2
1Bh	0	0	1	1	0	1	1	IREF3	read/write	output gain control register 3
1Ch	0	0	1	1	1	0	0	IREF4	read/write	output gain control register 4
1Dh	0	0	1	1	1	0	1	IREF5	read/write	output gain control register 5
1Eh	0	0	1	1	1	1	0	IREF6	read/write	output gain control register 6
1Fh	0	0	1	1	1	1	1	IREF7	read/write	output gain control register 7
20h	0	1	0	0	0	0	0	IREF8	read/write	output gain control register 8
21h	0	1	0	0	0	0	1	IREF9	read/write	output gain control register 9
22h	0	1	0	0	0	1	0	IREF10	read/write	output gain control register 10
23h	0	1	0	0	0	1	1	IREF11	read/write	output gain control register 11
24h	0	1	0	0	1	0	0	IREF12	read/write	output gain control register 12
25h	0	1	0	0	1	0	1	IREF13	read/write	output gain control register 13
26h	0	1	0	0	1	1	0	IREF14	read/write	output gain control register 14
27h	0	1	0	0	1	1	1	IREF15	read/write	output gain control register 15
28h	0	1	0	1	0	0	0	RAMP_RATE_GRP0	read/write	ramp enable and rate control for group 0
29h	0	1	0	1	0	0	1	STEP_TIME_GRP0	read/write	step time control for group 0
2Ah	0	1	0	1	0	1	0	HOLD_CNTL_GRP0	read/write	hold ON/OFF time control for group 0
2Bh	0	1	0	1	0	1	1	IREF_GRP0	read/write	output gain control for group 0

Table 4. Register summary *…continued*

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
2Ch	0	1	0	1	1	0	0	RAMP_RATE_GRP1	read/write	ramp enable and rate control for group 1
2Dh	0	1	0	1	1	0	1	STEP_TIME_GRP1	read/write	step time control for group 1
2Eh	0	1	0	1	1	1	0	HOLD_CNTL_GRP1	read/write	hold ON/OFF time control for group 1
2Fh	0	1	0	1	1	1	1	IREF_GRP1	read/write	output gain control for group 1
30h	0	1	1	0	0	0	0	RAMP_RATE_GRP2	read/write	ramp enable and rate control for group 2
31h	0	1	1	0	0	0	1	STEP_TIME_GRP2	read/write	step time control for group 2
32h	0	1	1	0	0	1	0	HOLD_CNTL_GRP2	read/write	hold ON/OFF time control for group 2
33h	0	1	1	0	0	1	1	IREF_GRP2	read/write	output gain control for group 2
34h	0	1	1	0	1	0	0	RAMP_RATE_GRP3	read/write	ramp enable and rate control for group 3
35h	0	1	1	0	1	0	1	STEP_TIME_GRP3	read/write	step time control for group 3
36h	0	1	1	0	1	1	0	HOLD_CNTL_GRP3	read/write	hold ON/OFF time control for group 3
37h	0	1	1	0	1	1	1	IREF_GRP3	read/write	output gain control for group 3
38h	0	1	1	1	0	0	0	GRAD_MODE_SEL0	read/write	gradation mode select register for channel 7 to channel 0
39h	0	1	1	1	0	0	1	GRAD_MODE_SEL1	read/write	gradation mode select register for channel 15 to channel 8
3Ah	0	1	1	1	0	1	0	GRAD_GRP_SEL0	read/write	gradation group select for channel 3 to channel 0
3Bh	0	1	1	1	0	1	1	GRAD_GRP_SEL1	read/write	gradation group select for channel 7 to channel 4
3Ch	0	1	1	1	1	0	0	GRAD_GRP_SEL2	read/write	gradation group select for channel 11 to channel 8
3Dh	0	1	1	1	1	0	1	GRAD_GRP_SEL3	read/write	gradation group select for channel 15 to channel 12
3Eh	0	1	1	1	1	1	0	GRAD_CNTL	read/write	gradation control register for all four groups
3Fh	0	1	1	1	1	1	1	OFFSET	read/write	Offset/delay on LEDn outputs
40h	1	0	0	0	0	0	0	PWMALL	write only	brightness control for all LEDn
41h	1	0	0	0	0	0	1	IREFALL	write only	output gain control for all registers IREF0 to IREF15
42h	1	0	0	0	0	1	0	EFLAG0	read only	output error flag 0
43h	1	0	0	0	0	1	1	EFLAG1	read only	output error flag 1
44h	1	0	0	0	1	0	0	EFLAG2	read only	output error flag 2
45h	1	0	0	0	1	0	1	EFLAG3	read only	output error flag 3
46h to 7Fh	1 : 1	0 : 1	0 : 1	0 : 1	1 : 1	1 : 1	0 : 1	reserved[1]	read only	not used

[1] Reserved registers should not be written to and will always read back as zeros.

7.2.1 MODE1 — Mode register 1

Table 5. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	R/W	0*	reserved
5	-	R/W	0*	reserved
4	SLEEP	R/W	0*	Normal mode[1].
			1	Low-power mode. Oscillator off[2][3].
3	-	R/W	0*	reserved
2	-	R/W	0*	reserved
1	-	R/W	0*	reserved
0	-	R/W	0*	reserved

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2] No blinking, dimming or gradation control is possible when the oscillator is off.

[3] The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

7.2.2 MODE2 — Mode register 2

Table 6. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	OVERTEMP	read only	0*	O.K.
			1	overtemperature condition
6	ERROR	read only	0*	no error at LED outputs
			1	any open or short-circuit detected in error flag registers (EFLAGn)
5	DMBLNK	R/W	0*	group control = dimming
			1	group control = blinking
4	CLRERR	write only	0*	self clear after write ‘1’
			1	Write ‘1’ to clear all error status bits in EFLAGn register and ERROR (bit 6). The EFLAGn and ERROR bit will set to ‘1’ if open or short-circuit is detected again.
3	-	R/W	0*	reserved
2	EXP_EN	R/W	0*	linear adjustment for gradation control
			1	exponential adjustment for gradation control
1	-	read only	0*	reserved
0	-	read only	1*	reserved

Brightness adjustment for gradation control is either linear or exponential by setting the EXP_EN bit as shown in Figure 4. When EXP_EN = 0, linear adjustment scale is used. When EXP_EN = 1, exponential scale is used.

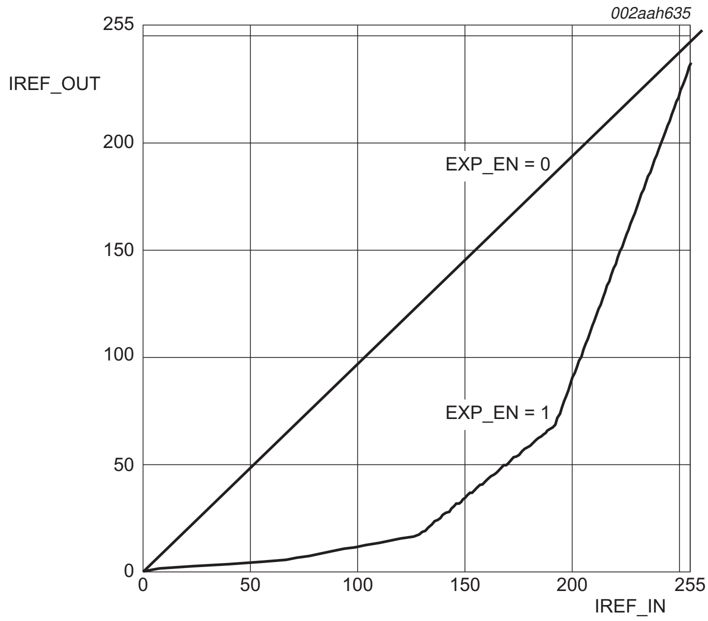


Fig 4. Linear and exponential adjustment curves

7.2.3 LEDOUT0 to LEDOUT3, LED driver output state

Table 7. LEDOUT0 to LEDOUT3 - LED driver output state registers (address 02h to 05h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	LEDOUT0	7:6	LDR3	R/W	10*	LED3 output state control
		5:4	LDR2	R/W	10*	LED2 output state control
		3:2	LDR1	R/W	10*	LED1 output state control
		1:0	LDR0	R/W	10*	LED0 output state control
03h	LEDOUT1	7:6	LDR7	R/W	10*	LED7 output state control
		5:4	LDR6	R/W	10*	LED6 output state control
		3:2	LDR5	R/W	10*	LED5 output state control
		1:0	LDR4	R/W	10*	LED4 output state control
04h	LEDOUT2	7:6	LDR11	R/W	10*	LED11 output state control
		5:4	LDR10	R/W	10*	LED10 output state control
		3:2	LDR9	R/W	10*	LED9 output state control
		1:0	LDR8	R/W	10*	LED8 output state control
05h	LEDOUT3	7:6	LDR15	R/W	10*	LED15 output state control
		5:4	LDR14	R/W	10*	LED14 output state control
		3:2	LDR13	R/W	10*	LED13 output state control
		1:0	LDR12	R/W	10*	LED12 output state control

LDRx = 00 — LED driver x is off (x = 0 to 15).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled). The $\overline{OE}$ pin can be used as external dimming/blinking control in this state.

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register (default power-up state) or PWMALL register for all LEDn outputs.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

Remark: Setting the device in low power mode while being on group dimming/blinking mode (LDRx = 11) may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

7.2.4 GRPPWM, group duty cycle control

Table 8. GRPPWM - Group brightness control register (address 06h) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
06h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 16 outputs is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (1)$$

7.2.5 GRPFREQ, group frequency

Table 9. GRPFREQ - Group frequency register (address 07h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
07h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{15.26}(s) \quad (2)$$

7.2.6 PWM0 to PWM15, individual brightness control

Table 10. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
09h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
0Ah	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
0Bh	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
0Ch	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
0Dh	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
0Eh	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
0Fh	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle
10h	PWM8	7:0	IDC8[7:0]	R/W	0000 0000*	PWM8 Individual Duty Cycle
11h	PWM9	7:0	IDC9[7:0]	R/W	0000 0000*	PWM9 Individual Duty Cycle
12h	PWM10	7:0	IDC10[7:0]	R/W	0000 0000*	PWM10 Individual Duty Cycle
13h	PWM11	7:0	IDC11[7:0]	R/W	0000 0000*	PWM11 Individual Duty Cycle
14h	PWM12	7:0	IDC12[7:0]	R/W	0000 0000*	PWM12 Individual Duty Cycle

Table 10. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description *…continued*

Address	Register	Bit	Symbol	Access	Value	Description
15h	PWM13	7:0	IDC13[7:0]	R/W	0000 0000*	PWM13 Individual Duty Cycle
16h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000*	PWM14 Individual Duty Cycle
17h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000*	PWM15 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FEh (99.2 % duty cycle = LED output at maximum brightness) and FFh (100 % duty cycle = LED output completed ON). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \qquad (3)$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM will not have effective brightness control of LEDs due to edge rate control of LED output pins.

7.2.7 IREF0 to IREF15, LED output current value registers

These registers reflect the gain settings for output current for LED0 to LED15.

Table 11. IREF0 to IREF15 - LED output gain control registers (address 18h to 27h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
18h	IREF0	7:0	R/W	00h*	LED0 output current setting
19h	IREF1	7:0	R/W	00h*	LED1 output current setting
1Ah	IREF2	7:0	R/W	00h*	LED2 output current setting
1Bh	IREF3	7:0	R/W	00h*	LED3 output current setting
1Ch	IREF4	7:0	R/W	00h*	LED4 output current setting
1Dh	IREF5	7:0	R/W	00h*	LED5 output current setting
1Eh	IREF6	7:0	R/W	00h*	LED6 output current setting
1Fh	IREF7	7:0	R/W	00h*	LED7 output current setting
20h	IREF8	7:0	R/W	00h*	LED8 output current setting
21h	IREF9	7:0	R/W	00h*	LED9 output current setting
22h	IREF10	7:0	R/W	00h*	LED10 output current setting
23h	IREF11	7:0	R/W	00h*	LED11 output current setting
24h	IREF12	7:0	R/W	00h*	LED12 output current setting
25h	IREF13	7:0	R/W	00h*	LED13 output current setting
26h	IREF14	7:0	R/W	00h*	LED14 output current setting
27h	IREF15	7:0	R/W	00h*	LED15 output current setting

7.2.8 Gradation control

Gradation control is designed to use four independent groups of registers to program the full cycle of the gradation timing to implement on each selected channel. Each group has four registers to define the ramp rate, step time, hold ON/OFF time, and final hold ON current, as shown in Figure 5.

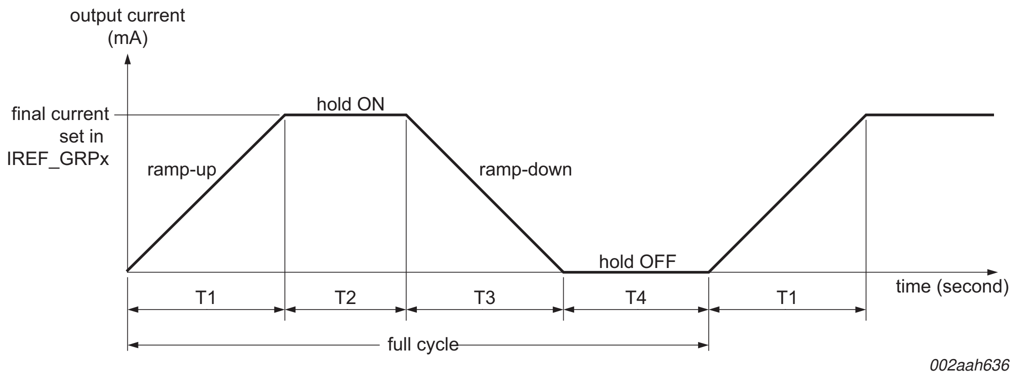


Fig 5. Gradation timing

- The ‘final’ and ‘hold ON’ current is defined in IREF_GRPx register value × (225 μA if REXT = 1 kΩ, or 112.5 μA if REXT = 2 kΩ).
- Ramp rate value and enable/disable ramp operation is defined in RAMP_RATE_GRPx register.
- Total number of ramp steps (or level changes) is calculated as ‘IREF_GRPx value’ ÷ ‘ramp rate value in RAMP_RATE_GRPx’. Rounds a number up to the next integer if the total number is not an integer.
- Time for each step is calculated as ‘cycle time’ × ‘multiple factor’ bits in STEP_TIME_GRPx register. Minimum time for one step is 0.5 ms (0.5 ms × 1) and maximum time is 512 ms (8 ms × 64).
- The ramp-up or ramp-down time (T1 or T3) is calculated as ‘(total steps + 1)’ × ‘step time’.
- Hold ON or OFF time (T2 or T4) is defined in HOLD_CNTL_GRPx register in the range of 0/0.25/0.5/0.75/1/2/4/6 seconds.
- Gradation start or stop with single shot mode (one full cycle only) or continuous mode (repeat full cycle) is defined in the GRAD_CNTL register for all groups.
- Each channel can be assigned to one of these four groups in the GRAD_GRP_SELx register.
- Each channel can set either normal mode or gradation mode operation in the GRAD_MODE_SELx register.

To enable the gradation operation, the following steps are required:

1. Program all gradation control registers except the gradation start bit in GRAD_CNTL register.
2. Program either LDRx = 01 (LED fully ON mode) only, or LDRx = 10 or 11 (PWM control mode) with individual brightness control PWMx register for duty cycle.

3. Program output current value IREFx register to non-zero, which will enable LED output.
4. Set the gradation start bit in GRAD_CNTL register for enabling gradation operation.

7.2.8.1 RAMP_RATE_GRP0 to RAMP_RATE_GRP3, ramp rate control registers

Table 12. RAMP_RATE_GRP[0:3] - Ramp enable and rate control registers (address 28h, 2Ch, 30h, 34h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
28h	RAMP_RATE_GRP0	7	R/W	0*	Ramp-up disable
2Ch	RAMP_RATE_GRP1			1	Ramp-up enable
30h	RAMP_RATE_GRP2	6	R/W	0*	Ramp-down disable
34h	RAMP_RATE_GRP3			1	Ramp-down enable
		5:0	R/W	0x00*	Ramp rate value per step is defined from 1 (00h) to 64 (3Fh)[1][2]

[1] Total number of ramp steps is defined as 'IREF_GRP[7:0]' ÷ 'ramp_rate[5:0]'. (Round up to next integer if it is not an integer number.)

[2] Per step current increment or decrement is calculated by the (ramp_rate × I_{ref}), where the I_{ref} reference current is 112.5 μA (REXT = 2 kΩ) or 225 μA (REXT = 1 kΩ).

7.2.8.2 STEP_TIME_GRP0 to STEP_TIME_GRP3, step time control registers

Table 13. STEP_TIME_GRP[0:3] - Step time control registers (address 29h, 2Dh, 31h, 35h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
29h	STEP_TIME_GRP0	7	read only	0*	reserved
2Dh	STEP_TIME_GRP1	6	R/W	0*	Cycle time is set to 0.5 ms
31h	STEP_TIME_GRP2			1	Cycle time is set to 8 ms
35h	STEP_TIME_GRP3	5:0	R/W	0x00*	Multiple factor per step, the multiple factor is defined from 1 (00h) to 64 (3Fh)[1]

[1] Step time = cycle time (0.5 ms or 8 ms) × multiple factor (1 ~ 64); minimum step time is 0.5 ms and maximum step time is 512 ms.

7.2.8.3 HOLD_CNTL_GRP0 to HOLD_CNTL_GRP3, hold ON and OFF control registers

Table 14. HOLD_CNTL_GRP[0:3] - Hold ON and OFF enable and time control registers (address 2Ah, 2Eh, 32h, 36h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
2Ah	HOLD_CNTL_GRP0	7	R/W	0*	Hold ON disable
2Eh	HOLD_CNTL_GRP1			1	Hold ON enable
32h	HOLD_CNTL_GRP2	6	R/W	0*	Hold OFF disable
36h	HOLD_CNTL_GRP3			1	Hold OFF enable
		5:3	R/W	000*	Hold ON time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s
		2:0	R/W	000*	Hold OFF time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s

[1] Hold ON or OFF minimum time is 0 s and maximum time is 6 s.

7.2.8.4 IREF_GRP0 to IREF_GRP3, output gain control

Table 15. IREF_GRP[0:3] - Final and hold ON output gain setting registers (address 2Bh, 2Fh, 33h, 37h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
2Bh	IREF_GRP0	7:0	R/W	00h*	Final ramp-up and hold ON output current gain setting[1]
2Fh	IREF_GRP1				
33h	IREF_GRP2				
37h	IREF_GRP3				

[1] Output current = $I_{ref} \times$ IREF_GRPx[7:0], where I_{ref} is reference current. I_{ref} = 112.5 μA if REXT = 2 kΩ, or I_{ref} = 225 μA if REXT = 1 kΩ

7.2.8.5 GRAD_MODE_SEL0 to GRAD_MODE_SEL1, Gradation mode select registers

Table 16. GRAD_MODE_SEL[0:1] - Gradation mode select register for channel 15 to channel 0 (address 38h, 39h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1][2]
38h	GRAD_MODE_SEL0	7:0	R/W	00*	Normal operation mode for channel 7 to channel 0
				FFh	Gradation operation mode for channel 7 to channel 0
39h	GRAD_MODE_SEL1	7:0	R/W	00*	Normal operation mode for channel 15 to channel 8
				FFh	Gradation operation mode for channel 15 to channel 8

[1] Each bit represents one channel that can set either 0 for normal mode (use IREFx to set individual LED output current), or 1 for gradation mode (use IREF_GRPx to set group LEDs output current.).

[2] In gradation mode, it only affects the source of the IREF current level and does not affect the PWMx operation or LEDOUTx registers' function. It is possible to use the gradation feature, individual PWMx and group PWM simultaneously.

7.2.8.6 GRAD_GRP_SEL0 to GRAD_GRP_SEL3, Gradation group select registers

Table 17. GRAD_GRP_SEL[0:3] - Gradation group select register for channel 15 to channel 0 (address 3Ah, 3Bh, 3Ch, 3Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1]
3Ah	GRAD_GRP_SEL0	7:6	R/W	00*	Gradation group select for LED3 output
		5:4	R/W	00*	Gradation group select for LED2 output
		3:2	R/W	00*	Gradation group select for LED1 output
		1:0	R/W	00*	Gradation group select for LED0 output
3Bh	GRAD_GRP_SEL1	7:6	R/W	01*	Gradation group select for LED7 output
		5:4	R/W	01*	Gradation group select for LED6 output
		3:2	R/W	01*	Gradation group select for LED5 output
		1:0	R/W	01*	Gradation group select for LED4 output
3Ch	GRAD_GRP_SEL2	7:6	R/W	10*	Gradation group select for LED11 output
		5:4	R/W	10*	Gradation group select for LED10 output
		3:2	R/W	10*	Gradation group select for LED9 output
		1:0	R/W	10*	Gradation group select for LED8 output
3Dh	GRAD_GRP_SEL3	7:6	R/W	11*	Gradation group select for LED15 output
		5:4	R/W	11*	Gradation group select for LED14 output
		3:2	R/W	11*	Gradation group select for LED13 output
		1:0	R/W	11*	Gradation group select for LED12 output

[1] LED[3:0] outputs default assigned to group 0; LED[7:4] outputs default assigned to group 1; LED[11:8] outputs default assigned to group 2; LED[15:12] outputs default assigned to group 3.

7.2.8.7 GRAD_CNTL, Gradation control register

Table 18. GRAD_CNTL - Gradation control register for group 3 to group 0 (address 3Eh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Eh	GRAD_CNTL	7	R/W	0*	Gradation stop or done for group 3[1]
				1	Gradation start for group 3[2]
		6	R/W	0*	Single shot operation for group 3
				1	Continuous operation for group 3
		5	R/W	0*	Gradation stop or done for group 2[1]
				1	Gradation start for group 2[2]
		4	R/W	0*	Single shot operation for group 2
				1	Continuous operation for group 2
		3	R/W	0*	Gradation stop or done for group 1[1]
				1	Gradation start for group 1[2]
		2	R/W	0*	Single shot operation for group 1
				1	Continuous operation for group 1
		1	R/W	0*	Gradation stop or done for group 0[1]
				1	Gradation start for group 0[2]
		0	R/W	0*	Single shot operation for group 0
				1	Continuous operation for group 0

[1] When the gradation operation is forced to stop, the output current stops immediately and is frozen at the last output level.

[2] This bit will be self-cleared when single mode is completed, and writing 0 to this bit will force to stop the gradation operation when single mode is not completed or continuous mode is running.

7.2.8.8 Ramp control — equation and calculation example

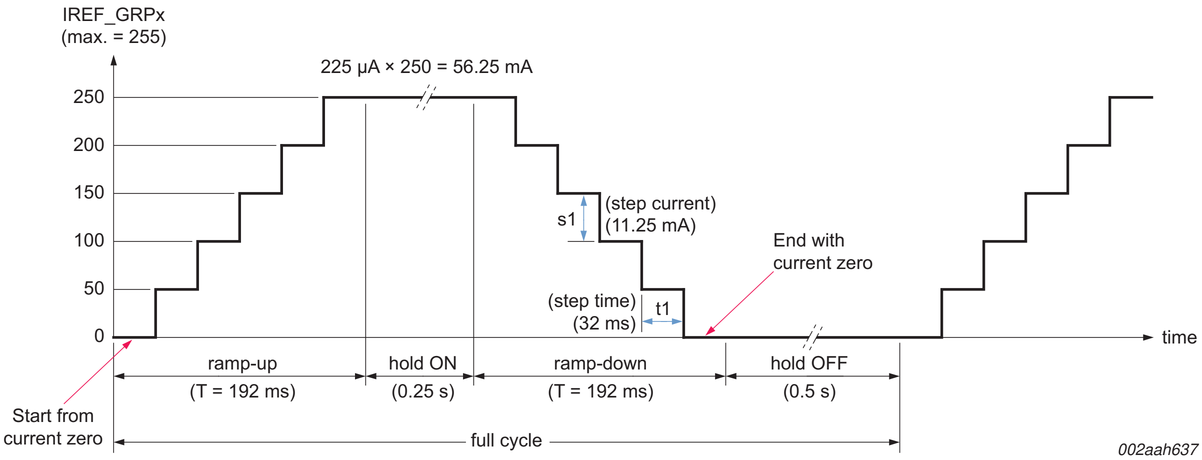


Fig 6. Ramp calculation example 1

- t1 (step time) = cycle time × multiple factor, where:
  - Cycle time = 0.5 ms (fast ramp) or 8 ms (slow ramp) in STEP_TIME_GRPx[6]
  - Multiple factor = 6-bit, from 1 (00h) to 64 (3Fh) counts in STEP_TIME_GRPx[5:0]
- s1 (step current) = ramp_rate × I_{ref}, where:
  - ramp_rate = 6-bit, from 1 (00h) to 64 (3Fh) counts in RAMP_RATE_GRPx[5:0]
  - I_{ref} = reference current either 112.5 µA if REXT = 2 kΩ, or 225 µA if REXT = 1 kΩ
- S (total steps) = (IREF_GRPx / ramp_rate), where:
  - IREF_GRPx = output current gain setting, 8-bit, up to 255 counts
  - ramp_rate = 6-bit, up to 64 counts in RAMP_RATE_GRPx[5:0]
  - If it is not an integer, then round up to next integer number.
- T (ramp time) = (S (total steps) + 1) × t1 (step time)
  - Ramp-up time starts from zero current and ends at the maximum current
  - Ramp-down time starts from the maximum current and ends at the zero current

Calculation example 1 (Figure 6):

- Assumption:
  - I_{ref} = 225 µA if REXT = 1 kΩ
  - Output hold ON current = 225 µA × 250 = 56.25 mA (IREF_GRPx[7:0] = FAh)
  - Cycle time = 0.5 ms (STEP_TIME_GRPx[6] = 0)
  - Multiple factor = 64 (STEP_TIME_GRPx[5:0] = 3Fh)
  - Ramp rate = 50 (RAMP_RATE_GRPx[5:0] = 31h)
  - Hold ON = 0.25 s (HOLD_CNTL_GRPx[5:3] = 001)
  - Hold OFF = 0.5 s (HOLD_CNTL_GRPx[2:0] = 010)
- t1 (step time) = cycle time (0.5 ms) × multiple (64) = 32 ms
- Step current = ramp_rate × I_{ref} = 50 × 225 µA = 11.25 mA

- S (total steps) = (IREF_GRPx ÷ ramp_rate) = (250 ÷ 50) = 5 steps
- T (ramp time) = (S + 1) × t1 = 6 × 32 ms = 192 ms

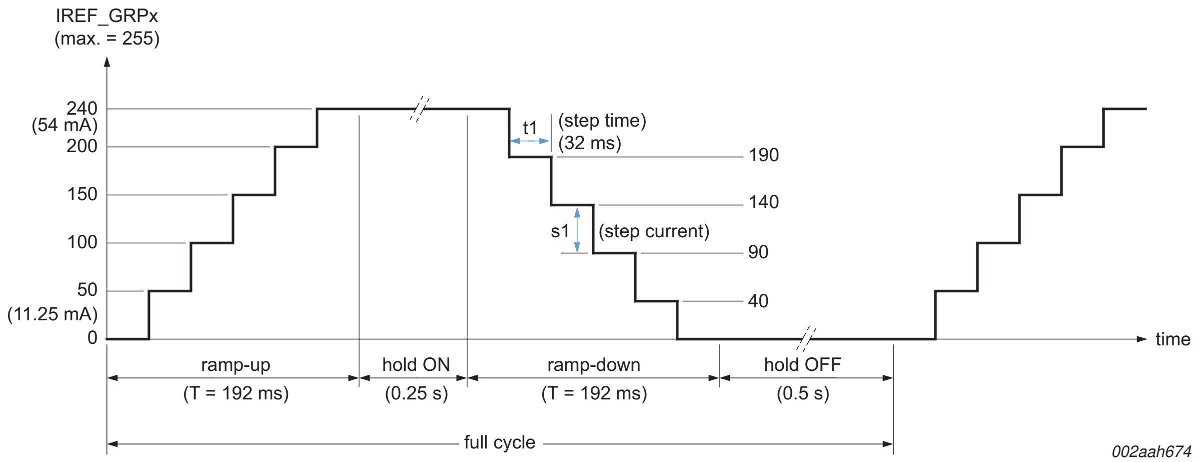
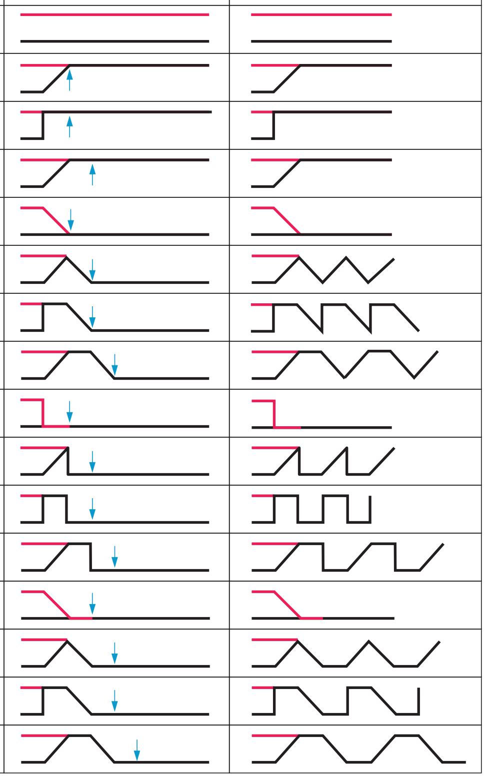


Fig 7. Ramp calculation example 2

Calculation example 2:

- Assumption:
  - I_{ref} = 225 μA if REXT = 1 kΩ
  - Output hold ON current = 225 μA × 240 = 54 mA (IREF_GRPx[7:0] = F0h)
  - Cycle time = 0.5 ms (STEP_TIME_GRPx[6] = 0)
  - Multiple factor = 64 (STEP_TIME_GRPx[5:0] = 3Fh)
  - Ramp rate = 50 (RAMP_RATE_GRPx[5:0] = 31h)
  - Hold ON = 0.25 s (HOLD_CNTL_GRPx[5:3] = 001)
  - Hold OFF = 0.5 s (HOLD_CNTL_GRPx[2:0] = 010)
- t1 (step time) = cycle time (0.5 ms) × multiple (64) = 32 ms
- Step current = ramp_rate × I_{ref} = 50 × 225 μA = 11.25 mA (except the last one)
- S (total steps) = IREF_GRPx ÷ ramp_rate = 240 ÷ 50 = 4.8 steps (round up to next integer) = 5 steps
- T (ramp time) = (S + 1) × t1 = 6 × 32 ms = 192 ms

	(enable bit) Ramp UP	(enable bit) Hold ON	(enable bit) Ramp DOWN	(enable bit) Hold OFF	Single shot waveform	Continuous waveform
1	0	0	0	0		
2	1	0	0	0		
3	0	1	0	0		
4	1	1	0	0		
5	0	0	1	0		
6	1	0	1	0		
7	0	1	1	0		
8	1	1	1	0		
9	0	0	0	1		
10	1	0	0	1		
11	0	1	0	1		
12	1	1	0	1		
13	0	0	1	1		
14	1	0	1	1		
15	0	1	1	1		
16	1	1	1	1		



wavefrom when initial current is not zero

the moment when START bit changes to 0 (single shot sequence ends)

aaa-009234

Fig 8. Gradation output waveform in single shot or continuous mode

7.2.9 OFFSET — LEDn output delay offset register

Table 19. OFFSET - LEDn output delay offset register (address 3Fh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Fh	OFFSET	7:4	read only	0000*	not used
		3:0	R/W	1000*	LEDn output delay offset factor

The PCA9745B can be programmed to have turn-on delay between LED outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

The order in which the LED outputs are enabled will always be the same (channel 0 will enable first and channel 15 will enable last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows:

0000 = no delay between outputs (all on, all off at the same time)

0001 = delay of 1 clock cycle (125 ns) between successive outputs

0010 = delay of 2 clock cycles (250 ns) between successive outputs

0011 = delay of 3 clock cycles (375 ns) between successive outputs

:

1111 = delay of 15 clock cycles (1.875 μs) between successive outputs

Example: If the value in the OFFSET register is 1000 the corresponding delay = 8 × 125 ns = 1 μs delay between successive outputs.

channel 0 turns on at time 0 μs

channel 1 turns on at time 1 μs

channel 2 turns on at time 2 μs

channel 3 turns on at time 3 μs

channel 4 turns on at time 4 μs

channel 5 turns on at time 5 μs

channel 6 turns on at time 6 μs

channel 7 turns on at time 7 μs

channel 8 turns on at time 8 μs

channel 9 turns on at time 9 μs

channel 10 turns on at time 10 μs

channel 11 turns on at time 11 μs

channel 12 turns on at time 12 μs

channel 13 turns on at time 13 μs

channel 14 turns on at time 14 μs

channel 15 turns on at time 15 μs

7.2.10 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register will be used for PWM duty cycle for all the LEDn outputs and will be reflected in PWM0 through PWM15 registers.

Table 20. PWMALL - brightness control for all LEDn outputs register (address 40h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
40h	PWMALL	7:0	write only	0000 0000*	duty cycle for all LEDn outputs

Remark: Write to any of the PWM0 to PWM15 registers will overwrite the value in corresponding PWMn register programmed by PWMALL.

7.2.11 IREFALL register: output current value for all LED outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LED outputs will be set to a current corresponding to this register value.

Writes to IREF0 to IREF15 will overwrite the output current settings.

Table 21. IREFALL - Output gain control for all LED outputs (address 41h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
41h	IREFALL	7:0	write only	00h*	Current gain setting for all LED outputs.

7.2.12 LED driver constant current outputs

In LED display applications, PCA9745B provides nearly no current variations from channel to channel and from device to device. The maximum current skew between channels is less than ±4 % and less than ±6 % between devices.

7.2.12.1 Adjusting output current

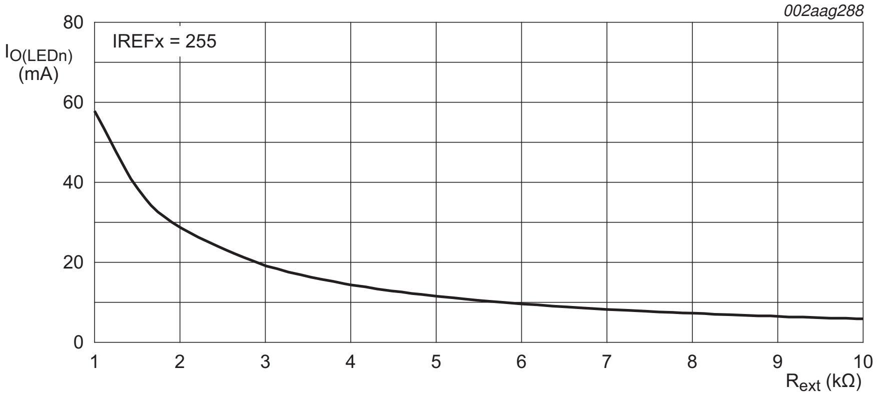
The PCA9745B scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_O) at each output port. The maximum output current for the outputs can be set using R_{ext}. In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF15. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

Equation 4 and Equation 5 can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O\_LED\_MIN = \frac{900\ mV}{R_{ext}} \times \frac{1}{4} \text{ (minimum constant current)} \quad (4)$$

$$I_O\_LED\_MAX = (255 \times I_O\_LED\_MIN) = \left(\frac{900\ mV}{R_{ext}} \times \frac{255}{4}\right) \quad (5)$$

For a given IREFx setting, $I_O\_LED = IREFx \times \frac{900\ mV}{R_{ext}} \times \frac{1}{4}$.



$I_{O(LEDn)}$ (mA) = IREFx × (0.9 / 4) / R_{ext} (kΩ)

maximum $I_{O(LEDn)}$ (mA) = 255 × (0.9 / 4) / R_{ext} (kΩ)

Remark: Default IREFx at power-up = 0.

Fig 9. Maximum I_{LED} versus R_{ext}

Example 1: If R_{ext} = 1 kΩ, I_O_LED_MIN = 225 μA, I_O_LED_MAX = 57.375 mA (as shown in Figure 10).

So each channel can be programmed with its individual IREFx in 256 steps and in 225 μA increments to a maximum output current of 57.375 mA independently.

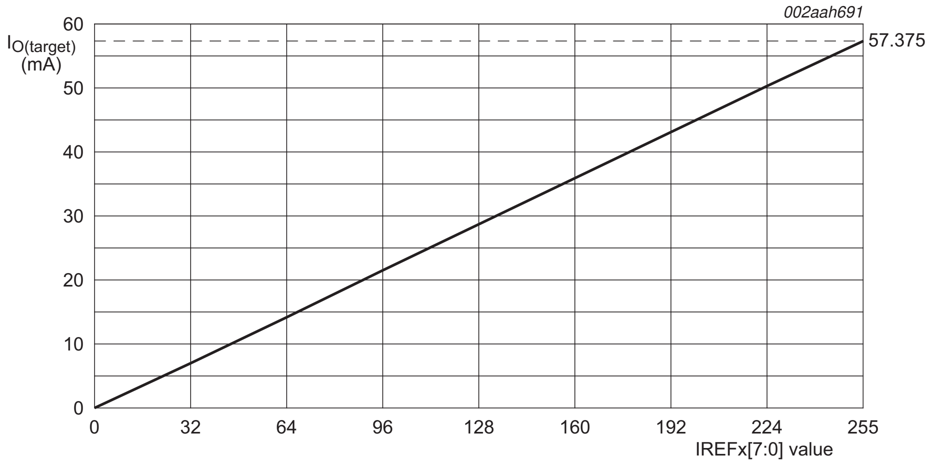


Fig 10. $I_{O(target)}$ versus IREFx value with R_{ext} = 1 kΩ

Example 2: If R_{ext} = 2 kΩ, I_O_LED_MIN = 112.5 μA, I_O_LED_MAX = 28.687 mA (as shown in Figure 11).

So each channel can be programmed with its individual IREFx in 256 steps and in 112.5 μA increments to a maximum output channel of 28.687 mA independently.

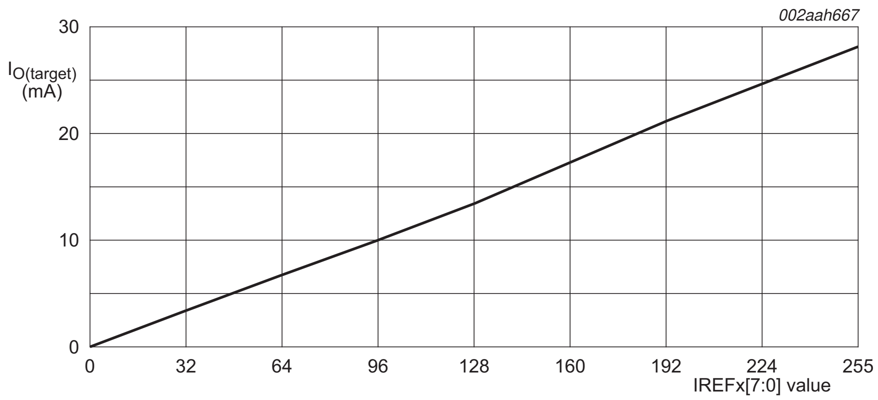


Fig 11. $I_{O(target)}$ versus IREFx value with R_{ext} = 2 kΩ