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PCA9956B

24-channel Fm+ I2C-bus 57 mA/20 V constant current LED driver

Rev. 1.1 — 15 December 2015   **Product data sheet**

1. General description

The PCA9956B is an I2C-bus controlled 24-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCA9956B operates with a supply voltage range of 3 V to 5.5 V and the constant current sink LED outputs allow up to 20 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 225 μA to 57 mA.

This device has built-in open, short load and overtemperature detection circuitry. The error information from the corresponding register can be read via the I2C-bus. Additionally, a thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCA9956B device has a Fast-mode Plus (Fm+) I2C-bus interface. Fm+ devices offer higher frequency (up to 1 MHz) or more densely populated bus operation (up to 4000 pF).

The active LOW output enable input pin ($\overline{OE}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I2C-bus addresses allow all or defined groups of PCA9956B devices to respond to a common I2C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I2C-bus commands. On power-up, PCA9956B will have a unique Sub Call address to identify it as a 24-channel LED driver. This allows mixing of devices with different channel widths. Three hardware address pins on PCA9956B allow up to 125 devices on the same bus.

The Software Reset (SWRST) function allows the master to perform a reset of the PCA9956B through the I2C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output current switches to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

2. Features and benefits

- 24 LED drivers. Each output programmable at:
  - ◆ Off
  - ◆ On
  - ◆ Programmable LED brightness
  - ◆ Programmable group dimming/blinking mixed with individual LED brightness
  - ◆ Programmable LED output delay to reduce EMI and surge currents
- 24 constant current output channels can sink up to 57 mA, tolerate up to 20 V when OFF
- Output current adjusted through an external resistor (REXT input)
- Output current accuracy
  - ◆ ±4 % between output channels
  - ◆ ±6 % between PCA9956B devices
- Open/short load/overtemperature detection mode to detect individual LED errors
- 1 MHz Fast-mode Plus compatible I²C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs
- Three quinary hardware address pins allow 125 PCA9956B devices to be connected to the same I²C-bus and to be individually programmed
- Four software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCA9956Bs on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that $\frac{1}{3}$ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for each programmable I²C-bus address.
- Unique power-up default Sub Call address allows mixing of devices with different channel widths
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- No glitch on LEDn outputs on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins

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- ■ −40 °C to +85 °C operation
- ■ ESD protection exceeds 3000 V HBM per JESD22-A114
- ■ Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- ■ Packages offered: HTSSOP38

3. Applications

- ■ Amusement products
- ■ RGB or RGBA LED drivers
- ■ LED status information
- ■ LED displays
- ■ LCD backlights
- ■ Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1.   Ordering information

Type number	Topside mark	Package		
		Name	**Description**	**Version**
PCA9956BTW	PCA9956BTW	HTSSOP38	plastic thermal enhanced thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm; exposed die pad	SOT1331-1

4.1 Ordering options

Table 2.   Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9956BTW	PCA9956BTWY	HTSSOP38	Reel 13" Q1/T1 *Standard mark SMD dry pack	2500	T_{amb} = −40 °C to +85 °C

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5. Block diagram

Dim repetition rate = 122 Hz.

Blink repetition rate = 15 Hz to every 16.8 seconds.

Fig 1.   Block diagram of PCA9956B
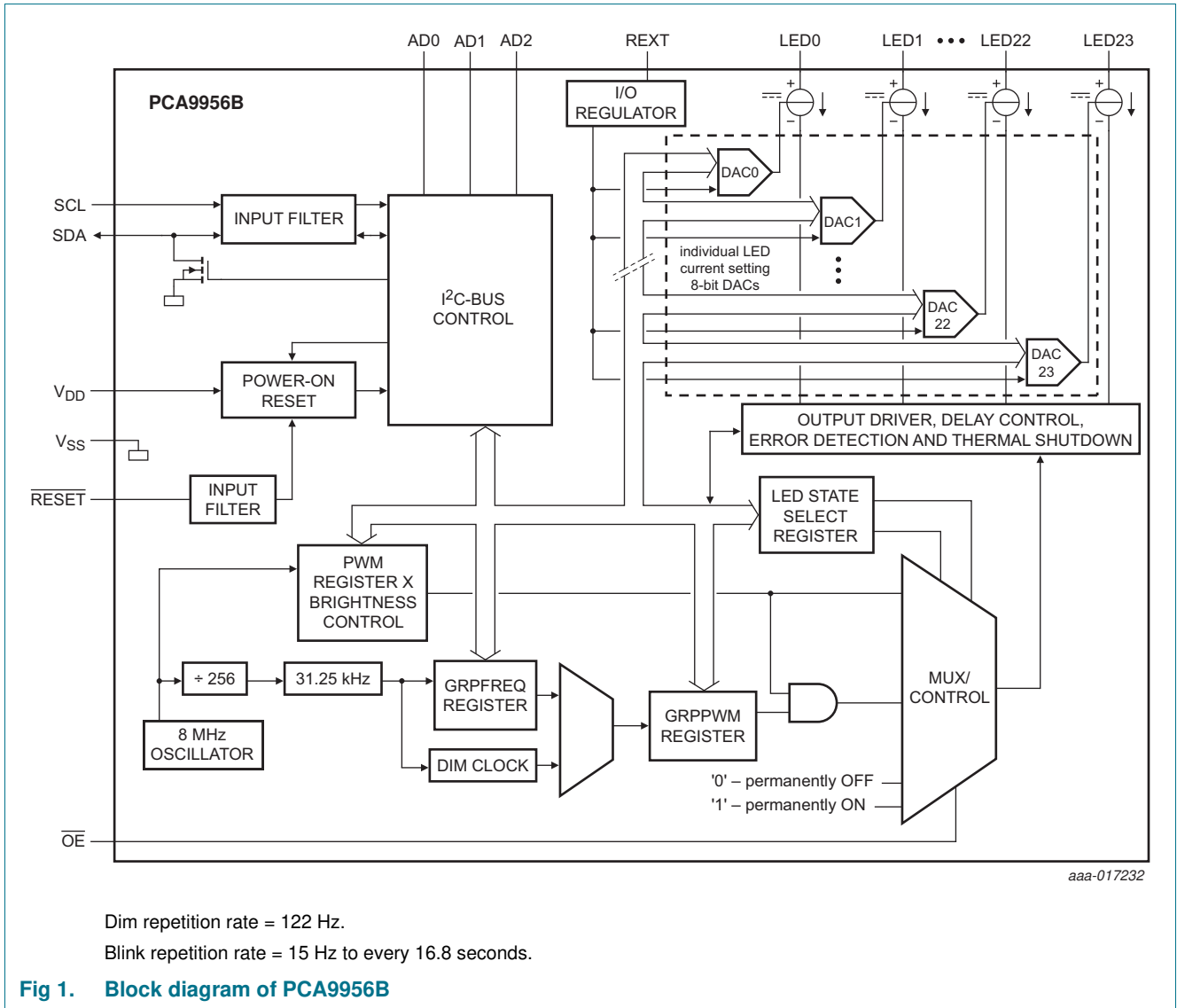
6. Pinning information

6.1 Pinning

REXT	1	38	V_DD
AD0	2	37	SDA
AD1	3	36	SCL
AD2	4	35	RESET
OE	5	34	V_SS
LED0	6	33	LED23
LED1	7	32	LED22
LED2	8	31	LED21
LED3	9	30	LED20
LED4	10	29	LED19
LED5	11	28	LED18
LED6	12	27	LED17
LED7	13	26	LED16
V_SS	14	25	V_SS
LED8	15	24	LED15
LED9	16	23	LED14
LED10	17	22	LED13
V_SS	18	21	V_SS
LED11	19	20	LED12

PCA9956BTW

(1)

Transparant top view   aaa-017233

(1) Thermal pad; connected to V_SS.

Fig 2.   Pin configuration for HTSSOP38

6.2 Pin description

Table 3.   Pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
AD0	2	I	address input 0
AD1	3	I	address input 1
AD2	4	I	address input 2
$\overline{OE}$	5	I	active LOW output enable for LEDs
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	10	O	LED driver 4
LED5	11	O	LED driver 5
LED6	12	O	LED driver 6
LED7	13	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	19	O	LED driver 11
LED12	20	O	LED driver 12
LED13	22	O	LED driver 13
LED14	23	O	LED driver 14
LED15	24	O	LED driver 15
LED16	26	O	LED driver 16
LED17	27	O	LED driver 17
LED18	28	O	LED driver 18
LED19	29	O	LED driver 19
LED20	30	O	LED driver 20
LED21	31	O	LED driver 21
LED22	32	O	LED driver 22
LED23	33	O	LED driver 23
$\overline{RESET}$	35	I	active LOW reset input with external 10 kΩ pull-up resistor
SCL	36	I	serial clock line
SDA	37	I/O	serial data line
V_{SS}	14, 18, 21, 25, 34 [1]	ground	supply ground
V_{DD}	38	power supply	supply voltage

[1]   HTSSOP38 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 1 "Block diagram of PCA9956B".

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

For PCA9956B there are a maximum of 125 possible programmable addresses using the three quinary hardware address pins.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCA9956B is shown in Figure 3. The 7-bit slave address is determined by the quinary input pads AD0, AD1 and AD2. Each pad can have one of five states (GND, pull-up, floating, pull-down, and V_{DD}) based on how the input pad is connected on the board. At power-up or hardware/software reset, the quinary input pads are sampled and set the slave address of the device internally. To conserve power, once the slave address is determined, the quinary input pads are turned off and will not be sampled until the next time the device is power cycled. Table 4 lists the five possible connections for the quinary input pads along with the external resistor values that must be used.

Table 4.   Quinary input pad connection

Pad connection (pins AD2, AD1, AD0)[1]	Mnemonic	External resistor (kΩ)	
		Min.	Max.
tie to ground	GND	0	17.9
resistor pull-down to ground	PD	34.8	270
open (floating)	FLT	503	∞
resistor pull-up to V_{DD}	PU	31.7	340
tie to V_{DD}	V_{DD}	0	22.1

[1]   These AD[2:0] inputs must be stable before the supply V_{DD} to the chip.

Table 5 lists all 125 possible slave addresses of the device based on all combinations of the five states connected to three address input pins AD0, AD1 and AD2.

Table 5.   I²C-bus slave address

Hardware selectable input pins			I²C-bus slave address for PCA9956B			
AD2	AD1	AD0	Decimal	Hex	Binary (A[6:0])	Address (R/$\overline{W}$ = 0)
GND	GND	GND	1	01	0000001[1]	02h
GND	GND	PD	2	02	0000010[1]	04h
GND	GND	FLT	3	03	0000011[1]	06h
GND	GND	PU	4	04	0000100[1]	08h
GND	GND	V_{DD}	5	05	0000101[1]	0Ah
GND	PD	GND	6	06	0000110[1]	0Ch
GND	PD	PD	7	07	0000111[1]	0Eh
GND	PD	FLT	8	08	0001000	10h
GND	PD	PU	9	09	0001001	12h

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24-channel Fm+ I²C-bus 57 mA/20 V constant current LED driver

Table 5. **I²C-bus slave address** *…continued*

Hardware selectable input pins			I²C-bus slave address for PCA9956B			
AD2	AD1	AD0	Decimal	Hex	Binary (A[6:0])	Address (R/W̄ = 0)
GND	PD	V_DD	10	0A	0001010	14h
GND	FLT	GND	11	0B	0001011	16h
GND	FLT	PD	12	0C	0001100	18h
GND	FLT	FLT	13	0D	0001101	1Ah
GND	FLT	PU	14	0E	0001110	1Ch
GND	FLT	V_DD	15	0F	0001111	1Eh
GND	PU	GND	16	10	0010000	20h
GND	PU	PD	17	11	0010001	22h
GND	PU	FLT	18	12	0010010	24h
GND	PU	PU	19	13	0010011	26h
GND	PU	V_DD	20	14	0010100	28h
GND	V_DD	GND	21	15	0010101	2Ah
GND	V_DD	PD	22	16	0010110	2Ch
GND	V_DD	FLT	23	17	0010111	2Eh
GND	V_DD	PU	24	18	0011000	30h
GND	V_DD	V_DD	25	19	0011001	32h
PD	GND	GND	26	1A	0011010	34h
PD	GND	PD	27	1B	0011011	36h
PD	GND	FLT	28	1C	0011100	38h
PD	GND	PU	29	1D	0011101	3Ah
PD	GND	V_DD	30	1E	0011110	3Ch
PD	PD	GND	31	1F	0011111	3Eh
PD	PD	PD	32	20	0100000	40h
PD	PD	FLT	33	21	0100001	42h
PD	PD	PU	34	22	0100010	44h
PD	PD	V_DD	35	23	0100011	46h
PD	FLT	GND	36	24	0100100	48h
PD	FLT	PD	37	25	0100101	4Ah
PD	FLT	FLT	38	26	0100110	4Ch
PD	FLT	PU	39	27	0100111	4Eh
PD	FLT	V_DD	40	28	0101000	50h
PD	PU	GND	41	29	0101001	52h
PD	PU	PD	42	2A	0101010	54h
PD	PU	FLT	43	2B	0101011	56h
PD	PU	PU	44	2C	0101100	58h
PD	PU	V_DD	45	2D	0101101	5Ah
PD	V_DD	GND	46	2E	0101110	5Ch
PD	V_DD	PD	47	2F	0101111	5Eh
PD	V_DD	FLT	48	30	0110000	60h
PD	V_DD	PU	49	31	0110001	62h

Table 5. I2C-bus slave address *…continued*

Hardware selectable input pins			I2C-bus slave address for PCA9956B			
AD2	AD1	AD0	Decimal	Hex	Binary (A[6:0])	Address (R/W̅ = 0)
PD	V_{DD}	V_{DD}	50	32	0110010	64h
FLT	GND	GND	51	33	0110011	66h
FLT	GND	PD	52	34	0110100	68h
FLT	GND	FLT	53	35	0110101	6Ah
FLT	GND	PU	54	36	0110110	6Ch
FLT	GND	V_{DD}	55	37	0110111	6Eh
FLT	PD	GND	56	38	0111000	70h
FLT	PD	PD	57	39	0111001	72h
FLT	PD	FLT	58	3A	0111010	74h
FLT	PD	PU	59	3B	0111011	76h
FLT	PD	V_{DD}	60	3C	0111100	78h
FLT	FLT	GND	61	3D	0111101	7Ah
FLT	FLT	PD	62	3E	0111110	7Ch
FLT	FLT	FLT	63	3F	0111111	7Eh
FLT	FLT	PU	64	40	1000000	80h
FLT	FLT	V_{DD}	65	41	1000001	82h
FLT	PU	GND	66	42	1000010	84h
FLT	PU	PD	67	43	1000011	86h
FLT	PU	FLT	68	44	1000100	88h
FLT	PU	PU	69	45	1000101	8Ah
FLT	PU	V_{DD}	70	46	1000110	8Ch
FLT	V_{DD}	GND	71	47	1000111	8Eh
FLT	V_{DD}	PD	72	48	1001000	90h
FLT	V_{DD}	FLT	73	49	1001001	92h
FLT	V_{DD}	PU	74	4A	1001010	94h
FLT	V_{DD}	V_{DD}	75	4B	1001011	96h
PU	GND	GND	76	4C	1001100	98h
PU	GND	PD	77	4D	1001101	9Ah
PU	GND	FLT	78	4E	1001110	9Ch
PU	GND	PU	79	4F	1001111	9Eh
PU	GND	V_{DD}	80	50	1010000	A0h
PU	PD	GND	81	51	1010001	A2h
PU	PD	PD	82	52	1010010	A4h
PU	PD	FLT	83	53	1010011	A6h
PU	PD	PU	84	54	1010100	A8h
PU	PD	V_{DD}	85	55	1010101	AAh
PU	FLT	GND	86	56	1010110	ACh
PU	FLT	PD	87	57	1010111	AEh
PU	FLT	FLT	88	58	1011000	B0h
PU	FLT	PU	89	59	1011001	B2h

Table 5.   I²C-bus slave address *…continued*

Hardware selectable input pins			I²C-bus slave address for PCA9956B			
AD2	AD1	AD0	Decimal	Hex	Binary (A[6:0])	Address (R/W̄ = 0)
PU	FLT	V_DD	90	5A	1011010	B4h
PU	PU	GND	91	5B	1011011	B6h
PU	PU	PD	92	5C	1011100	B8h
PU	PU	FLT	93	5D	1011101	BAh
PU	PU	PU	94	5E	1011110	BCh
PU	PU	V_DD	95	5F	1011111	BEh
PU	V_DD	GND	96	60	1100000	C0h
PU	V_DD	PD	97	61	1100001	C2h
PU	V_DD	FLT	98	62	1100010	C4h
PU	V_DD	PU	99	63	1100011	C6h
PU	V_DD	V_DD	100	64	1100100	C8h
V_DD	GND	GND	101	65	1100101	CAh
V_DD	GND	PD	102	66	1100110	CCh
V_DD	GND	FLT	103	67	1100111	CEh
V_DD	GND	PU	104	68	1101000	D0h
V_DD	GND	V_DD	105	69	1101001	D2h
V_DD	PD	GND	106	6A	1101010	D4h
V_DD	PD	PD	107	6B	1101011	D6h
V_DD	PD	FLT	108	6C	1101100	D8h
V_DD	PD	PU	109	6D	1101101	DAh
V_DD	PD	V_DD	110	6E	1101110	DCh
V_DD	FLT	GND	111	6F	1101111	DEh
V_DD	FLT	PD	112	70	1110000	E0h
V_DD	FLT	FLT	113	71	1110001	E2h
V_DD	FLT	PU	114	72	1110010	E4h
V_DD	FLT	V_DD	115	73	1110011	E6h
V_DD	PU	GND	116	74	1110100	E8h
V_DD	PU	PD	117	75	1110101	EAh
V_DD	PU	FLT	118	76	1110110	ECh
V_DD	PU	PU	119	77	1110111	EEh
V_DD	PU	V_DD	120	78	1111000[1]	F0h
V_DD	V_DD	GND	121	79	1111001[1]	F2h
V_DD	V_DD	PD	122	7A	1111010[1]	F4h
V_DD	V_DD	FLT	123	7B	1111011[1]	F6h
V_DD	V_DD	PU	124	7C	1111100[1]	F8h
V_DD	V_DD	V_DD	125	7D	1111101[1]	FAh

[1]   See 'Remark' below.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- 'reserved for future use' I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)

slave address[1]

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ |

002aaf132

(1) This slave address must match one of the 125 internal addresses as shown in Table 5.

Fig 3. PCA9956B slave address
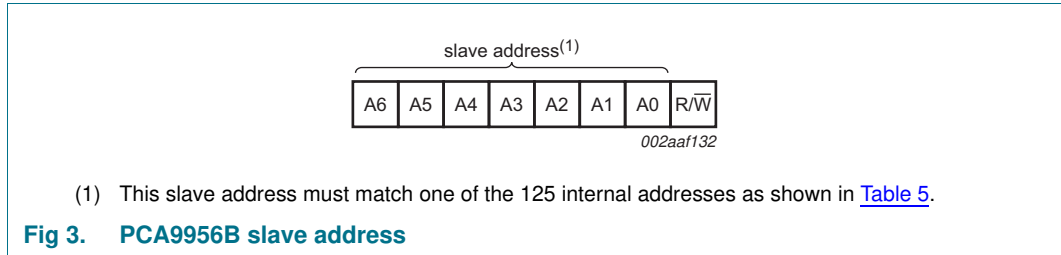
The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled. PCA9956B sends an ACK when E0h (R/$\overline{W}$ = 0) or E1h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.10 "ALLCALLADR, LED All Call I²C-bus address" for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000X) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All of the PCA9956Bs on the I²C-bus will acknowledge the address if sent by the I²C-bus master.

7.1.3 LED Sub Call I²C-bus addresses

- Three different I²C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: EEh or 1110 111X
  - SUBADR2 register: EEh or 1110 111X
  - SUBADR3 register: EEh or 1110 111X
- Programmable through I²C-bus (volatile programming)
- At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 I²C-bus addresses are disabled.

Remark: At power-up SUBADR1 identifies this device as a 24-channel driver.

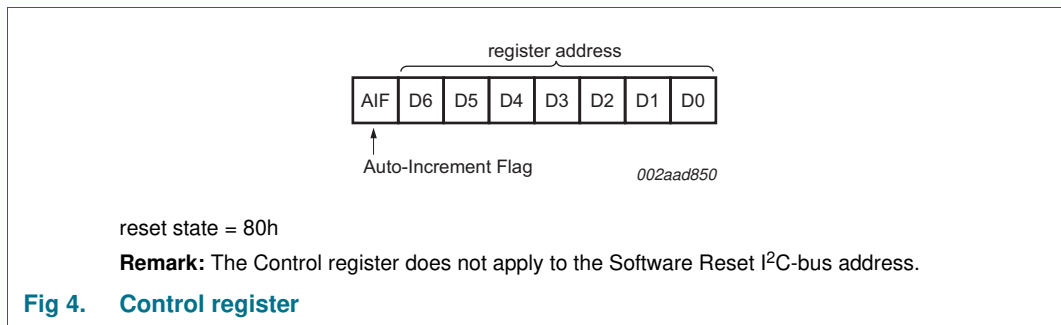See Section 7.3.9 "LED Sub Call I²C-bus addresses for PCA9956B" for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

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7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCA9956B, which will be stored in the Control register.

The lowest 7 bits are used as a pointer to determine which register will be accessed (D[6:0]). The highest bit is used as Auto-Increment Flag (AIF).

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature.

| AIF | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

register address

Auto-Increment Flag   002aad850

reset state = 80h

Remark: The Control register does not apply to the Software Reset I2C-bus address.

Fig 4.   Control register

When the Auto-Increment Flag is set (AIF = logic 1), the seven low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

Table 6.   Auto-Increment options

AIF	AI1[1]	AI0[1]	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for registers (00h to 3Eh). D[6:0] roll over to 00h after the last register 3Eh is accessed.
1	0	1	Auto-Increment for individual brightness registers only (0Ah to 21h). D[6:0] roll over to 0Ah after the last register (21h) is accessed.
1	1	0	Auto-Increment for MODE1 to IREF23 control registers (00h to 39h). D[6:0] roll over to 00h after the last register (39h) is accessed.
1	1	1	Auto-Increment for global control registers and individual brightness registers (08h to 21h). D[6:0] roll over to 08h after the last register (21h) is accessed.

[1]   AI1 and AI0 come from MODE1 register.

Remark: Other combinations not shown in Table 6 (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I2C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when all the registers must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 24 LED drivers must be individually programmed with different values during the same I2C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when MODE1 to IREF23 registers must be programmed with different settings during the same I2C-bus communication.

AIF + AI[1:0] = 111b is used when the 24 LED drivers must be individually programmed with different values in addition to global programming.

Only the 7 least significant bits D[6:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[6:0] is the first register that will be addressed (read or write operation), and can be anywhere between 00h and 3Eh (as defined in Table 7). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI0. See Table 6 for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1001 0000, then the register addressing sequence will be (in hexadecimal):
10 → 11 → … → 21 → 0A → 0B → … → 21 → 0A → 0B → … as long as the master keeps sending or reading data.

If MODE1 register bit AI1 = 0 and AI0 = 0 and if the Control register = 1010 0010, then the register addressing sequence will be (in hexadecimal):
22 → 23 → … → 3E → 00 → 01 → … → 21 → 0A → 0B → … as long as the master keeps sending or reading data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1000 0101, then the register addressing sequence will be (in hexadecimal):
05 → 06 → … → 21 → 0A → 0B → … → 21 → 0A → 0B → … as long as the master keeps sending or reading data.

Remark: Writing to registers marked 'not used' will return NACK.

7.3 Register definitions

Table 7.   Register summary

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	0	0	0	1	0	LEDOUT0	read/write	LED output state 0
03h	0	0	0	0	0	1	1	LEDOUT1	read/write	LED output state 1
04h	0	0	0	0	1	0	0	LEDOUT2	read/write	LED output state 2
05h	0	0	0	0	1	0	1	LEDOUT3	read/write	LED output state 3
06h	0	0	0	0	1	1	0	LEDOUT4	read/write	LED output state 4
07h	0	0	0	0	1	1	1	LEDOUT5	read/write	LED output state 5
08h	0	0	0	1	0	0	0	GRPPWM	read/write	group duty cycle control
09h	0	0	0	1	0	0	1	GRPFREQ	read/write	group frequency
0Ah	0	0	0	1	0	1	0	PWM0	read/write	brightness control LED0
0Bh	0	0	0	1	0	1	1	PWM1	read/write	brightness control LED1
0Ch	0	0	0	1	1	0	0	PWM2	read/write	brightness control LED2
0Dh	0	0	0	1	1	0	1	PWM3	read/write	brightness control LED3
0Eh	0	0	0	1	1	1	0	PWM4	read/write	brightness control LED4

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Table 7.   Register summary *…continued*

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
0Fh	0	0	0	1	1	1	1	PWM5	read/write	brightness control LED5
10h	0	0	1	0	0	0	0	PWM6	read/write	brightness control LED6
11h	0	0	1	0	0	0	1	PWM7	read/write	brightness control LED7
12h	0	0	1	0	0	1	0	PWM8	read/write	brightness control LED8
13h	0	0	1	0	0	1	1	PWM9	read/write	brightness control LED9
14h	0	0	1	0	1	0	0	PWM10	read/write	brightness control LED10
15h	0	0	1	0	1	0	1	PWM11	read/write	brightness control LED11
16h	0	0	1	0	1	1	0	PWM12	read/write	brightness control LED12
17h	0	0	1	0	1	1	1	PWM13	read/write	brightness control LED13
18h	0	0	1	1	0	0	0	PWM14	read/write	brightness control LED14
19h	0	0	1	1	0	0	1	PWM15	read/write	brightness control LED15
1Ah	0	0	1	1	0	1	0	PWM16	read/write	brightness control LED16
1Bh	0	0	1	1	0	1	1	PWM17	read/write	brightness control LED17
1Ch	0	0	1	1	1	0	0	PWM18	read/write	brightness control LED18
1Dh	0	0	1	1	1	0	1	PWM19	read/write	brightness control LED19
1Eh	0	0	1	1	1	1	0	PWM20	read/write	brightness control LED20
1Fh	0	0	1	1	1	1	1	PWM21	read/write	brightness control LED21
20h	0	1	1	0	0	0	0	PWM22	read/write	brightness control LED22
21h	0	1	1	0	0	0	1	PWM23	read/write	brightness control LED23
22h	0	1	0	0	0	1	0	IREF0	read/write	output gain control register 0
23h	0	1	0	0	0	1	1	IREF1	read/write	output gain control register 1
24h	0	1	0	0	1	0	0	IREF2	read/write	output gain control register 2
25h	0	1	0	0	1	0	1	IREF3	read/write	output gain control register 3
26h	0	1	0	0	1	1	0	IREF4	read/write	output gain control register 4
27h	0	1	0	0	1	1	1	IREF5	read/write	output gain control register 5
28h	0	1	0	1	0	0	0	IREF6	read/write	output gain control register 6
29h	0	1	0	1	0	0	1	IREF7	read/write	output gain control register 7
2Ah	0	1	0	1	0	1	0	IREF8	read/write	output gain control register 8
2Bh	0	1	0	1	0	1	1	IREF9	read/write	output gain control register 9
2Ch	0	1	0	1	1	0	0	IREF10	read/write	output gain control register 10
2Dh	0	1	0	1	1	0	1	IREF11	read/write	output gain control register 11
2Eh	0	1	0	1	1	1	0	IREF12	read/write	output gain control register 12
2Fh	0	1	0	1	1	1	1	IREF13	read/write	output gain control register 13
30h	0	1	1	0	0	0	0	IREF14	read/write	output gain control register 14
31h	0	1	1	0	0	0	1	IREF15	read/write	output gain control register 15
32h	0	1	1	0	0	1	0	IREF16	read/write	output gain control register 16
33h	0	1	1	0	0	1	1	IREF17	read/write	output gain control register 17
34h	0	1	1	0	1	0	0	IREF18	read/write	output gain control register 18
35h	0	1	1	0	1	0	1	IREF19	read/write	output gain control register 19
36h	0	1	1	0	1	1	0	IREF20	read/write	output gain control register 20

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Table 7.   Register summary *…continued*

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
37h	0	1	1	0	1	1	1	IREF21	read/write	output gain control register 21
38h	0	1	1	1	0	0	0	IREF22	read/write	output gain control register 22
39h	0	1	1	1	0	0	1	IREF23	read/write	output gain control register 23
3Ah	0	1	1	1	0	1	0	OFFSET	read/write	Offset/delay on LEDn outputs
3Bh	0	1	1	1	0	1	1	SUBADR1	read/write	I2C-bus subaddress 1
3Ch	0	1	1	1	1	0	0	SUBADR2	read/write	I2C-bus subaddress 2
3Dh	0	1	1	1	1	0	1	SUBADR3	read/write	I2C-bus subaddress 3
3Eh	0	1	1	1	1	1	0	ALLCALLADR	read/write	All Call I2C-bus address
3Fh	0	1	1	1	1	1	1	PWMALL	write only	brightness control for all LEDn
40h	1	0	0	0	0	0	0	IREFALL	write only	output gain control for all registers IREF0 to IREF23
41h	1	0	0	0	0	0	1	EFLAG0	read only	output error flag 0
42h	1	0	0	0	0	1	0	EFLAG1	read only	output error flag 1
43h	1	0	0	0	0	1	1	EFLAG2	read only	output error flag 2
44h	1	0	0	0	1	0	0	EFLAG3	read only	output error flag 3
45h	1	0	0	0	1	0	1	EFLAG4	read only	output error flag 4
46h	1	0	0	0	1	1	0	EFLAG5	read only	output error flag 5
47h to 7Fh								reserved	read only	not used[1]

[1]   Reserved registers should not be written to and will always read back as zeros.

7.3.1 MODE1 — Mode register 1

Table 8.   MODE1 - Mode register 1 (address 00h) bit description
Legend: * default value.

Bit	Symbol	Access	Value	Description
7	AIF	read only	0	Register Auto-Increment disabled.
			1*	Register Auto-Increment enabled.
6	AI1	R/W	0*	Auto-Increment bit 1 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 1 = 1. Auto-increment range as defined in Table 6.
5	AI0	R/W	0*	Auto-Increment bit 0 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 0 = 1. Auto-increment range as defined in Table 6.
4	SLEEP	R/W	0*	Normal mode[1].
			1	Low power mode. Oscillator off[2][3].
3	SUB1	R/W	0	PCA9956B does not respond to I2C-bus subaddress 1.
			1*	PCA9956B responds to I2C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9956B does not respond to I2C-bus subaddress 2.
			1	PCA9956B responds to I2C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9956B does not respond to I2C-bus subaddress 3.
			1	PCA9956B responds to I2C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9956B does not respond to LED All Call I2C-bus address.
			1*	PCA9956B responds to LED All Call I2C-bus address.

[1]   It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2]   No blinking or dimming is possible when the oscillator is off.

[3]   The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

7.3.2 MODE2 — Mode register 2

Table 9.   MODE2 - Mode register 2 (address 01h) bit description
Legend: * default value.

Bit	Symbol	Access	Value	Description
7	OVERTEMP	read only	0*	O.K.
			1	overtemperature condition
6	ERROR	read only	0*	no error at LED outputs
			1	any open or short-circuit detected in error flag registers (EFLAGn)
5	DMBLNK	R/W	0*	group control = dimming
			1	group control = blinking
4	CLRERR	write only	0*	self clear after write '1'
			1	Write '1' to clear all error status bits in EFLAGn register and ERROR (bit 6). The EFLAGn and ERROR bit will set to '1' if open or short-circuit is detected again.
3	OCH	R/W	0*	outputs change on STOP command
			1	outputs change on ACK

Table 9. **MODE2 - Mode register 2 (address 01h) bit description** *…continued*
*Legend: * default value.*

Bit	Symbol	Access	Value	Description
2	-	read only	1*	reserved
1	-	read only	0*	reserved
0	-	read only	1*	reserved

7.3.3 LEDOUT0 to LEDOUT5, LED driver output state

Table 10. **LEDOUT0 to LEDOUT5 - LED driver output state registers (address 02h to 07h) bit description**
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	LEDOUT0	7:6	LDR3	R/W	10*	LED3 output state control
		5:4	LDR2	R/W	10*	LED2 output state control
		3:2	LDR1	R/W	10*	LED1 output state control
		1:0	LDR0	R/W	10*	LED0 output state control
03h	LEDOUT1	7:6	LDR7	R/W	10*	LED7 output state control
		5:4	LDR6	R/W	10*	LED6 output state control
		3:2	LDR5	R/W	10*	LED5 output state control
		1:0	LDR4	R/W	10*	LED4 output state control
04h	LEDOUT2	7:6	LDR11	R/W	10*	LED11 output state control
		5:4	LDR10	R/W	10*	LED10 output state control
		3:2	LDR9	R/W	10*	LED9 output state control
		1:0	LDR8	R/W	10*	LED8 output state control
05h	LEDOUT3	7:6	LDR15	R/W	10*	LED15 output state control
		5:4	LDR14	R/W	10*	LED14 output state control
		3:2	LDR13	R/W	10*	LED13 output state control
		1:0	LDR12	R/W	10*	LED12 output state control
06h	LEDOUT4	7:6	LDR19	R/W	10*	LED19 output state control
		5:4	LDR18	R/W	10*	LED18 output state control
		3:2	LDR17	R/W	10*	LED17 output state control
		1:0	LDR16	R/W	10*	LED16 output state control
07h	LEDOUT5	7:6	LDR23	R/W	10*	LED23 output state control
		5:4	LDR22	R/W	10*	LED22 output state control
		3:2	LDR21	R/W	10*	LED21 output state control
		1:0	LDR20	R/W	10*	LED20 output state control

LDRx = 00 — LED driver x is off (x = 0 to 23).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled). The $\overline{OE}$ pin can be used as external dimming/blinking control in this state.

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register (default power-up state) or PWMALL register for all LEDn outputs.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

Remark: Setting the device in low power mode while being on group dimming/blinking mode may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

7.3.4 GRPPWM, group duty cycle control

Table 11.   GRPPWM - Group brightness control register (address 08h) bit description
*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
08h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 24 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT5 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle\ =\ \frac{GDC[7:0]}{256} \tag{1}$$

7.3.5 GRPFREQ, group frequency

Table 12.   GRPFREQ - Group frequency register (address 09h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT5 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period\ =\ \frac{GFRQ[7:0]+1}{15.26}(s) \tag{2}$$

7.3.6 PWM0 to PWM23, individual brightness control

Table 13.   PWM0 to PWM23 - PWM registers 0 to 23 (address 0Ah to 21h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
0Bh	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
0Ch	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
0Dh	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
0Eh	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
0Fh	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
10h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
11h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle
12h	PWM8	7:0	IDC8[7:0]	R/W	0000 0000*	PWM8 Individual Duty Cycle
13h	PWM9	7:0	IDC9[7:0]	R/W	0000 0000*	PWM9 Individual Duty Cycle
14h	PWM10	7:0	IDC10[7:0]	R/W	0000 0000*	PWM10 Individual Duty Cycle
15h	PWM11	7:0	IDC11[7:0]	R/W	0000 0000*	PWM11 Individual Duty Cycle
16h	PWM12	7:0	IDC12[7:0]	R/W	0000 0000*	PWM12 Individual Duty Cycle
17h	PWM13	7:0	IDC13[7:0]	R/W	0000 0000*	PWM13 Individual Duty Cycle
18h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000*	PWM14 Individual Duty Cycle
19h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000*	PWM15 Individual Duty Cycle
1Ah	PWM16	7:0	IDC16[7:0]	R/W	0000 0000*	PWM16 Individual Duty Cycle
1Bh	PWM17	7:0	IDC17[7:0]	R/W	0000 0000*	PWM17 Individual Duty Cycle
1Ch	PWM18	7:0	IDC18[7:0]	R/W	0000 0000*	PWM18 Individual Duty Cycle
1Dh	PWM19	7:0	IDC19[7:0]	R/W	0000 0000*	PWM19 Individual Duty Cycle
1Eh	PWM20	7:0	IDC20[7:0]	R/W	0000 0000*	PWM20 Individual Duty Cycle
1Fh	PWM21	7:0	IDC21[7:0]	R/W	0000 0000*	PWM21 Individual Duty Cycle
20h	PWM22	7:0	IDC22[7:0]	R/W	0000 0000*	PWM22 Individual Duty Cycle
21h	PWM23	7:0	IDC23[7:0]	R/W	0000 0000*	PWM23 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT5 registers).

$$duty\ cycle\ =\ \frac{IDCx[7:0]}{256} \tag{3}$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM will not have effective brightness control of LEDs due to edge rate control of LED output pins.

7.3.7 IREF0 to IREF23, LED output current value registers

These registers reflect the gain settings for output current for LED0 to LED23.

Table 14.   IREF0 to IREF23 - LED output gain control registers (address 22h to 39h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
22h	IREF0	7:0	R/W	00h*	LED0 output current setting
23h	IREF1	7:0	R/W	00h*	LED1 output current setting
24h	IREF2	7:0	R/W	00h*	LED2 output current setting
25h	IREF3	7:0	R/W	00h*	LED3 output current setting
26h	IREF4	7:0	R/W	00h*	LED4 output current setting
27h	IREF5	7:0	R/W	00h*	LED5 output current setting
28h	IREF6	7:0	R/W	00h*	LED6 output current setting
29h	IREF7	7:0	R/W	00h*	LED7 output current setting
2Ah	IREF8	7:0	R/W	00h*	LED8 output current setting
2Bh	IREF9	7:0	R/W	00h*	LED9 output current setting
2Ch	IREF10	7:0	R/W	00h*	LED10 output current setting
2Dh	IREF11	7:0	R/W	00h*	LED11 output current setting
2Eh	IREF12	7:0	R/W	00h*	LED12 output current setting
2Fh	IREF13	7:0	R/W	00h*	LED13 output current setting
30h	IREF14	7:0	R/W	00h*	LED14 output current setting
31h	IREF15	7:0	R/W	00h*	LED15 output current setting
32h	IREF16	7:0	R/W	00h*	LED16 output current setting
33h	IREF17	7:0	R/W	00h*	LED17 output current setting
34h	IREF18	7:0	R/W	00h*	LED18 output current setting
35h	IREF19	7:0	R/W	00h*	LED19 output current setting
36h	IREF20	7:0	R/W	00h*	LED20 output current setting
37h	IREF21	7:0	R/W	00h*	LED21 output current setting
38h	IREF22	7:0	R/W	00h*	LED22 output current setting
39h	IREF23	7:0	R/W	00h*	LED23 output current setting

7.3.8 OFFSET — LEDn output delay offset register

Table 15.   OFFSET - LEDn output delay offset register (address 3Ah) bit description
*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Ah	OFFSET	7:4	read only	0000*	not used
		3:0	R/W	1000*	LEDn output delay offset factor

The PCA9956B can be programmed to have turn-on delay between LED outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

The order in which the LED outputs are enabled will always be the same (channel 0 will enable first and channel 23 will enable last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows:

0000 = no delay between outputs (all on, all off at the same time)

0001 = delay of 1 clock cycle (125 ns) between successive outputs

0010 = delay of 2 clock cycles (250 ns) between successive outputs

0011 = delay of 3 clock cycles (375 ns) between successive outputs

:

0111 = delay of 7 clock cycles (875 ns) between successive outputs

1000 = delay of 8 clock cycles (1 μs) between successive outputs

1001 = delay of 9 clock cycles (1.125 μs) between successive outputs

1010 = delay of 10 clock cycles (1.25 μs) between successive outputs

1011 = delay of 11 clock cycles (1.375 μs) between successive outputs

1100 to 1111 = reserved and do not use

Example: If the value in the OFFSET register is 1000 the corresponding delay = 8×125 ns = 1 μs delay between successive outputs.

channel 0 turns on at time 0 μs

channel 1 turns on at time 1 μs

channel 2 turns on at time 2 μs

channel 3 turns on at time 3 μs

channel 4 turns on at time 4 μs

channel 5 turns on at time 5 μs

channel 6 turns on at time 6 μs

channel 7 turns on at time 7 μs

channel 8 turns on at time 8 μs

channel 9 turns on at time 9 μs

channel 10 turns on at time 10 μs

channel 11 turns on at time 11 μs

channel 12 turns on at time 12 μs

channel 13 turns on at time 13 μs

channel 14 turns on at time 14 μs

channel 15 turns on at time 15 μs

channel 16 turns on at time 16 μs

channel 17 turns on at time 17 μs

channel 18 turns on at time 18 μs

channel 19 turns on at time 19 μs

channel 20 turns on at time 20 μs

channel 21 turns on at time 21 μs

channel 22 turns on at time 22 μs

channel 23 turns on at time 23 μs

7.3.9 LED Sub Call I²C-bus addresses for PCA9956B

Table 16.   SUBADR1 to SUBADR3 - I²C-bus subaddress registers 1 to 3 (address 3Bh to 3Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Bh	SUBADR1	7:1	A1[7:1]	R/W	1110 111*	I²C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
3Ch	SUBADR2	7:1	A2[7:1]	R/W	1110 111*	I²C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
3Dh	SUBADR3	7:1	A3[7:1]	R/W	1110 111*	I²C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Default power-up values are EEh, EEh, EEh. At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 are disabled. The power-up default bit subaddress of EEh indicates that this device is a 24-channel LED driver.

All three subaddresses are programmable. Once subaddresses have been programmed to their right values, SUBx bits need to be set to logic 1 in order to have the device acknowledging these addresses (MODE1 register) (0). When SUBx is set to logic 1, the corresponding I²C-bus subaddress can be used during either an I²C-bus read or write sequence.

7.3.10 ALLCALLADR, LED All Call I²C-bus address

Table 17.   ALLCALLADR - LED All Call I²C-bus address register (address 3Eh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Eh	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I²C-bus address register
		0	AC[0]	R only	0*	reserved

The LED All Call I²C-bus address allows all the PCA9956Bs on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to logic 1 [power-up default state]). This address is programmable through the I²C-bus and can be used during either an I²C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0 in MODE1 register, the device does not acknowledge the address programmed in register ALLCALLADR.

7.3.11 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register will be used for PWM duty cycle for all the LEDn outputs and will be reflected in PWM 0 through PWM23 registers.

Table 18.   PWMALL - brightness control for all LEDn outputs register (address 3Fh) bit description
*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Fh	PWMALL	7:0	write only	0000 0000*	duty cycle for all LEDn outputs

Remark: Write to any of the PWM0 to PWM23 registers will overwrite the value in corresponding PWMn register programmed by PWMALL.

7.3.12 IREFALL register: output current value for all LED outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LED outputs will be set to a current corresponding to this register value.

Writes to IREF0 to IREF23 will overwrite the output current settings.

Table 19.   IREFALL - Output gain control for all LED outputs (address 40h) bit description
*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
40h	IREFALL	7:0	write only	00h*	Current gain setting for all LED outputs.

7.3.13 LED driver constant current outputs

In LED display applications, PCA9956B provides nearly no current variations from channel to channel and from device to device. The maximum current skew between channels is less than ±4 % and less than ±6 % between devices.
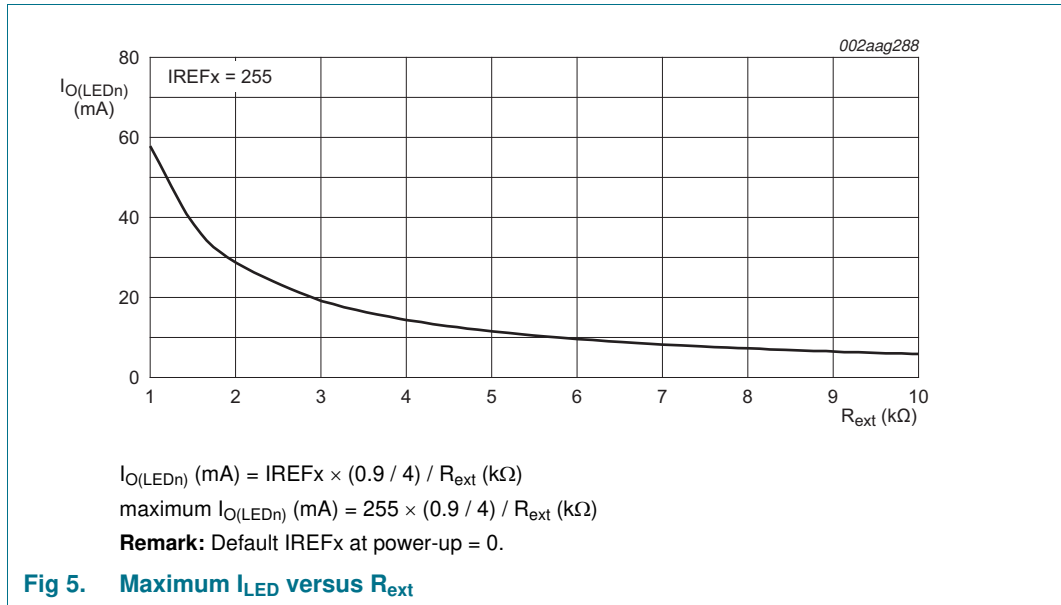
7.3.13.1 Adjusting output current

The PCA9956B scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_O) at each output port. The maximum output current for the outputs can be set using R_{ext}. In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF23. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

Equation 4 and Equation 5 can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O\_LED\_MIN = \frac{900\ mV}{R_{ext}} \times \frac{1}{4}\ (\text{minimum constant current}) \tag{4}$$

$$I_O\_LED\_MAX = (255 \times I_O\_LED\_MIN) = \left(\frac{900\ mV}{R_{ext}} \times \frac{255}{4}\right) \tag{5}$$

For a given IREFx setting, $I_O\_LED = IREFx \times \dfrac{900\ mV}{R_{ext}} \times \dfrac{1}{4}$.

$$I_{O(LEDn)} \text{ (mA)} = IREFx \times (0.9 / 4) / R_{ext} \text{ (k}\Omega\text{)}$$

$$\text{maximum } I_{O(LEDn)} \text{ (mA)} = 255 \times (0.9 / 4) / R_{ext} \text{ (k}\Omega\text{)}$$

Remark: Default IREFx at power-up = 0.

Fig 5.   Maximum I_{LED} versus R_{ext}

Example 1: If R_{ext} = 1 kΩ, I_O_LED_MIN = 225 μA, I_O_LED_MAX = 57.375 mA (as shown in Figure 6).

So each channel can be programmed with its individual IREFx in 256 steps and in 225 μA increments to a maximum output current of 57.375 mA independently.

Fig 6. $I_{O(target)}$ versus IREFx value with R_{ext} = 1 kΩ
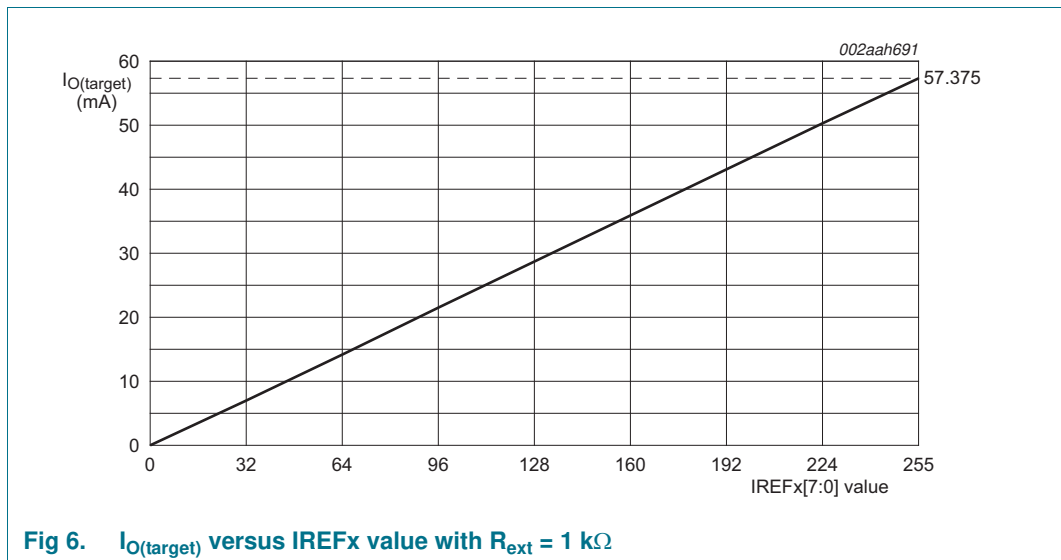
Example 2: If R_{ext} = 2 kΩ, I_O_LED_MIN = 112.5 μA, I_O_LED_MAX = 28.687 mA (as shown in Figure 7).

So each channel can be programmed with its individual IREFx in 256 steps and in 112.5 μA increments to a maximum output channel of 28.687 mA independently.
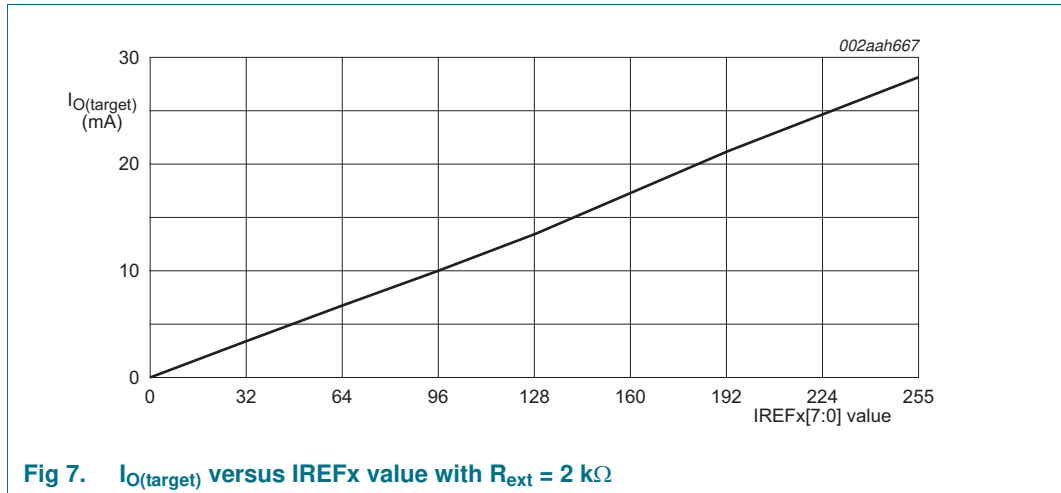
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Fig 7. **I$_{O(target)}$ versus IREFx value with R$_{ext}$ = 2 kΩ**

7.3.14 LED error detection

The PCA9956B is capable of detecting an LED open or a short condition at its open-drain LED outputs. Users will recognize these faults by reading the status of a pair of error bits (ERRx) in error flag registers (EFLAGn) for each channel. Both LDRx value in LEDOUTx registers and IREFx value must be set to '00' for those unused LED output channels. If the output is selected to be fully on, individual dim, or individual and group dim, that channel will be tested.

The user can poll the ERROR status bit (bit 6 in MODE2 register) to check if there is a fault condition in any of the 24 channels. The EFLAGn registers can then be read to determine which channels are at fault and the type of fault in those channels. The error status reported by the EFLAGn register is real time information that will get self cleared once the error is fixed and write '1' to CLRERR (bit 4 in MODE2 register).

Remark: Checks for open and short-circuit will not occur if the PWM value in PWM0 to PWM23 registers is less than 8.

Table 20. EFLAG0 to EFLAG5 - Error flag registers (address 41h to 46h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
41h	EFLAG0	7:6	ERR3	R only	00*	Error status for LED3 output
		5:4	ERR2	R only	00*	Error status for LED2 output
		3:2	ERR1	R only	00*	Error status for LED1 output
		1:0	ERR0	R only	00*	Error status for LED0 output
42h	EFLAG1	7:6	ERR7	R only	00*	Error status for LED7 output
		5:4	ERR6	R only	00*	Error status for LED6 output
		3:2	ERR5	R only	00*	Error status for LED5 output
		1:0	ERR4	R only	00*	Error status for LED4 output
43h	EFLAG2	7:6	ERR11	R only	00*	Error status for LED11 output
		5:4	ERR10	R only	00*	Error status for LED10 output
		3:2	ERR9	R only	00*	Error status for LED9 output
		1:0	ERR8	R only	00*	Error status for LED8 output

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