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PCAL6408A

Low-voltage translating, 8-bit I²C-bus/SMBus I/O expander with interrupt output, reset, and configuration registers

Rev. 3.2 — 19 April 2017 Product data sheet

1. General description

The PCAL6408A is an 8-bit general-purpose I/O expander that provides remote I/O expansion for most microcontroller families via the I²C-bus interface.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level to I/O devices operating at a different (usually higher) voltage level. The PCAL6408A has built-in level shifting feature that makes these devices extremely flexible in mixed signal environments where communication between incompatible I/O voltages is required.

Its wide V_{DD} range of 1.65 V to 5.5 V on the dual power rail allows seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL6408A: $V_{DD(I2C\text{-}bus)}$ and $V_{DD(P)}$. $V_{DD(I2C\text{-}bus)}$ provides the supply voltage for the interface at the master side (for example, a microcontroller) and the $V_{DD(P)}$ provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCAL6408A is provided through $V_{DD(I2C\text{-}bus)}$. $V_{DD(I2C\text{-}bus)}$ should be connected to the V_{DD} of the external SCL/SDA lines. This indicates the V_{DD} level of the I²C-bus to the PCAL6408A, while the voltage level on Port P of the PCAL6408A is determined by the $V_{DD(P)}$.

The PCAL6408A contains the PCA6408A register set of 8-bit Configuration, Input, Output, and Polarity Inversion registers and additionally, the PCAL6408A has Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs. The PCAL6408A is a pin-to-pin replacement to the PCA6408A, however, the PCAL6408A powers up with all I/O interrupts masked. This mask default allows for a board bring-up free of spurious interrupts at power-up.

At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.

The system master can reset the PCAL6408A in the event of a time-out or other improper operation by asserting a LOW in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I²C-bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the part.

The PCAL6408A open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCAL6408A can remain a simple slave device. The input latch feature holds or latches the input pin state and keeps the logic values that created the interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I²C-bus address and allow up to two devices to share the same I²C-bus or SMBus.

2. Features and benefits

- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- Low standby current consumption of 1 μA
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.25 V (typical) at 2.5 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
  - V_{hys} = 0.5 V (typical) at 5 V
- 5 V tolerant I/O ports
- Active LOW reset input ($\overline{\text{RESET}}$)
- Open-drain active LOW interrupt output ($\overline{\text{INT}}$)
- 400 kHz Fast-mode I²C-bus
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II

- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: HVQFN16, TSSOP16, XQFN16, XFBGA16 (1.6 mm × 1.6 mm × 0.5 mm), X2QFN16 (LGA, Land Grid Array) 1.6 mm x 1.6 mm x 0.35 mm

2.1 Agile I/O features

- Software backward compatible with PCA6408A with interrupts disabled at power-up
- Pin-to-pin drop-in replacement for PCA6408A
- Output port configuration: bank selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/pull-down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCAL6408ABS	L8A	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCAL6408APW	PL6408A	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCAL6408AHK	L8	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	SOT1161-1
PCAL6408AEX	L8	XFBGA16[1]	plastic, extremely thin fine-pitch ball grid array package; 16 balls; body 1.6 × 1.6 × 0.5 mm	SOT1354-1
PCAL6408AEX1	18X[2]	X2QFN16	plastic, thermal enhanced super thin land grid array or quad flat package; no leads; 16 terminals; body 1.6 × 1.6 × 0.35 mm	SOT1896-1

[1] XFBGA16 package is discontinued with lifetime buy November 2016; new designs must use X2QFN16 package.

[2] “X” rotates from 1 to 5 and indicates the work week of the indicated month

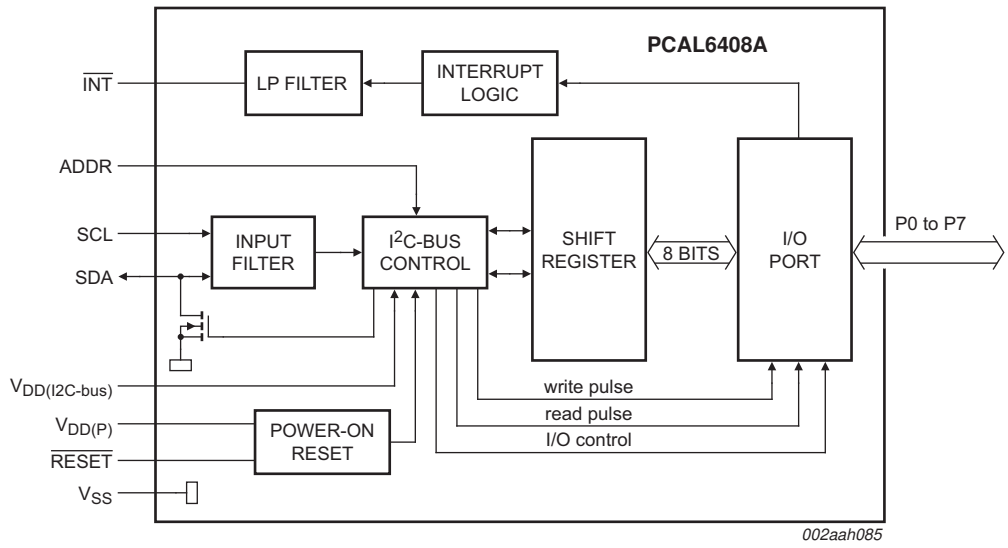
3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCAL6408ABS	PCAL6408ABSHP	HVQFN16	Reel 13” Q2/T3 *standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCAL6408APW	PCAL6408APWJ	TSSOP16	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCAL6408AHK	PCAL6408AHKX	XQFN16	Reel 7” Q1/T1 *standard mark SMD	4000	T_{amb} = −40 °C to +85 °C
PCAL6408AEX	PCAL6408AEXX	XFBGA16[1]	Reel 7” Q1/T1 *standard mark SMD	5000	T_{amb} = −40 °C to +85 °C
PCAL6408AEX1	PCAL6408AEX1Z	X2QFN16	Reel 7” Q2/T1 *standard mark SMD	5000	T_{amb} = −40 °C to +85 °C

[1] XFBGA16 package is discontinued with lifetime buy November 2016; new designs must use X2QFN16 package.

4. Block diagram



All I/Os are set to inputs at reset.

Fig 1. Block diagram (positive logic)

5. Pinning information

5.1 Pinning

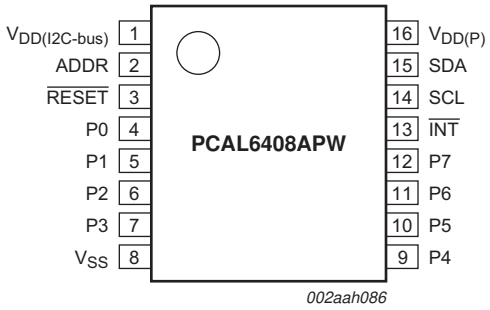
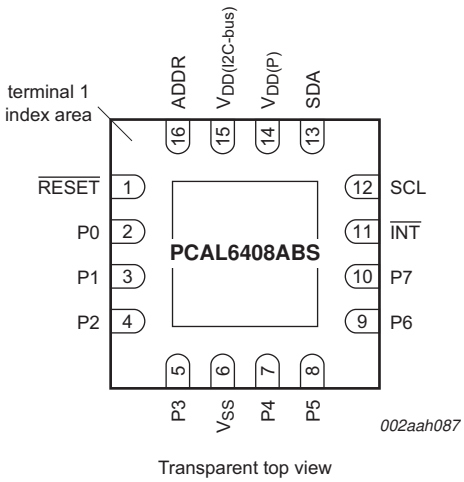


Fig 2. Pin configuration for TSSOP16



The exposed center pad, if used, must be connected only as a secondary V_{SS} or must be left electrically open.

Fig 3. Pin configuration for HVQFN16

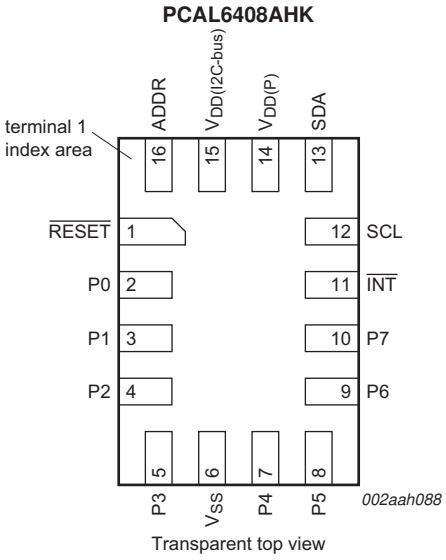
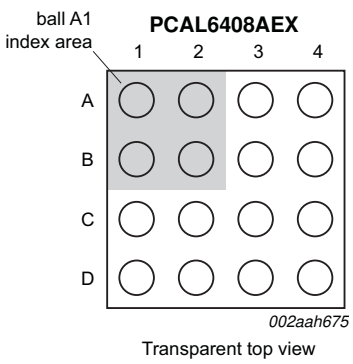
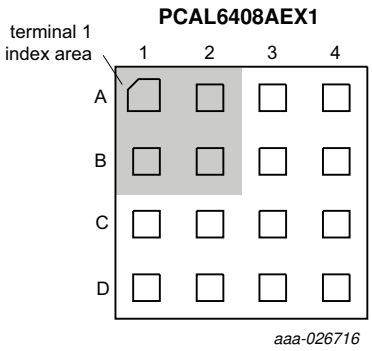


Fig 4. Pin configuration for XQFN16



Transparent top view

Fig 5. Pin configuration for 1.6 mm × 1.6 mm XFBGA16



Transparent top view

Fig 6. Pin configuration for 1.6 mm × 1.6 mm X2QFN16 EX1 land grid array

	1	2	3	4
A	RESET	$V_{DD(I2C\text{-}bus)}$	$V_{DD(P)}$	SCL
B	P0	ADDR	SDA	$\overline{INT}$
C	P2	P1	P7	P6
D	P3	V_{SS}	P4	P5

002aah676

Transparent top view

Fig 7. Ball mapping for 1.6 mm × 1.6 mm XFBGA16/X2QFN16

5.2 Pin description

Table 3. Pin description

Symbol	Pin				Description
	TSSOP16	HVQFN16	XQFN16	XFBGA16, X2QFN16	
$V_{DD(I2C\text{-}bus)}$	1	15	15	A2	Supply voltage of I²C-bus. Connect directly to the V_{DD} of the external I²C master. Provides voltage-level translation.
ADDR	2	16	16	B2	Address input. Connect directly to $V_{DD(P)}$ or ground.
$\overline{RESET}$	3	1	1	A1	Active LOW reset input. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor if no active connection is used.
P0[1]	4	2	2	B1	Port P input/output 0.
P1[1]	5	3	3	C2	Port P input/output 1.
P2[1]	6	4	4	C1	Port P input/output 2.
P3[1]	7	5	5	D1	Port P input/output 3.
V_{SS}	8	6	6	D2	Ground.
P4[1]	9	7	7	D3	Port P input/output 4.
P5[1]	10	8	8	D4	Port P input/output 5.
P6[1]	11	9	9	C4	Port P input/output 6.

Table 3. Pin description *…continued*

Symbol	Pin				Description
	TSSOP16	HVQFN16	XQFN16	XFBGA16, X2QFN16	
P7[1]	12	10	10	C3	Port P input/output 7.
$\overline{INT}$	13	11	11	B4	Interrupt output. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
SCL	14	12	12	A4	Serial clock bus. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
SDA	15	13	13	B3	Serial data bus. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
$V_{DD(P)}$	16	14	14	A3	Supply voltage of PCAL6408A for Port P.

[1] All I/O are configured as input at power-on.

6. Voltage translation

Table 4 shows how to set up V_{DD} levels for the necessary voltage translation between the I²C-bus and the PCAL6408A.

Table 4. Voltage translation

$V_{DD(I2C-bus)}$ (SDA and SCL of I²C master)	$V_{DD(P)}$ (Port P)
1.8 V	1.8 V
1.8 V	2.5 V
1.8 V	3.3 V
1.8 V	5 V
2.5 V	1.8 V
2.5 V	2.5 V
2.5 V	3.3 V
2.5 V	5 V
3.3 V	1.8 V
3.3 V	2.5 V
3.3 V	3.3 V
3.3 V	5 V
5 V	1.8 V
5 V	2.5 V
5 V	3.3 V
5 V	5 V

7. Functional description

Refer to Figure 1 “Block diagram (positive logic)”.

7.1 Device address

The address of the PCAL6408A is shown in Figure 8.

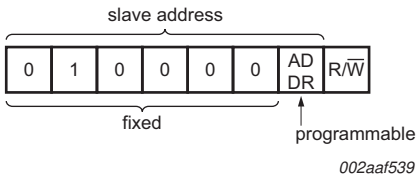


Fig 8. PCAL6408A address

ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible slave addresses. The last bit of the slave address defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

7.2 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C-bus slave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

7.3 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCAL6408A. 2 bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that are affected. Bit 6 in conjunction with the lower 3 bits of the Command byte are used to point to the extended features of the device (Agile I/O). This register is 'write only'.

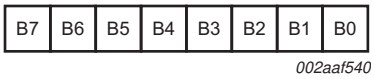


Fig 9. Pointer register bits

Table 6. Command byte

Pointer register bits								Command byte	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Output port	read/write byte	1111 1111
0	0	0	0	0	0	1	0	02h	Polarity Inversion	read/write byte	0000 0000
0	0	0	0	0	0	1	1	03h	Configuration	read/write byte	1111 1111
0	1	0	0	0	0	0	0	40h	Output drive strength 0	read/write byte	1111 1111
0	1	0	0	0	0	0	1	41h	Output drive strength 1	read/write byte	1111 1111
0	1	0	0	0	0	1	0	42h	Input latch	read/write byte	0000 0000
0	1	0	0	0	0	1	1	43h	Pull-up/pull-down enable	read/write byte	0000 0000
0	1	0	0	0	1	0	0	44h	Pull-up/pull-down selection	read/write byte	1111 1111
0	1	0	0	0	1	0	1	45h	Interrupt mask	read/write byte	1111 1111
0	1	0	0	0	1	1	0	46h	Interrupt status	read byte	0000 0000
0	1	0	0	1	1	1	1	4Fh	Output port configuration	read/write byte	0000 0000

[1] Undefined.

7.4 Register descriptions

7.4.1 Input port register (00h)

The Input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port register is read only; writes to this register have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 8.2 "Read commands".

Table 7. Input port register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

7.4.2 Output port register (01h)

The Output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from this register reflect the value that was written to this register, **not** the actual pin value.

Table 8. Output port register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

7.4.3 Polarity inversion register (02h)

The Polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Table 9. Polarity inversion register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

7.4.4 Configuration register (03h)

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 10. Configuration register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

7.4.5 Output drive strength registers (40h, 41h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example, Port 7 is controlled by register 41 CC7 (bits [7:6]), Port 6 is controlled by register 41 CC6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See Section 9.2 “Output drive strength control” for more details.

Table 11. Current control register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC3		CC2		CC1		CC0	
Default	1	1	1	1	1	1	1	1

Table 12. Current control register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC7		CC6		CC5		CC4	
Default	1	1	1	1	1	1	1	1

7.4.6 Input latch register (42h)

The Input latch register enables and disables the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input port register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared. See Figure 14.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 15. For example, if the P4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port register captures this change and an interrupt is generated (if unmasked). When the read is performed on the input port register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port register reads ‘1’. The next read of the input port register bit 4 should now read ‘0’.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input port register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input port register reflects the latched logic level.

Table 13. Input latch register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	L7	L6	L5	L4	L3	L2	L1	L0
Default	0	0	0	0	0	0	0	0

7.4.7 Pull-up/pull-down enable register (43h)

This register allows the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors are disconnected when the outputs are configured as open-drain outputs (see Section 7.4.11). Use the pull-up/pull-down selection registers to select either a pull-up or pull-down resistor.

Table 14. Pull-up/pull-down enable register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

7.4.8 Pull-up/pull-down selection register (44h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register has no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ.

Table 15. Pull-up/pull-down selection register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD7	PUD6	PUD5	PUD4	PUD3	PUD2	PUD1	PUD0
Default	1	1	1	1	1	1	1	1

7.4.9 Interrupt mask register (45h)

Interrupt mask register is set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin ($\overline{INT}$) is not asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin is asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 causes the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin is de-asserted.

Table 16. Interrupt mask register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	M7	M6	M5	M4	M3	M2	M1	M0
Default	1	1	1	1	1	1	1	1

7.4.10 Interrupt status register (46h)

This read-only register is used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit returns logic 0.

Table 17. Interrupt status register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	S7	S6	S5	S4	S3	S2	S1	S0
Default	0	0	0	0	0	0	0	0

7.4.11 Output port configuration register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 10). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (4Fh) before the Configuration register (03h) sets the port pins as outputs.

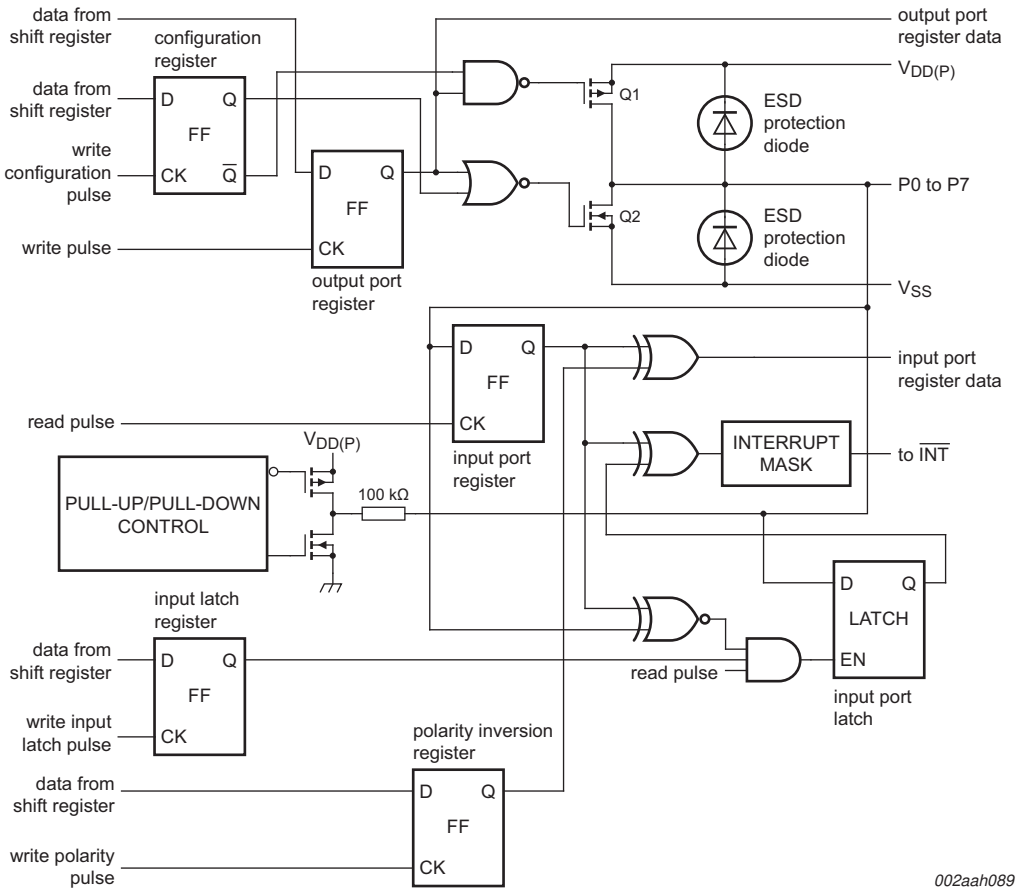
Table 18. Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							ODEN
Default	0	0	0	0	0	0	0	0

7.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig 10. Simplified schematic of the I/Os (P0 to P7)

7.6 Power-on reset

When power (from 0 V) is applied to $V_{DD(P)}$, an internal power-on reset holds the PCAL6408A in a reset condition until $V_{DD(P)}$ has reached V_{POR}. At that time, the reset condition is released and the PCAL6408A registers and I²C-bus/SMBus state machine initialize to their default states. After that, $V_{DD(P)}$ must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. See Section 9.3 “Power-on reset requirements”.

7.7 Reset input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCAL6408A registers and I²C-bus/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is LOW (0). When $\overline{\text{RESET}}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to $V_{DD(I2C-bus)}$ if no active connection is used.

7.8 Interrupt output ($\overline{\text{INT}}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt (see Figure 14). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input port register.

The $\overline{\text{INT}}$ output has an open-drain structure and requires a pull-up resistor to $V_{DD(P)}$ or $V_{DD(I2C-bus)}$ depending on the application. $\overline{\text{INT}}$ should be connected to the voltage source of the device that requires the interrupt information. When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

8. Bus transactions

The PCAL6408A is an I²C-bus slave device. Data is exchanged between the master and PCAL6408A through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Write commands

Data is transmitted to the PCAL6408A by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 8 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

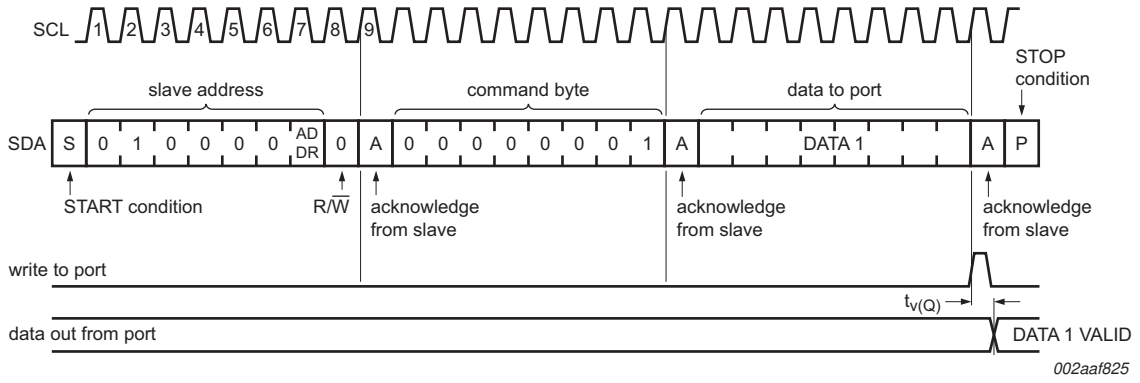


Fig 11. Write to Output port register

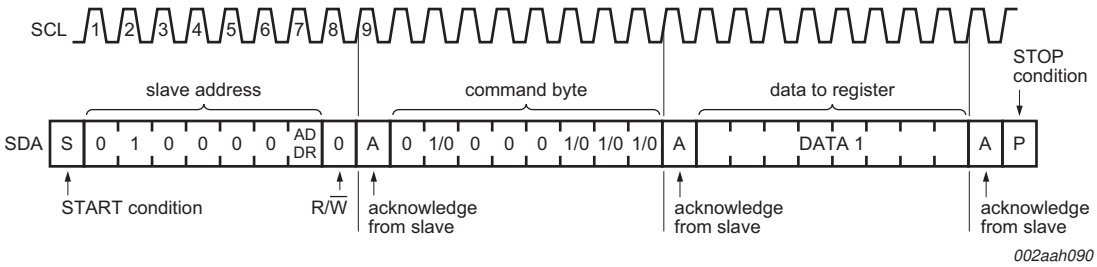


Fig 12. Write to Configuration or Polarity inversion registers

8.2 Read commands

To read data from the PCAL6408A, the bus master must first send the PCAL6408A address with the least significant bit set to a logic 0 (see Figure 8 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCAL6408A (see Figure 13 and Figure 14).

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

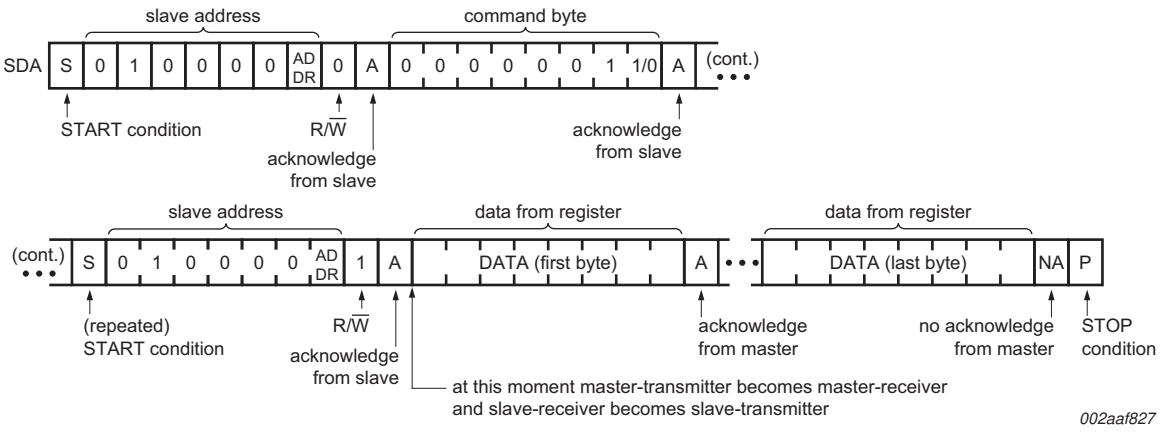
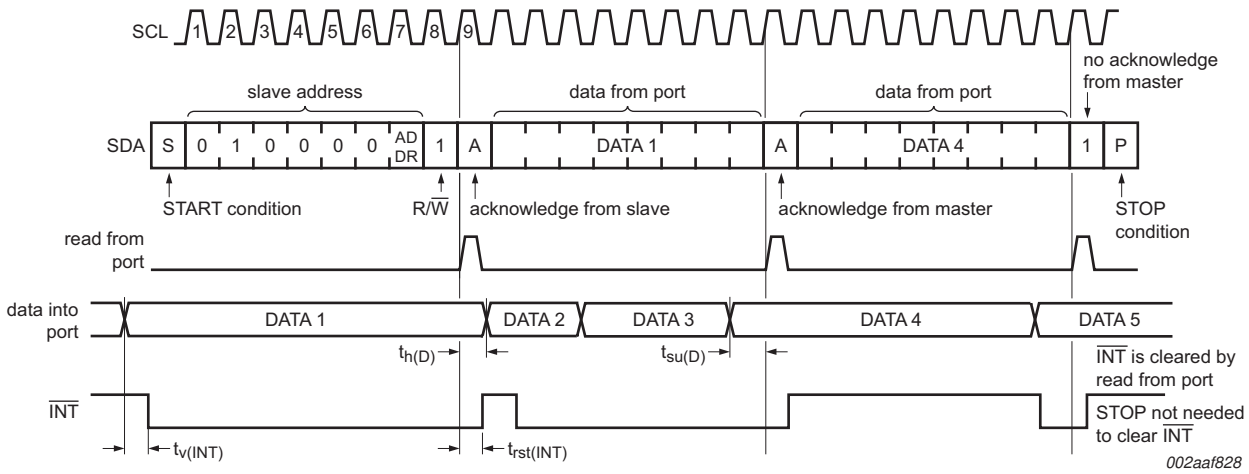


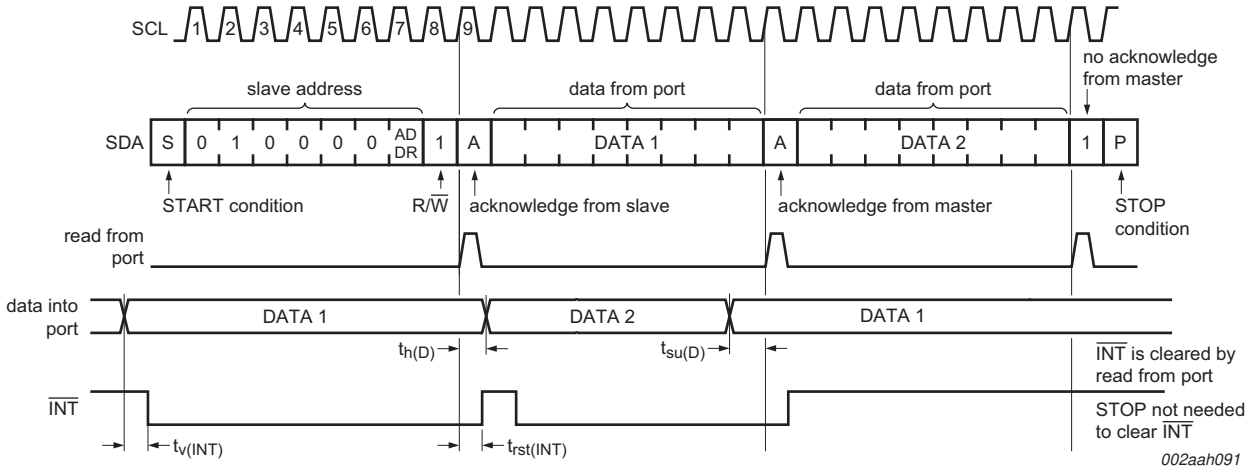
Fig 13. Read from register



Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 13).

Fig 14. Read Input port register (non-latched)

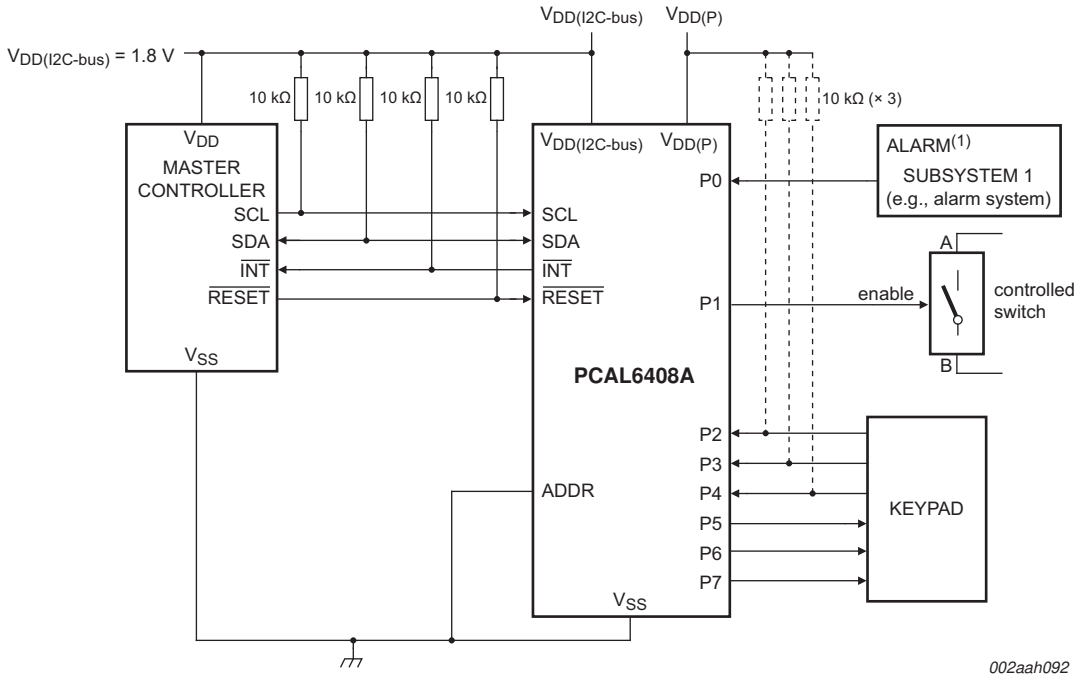


Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 13).

Fig 15. Read Input port register (latch enabled)

9. Application design-in information



Device address configured as 0100 000x for this example.

P0 and P2 through P4 are configured as inputs.

P1 and P5 through P7 are configured as outputs.

(1) Resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P port) do not need pull-up resistors.

Fig 16. Typical application

9.1 Minimizing I_{DD} when I/Os control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{DD} through a resistor as shown in Figure 16. The LED acts as a diode, so when the LED is off, the I/O V_I is about 1.2 V less than V_{DD}. The ΔI_{DD} parameter in Table 23 “Static characteristics” shows how I_{DD} increases as V_I becomes lower than V_{DD}. Designs that must minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off.

Figure 17 shows a high-value resistor in parallel with the LED. Figure 18 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevent additional supply current consumption when the LED is off.

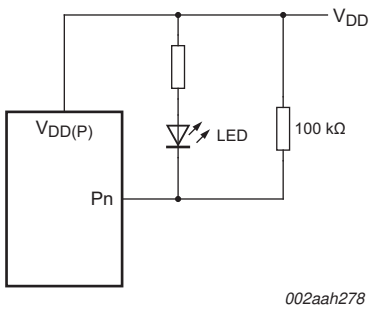


Fig 17. High-value resistor in parallel with the LED

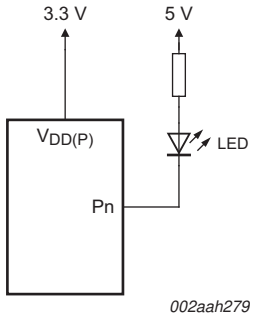


Fig 18. Device supplied by a lower voltage

9.2 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 19 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 10b, then only two of the fingers are active, reducing the current drive capability by 50 %.

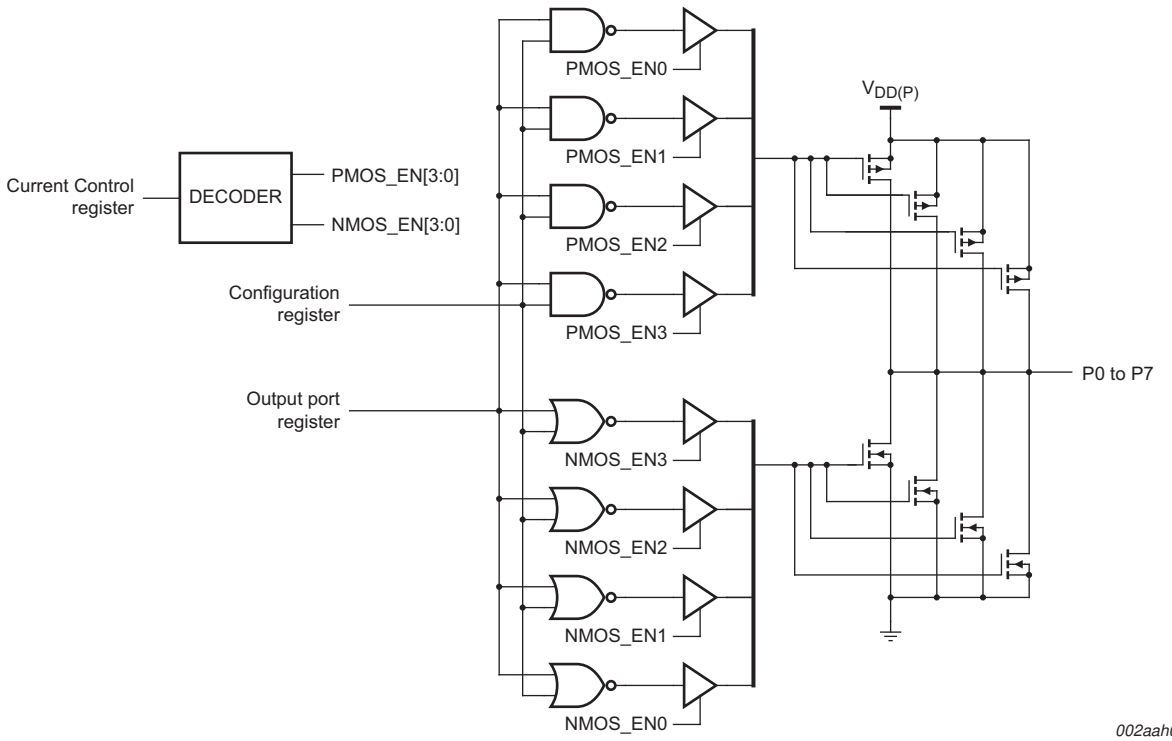


Fig 19. Simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and creates noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time creates ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

9.3 Power-on reset requirements

In the event of a glitch or data corruption, PCAL6408A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 20 and Figure 21.

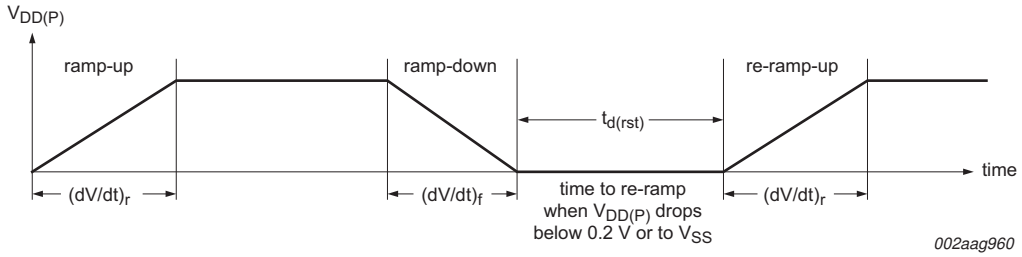


Fig 20. V_{DD} is lowered below 0.2 V or 0 V and then ramped up to V_{DD}

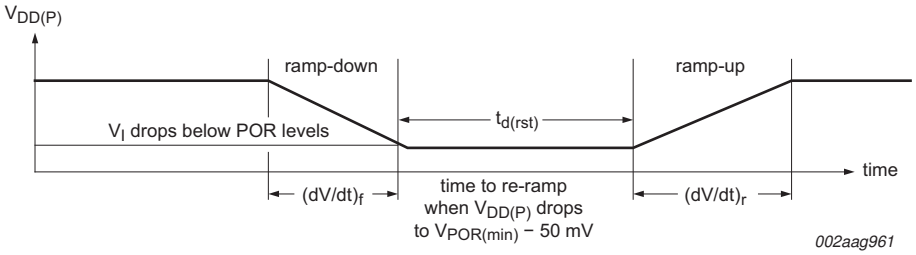


Fig 21. V_{DD} is lowered below the POR threshold, then ramped back up to V_{DD}

Table 19 specifies the performance of the power-on reset feature for PCAL6408A for both types of power-on reset.

Table 19. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 20		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 20		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 20; re-ramp time when $V_{DD(P)}$ drops below 0.2 V or to V_{SS}		1	-	-	µs
		Figure 21; re-ramp time when $V_{DD(P)}$ drops to $V_{POR(min)}$ − 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 22	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 22	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling $V_{DD(P)}$		0.7	-	-	V
		rising $V_{DD(P)}$		-	-	1.4	V

[1] Level that $V_{DD(P)}$ can glitch down to with a ramp rate of 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD(P)}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 22 and Table 19 provide more information on how to measure these specifications.

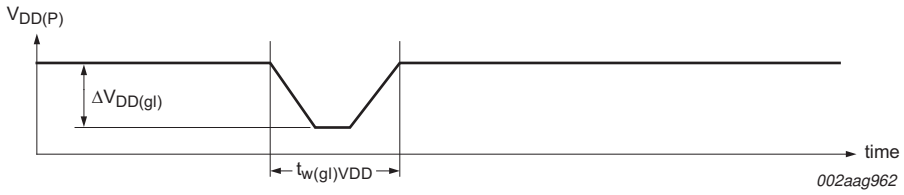


Fig 22. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 23 and Table 19 provide more details on this specification.

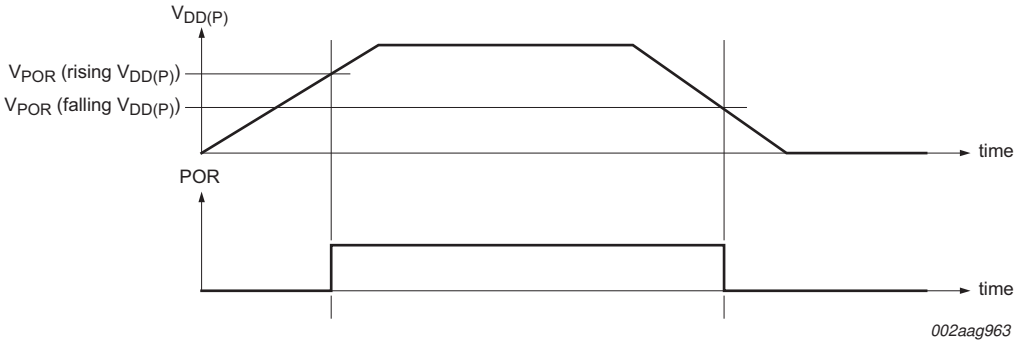


Fig 23. Power-on reset voltage (V_{POR})

9.4 Device current consumption with internal pull-up and pull-down resistors

The PCAL6408A integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails. Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in register 44h, while the resistor is connected by the enable register 43h. The configuration of the resistors is shown in Figure 10.

If the resistor is configured as a pull-up, that is, connected to V_{DD}, a current flows from the $V_{DD(P)}$ pin through the resistor to ground when the pin is held LOW. This current appears as additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, current flows from the power supply through the pin to the V_{SS} pin. While this current is not measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See Figure 27 for a graph of supply current versus the number of pull-up resistors.

10. Limiting values

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(I2C\text{-}bus)}$	I²C-bus supply voltage			−0.5	+6.5	V
$V_{DD(P)}$	supply voltage port P			−0.5	+6.5	V
V_I	input voltage		[1]	−0.5	+6.5	V
V_O	output voltage		[1]	−0.5	+6.5	V
I_{IK}	input clamping current	ADDR, $\overline{RESET}$, SCL; $V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD(P)}$		-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD(I2C\text{-}bus)}$		-	±20	mA
I_{OL}	LOW-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$		-	50	mA
		continuous; SDA, $\overline{INT}$; $V_O = 0$ V to $V_{DD(I2C\text{-}bus)}$		-	25	mA
I_{OH}	HIGH-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$		-	25	mA
I_{DD}	supply current	continuous through V_{SS}		-	200	mA
$I_{DD(P)}$	supply current port P	continuous through $V_{DD(P)}$		-	160	mA
$I_{DD(I2C\text{-}bus)}$	I²C-bus supply current	continuous through $V_{DD(I2C\text{-}bus)}$		-	10	mA
T_{stg}	storage temperature			−65	+150	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

11. Recommended operating conditions

Table 21. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(I2C\text{-}bus)}$	I²C-bus supply voltage			1.65	5.5	V
$V_{DD(P)}$	supply voltage port P			1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$		$0.7 \times V_{DD(I2C\text{-}bus)}$	5.5	V
		ADDR, P7 to P0		$0.7 \times V_{DD(P)}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$		−0.5	$0.3 \times V_{DD(I2C\text{-}bus)}$	V
		ADDR, P7 to P0		−0.5	$0.3 \times V_{DD(P)}$	V
I_{OH}	HIGH-level output current	P7 to P0		-	10	mA
I_{OL}	LOW-level output current	P7 to P0		-	25	mA
T_{amb}	ambient temperature	operating in free air		−40	+85	°C

12. Thermal characteristics

Table 22. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	TSSOP16 package	[1]	108	K/W
		HVQFN16 package	[1]	53	K/W
		XQFN16 package	[1]	184	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

13. Static characteristics

Table 23. Static characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(I2C-bus)}$ = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA; $V_{DD(P)}$ = 1.65 V to 5.5 V		−1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD(P)}$ or V_{SS}; I_O = 0 mA; $V_{DD(P)}$ = 1.65 V to 5.5 V	[2]	-	1	1.4	V
V_{OH}	HIGH-level output voltage[3]	P port; I_{OH} = −8 mA; CCX = 11b					
		$V_{DD(P)}$ = 1.65 V		1.2	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.8	-	-	V
		$V_{DD(P)}$ = 3 V		2.6	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.1	-	-	V
		P port; I_{OH} = −2.5 mA and CCX = 00b; I_{OH} = −5 mA and CCX = 01b; I_{OH} = −7.5 mA and CCX = 10b; I_{OH} = −10 mA and CCX = 11b;					
		$V_{DD(P)}$ = 1.65 V		1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.7	-	-	V
		$V_{DD(P)}$ = 3 V		2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.0	-	-	V
V_{OL}	LOW-level output voltage[3]	P port; I_{OL} = 8 mA; CCX = 11b					
		$V_{DD(P)}$ = 1.65 V		-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.25	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.2	V
		P port; I_{OL} = 2.5 mA and CCX = 00b; I_{OL} = 5 mA and CCX = 01b; I_{OL} = 7.5 mA and CCX = 10b; I_{OL} = 10 mA and CCX = 11b;					
		$V_{DD(P)}$ = 1.65 V		-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.3	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.2	V