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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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PCAL6416A

Low-voltage translating 16-bit I²C-bus/SMBus I/O expander with interrupt output, reset, and configuration registers

Rev. 6.2 — 7 April 2017 Product data sheet

1. General description

The PCAL6416A is a 16-bit general-purpose I/O expander that provides remote I/O expansion for most microcontroller families via the I²C-bus interface.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level to I/O devices operating at a different (usually higher) voltage level. The PCAL6416A has built-in level shifting feature that makes these devices extremely flexible in mixed signal environments where communication between incompatible I/O voltages is required. Its wide V_{DD} range of 1.65 V to 5.5 V on the dual power rail allows seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL6416A: $V_{DD(I2C\text{-}bus)}$ and $V_{DD(P)}$. $V_{DD(I2C\text{-}bus)}$ provides the supply voltage for the interface at the master side (for example, a microcontroller) and the $V_{DD(P)}$ provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCAL6416A is provided through $V_{DD(I2C\text{-}bus)}$. $V_{DD(I2C\text{-}bus)}$ should be connected to the V_{DD} of the external SCL/SDA lines. This indicates the V_{DD} level of the I²C-bus to the PCAL6416A, while the voltage level on Port P of the PCAL6416A is determined by the $V_{DD(P)}$.

The PCAL6416A contains the PCA6416A register set of four pairs of 8-bit Configuration, Input, Output, and Polarity Inversion registers and additionally, the PCAL6416A has Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs. The PCAL6416A is a pin-to-pin replacement to the PCA6416A, however, the PCAL6416A powers up with all I/O interrupts masked. This mask default allows for a board bring-up free of spurious interrupts at power-up.

At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.

The system master can reset the PCAL6416A in the event of a time-out or other improper operation by asserting a LOW in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I²C-bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part.

The PCAL6416A open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCAL6416A can remain a simple slave device. The input latch feature holds or latches the input pin state and keeps the logic values that created the interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I²C-bus address and allow up to two devices to share the same I²C-bus or SMBus.

2. Features and benefits

- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- Low standby current consumption:
  - 1.5 μA typical at 5 V V_{DD}
  - 1.0 μA typical at 3.3 V V_{DD}
- Schmitt trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.25 V (typical) at 2.5 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
  - V_{hys} = 0.5 V (typical) at 5 V
- 5 V tolerant I/O ports
- Active LOW reset input ($\overline{\text{RESET}}$)
- Open-drain active LOW interrupt output ($\overline{\text{INT}}$)
- 400 kHz Fast-mode I²C-bus
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Noise filter on SCL/SDA inputs

- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP24, HWQFN24, UFBGA24, VFBGA24, XFBGA24, X2QFN24 (LGA, Land Grid Array)

2.1 Agile I/O features

- Software backward compatible with PCA6416A with interrupts disabled at power-up
- Pin-to-pin drop-in replacement with PCA6416A
- Output port configuration: bank selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/pull-down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

3. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCAL6416AEV	L16A	VFBGA24	plastic very thin fine-pitch ball grid array package; 24 balls; body 3 × 3 × 0.85 mm	SOT1199-1
PCAL6416AEX	L6X[1]	XFBGA24[2]	plastic, extremely thin fine-pitch ball grid array package; 24 balls; body 2 × 2 × 0.5 mm	SOT1342-1
PCAL6416AEX1	16X[1]	X2QFN24	plastic, thermal enhanced super thin land grid array or quad flat package; no leads; 24 terminals; body 2.0 × 2.0 × 0.35 mm	SOT1895-1
PCAL6416AER	S6X[1]	UFBGA24[2]	plastic, ultra thin fine-pitch ball grid array package; 24 balls; body 2 × 2 × 0.65 mm	SOT1361-1
PCAL6416AHF	L16A	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm	SOT994-1
PCAL6416APW	PCAL6416A	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

[1] 'X' rotates from 1 to 5 and indicates the work week of the indicated month

[2] XFBGA24/UFBGA24 packages are discontinued with lifetime buy March 2017; new designs must use X2QFN24 package

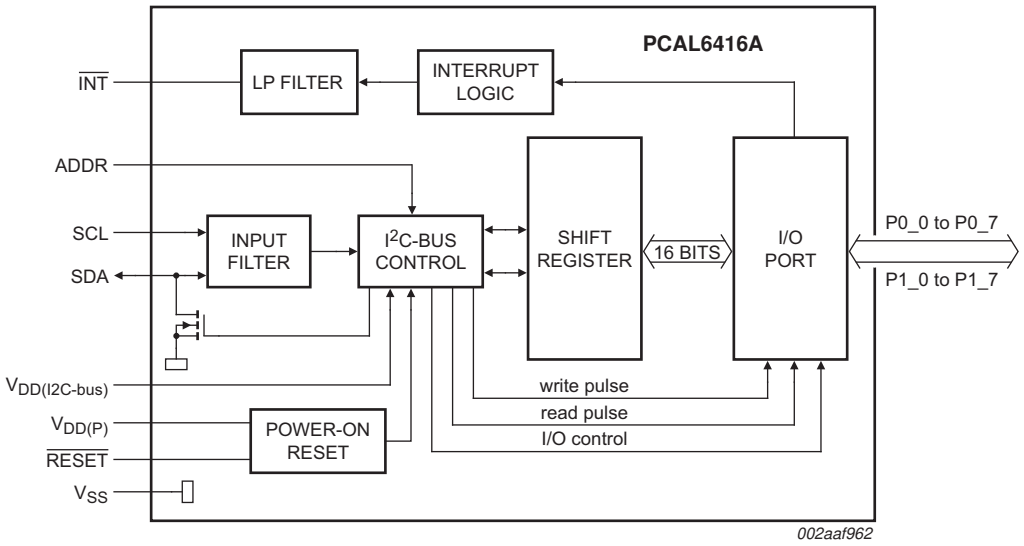
3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCAL6416AEV	PCAL6416AEVJ	VFBGA24	Reel 13” Q1/T1 *Standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCAL6416AEX	PCAL6416AEXX	XFBGA24[1]	Reel 7” Q1/T1 *Standard mark SMD	5000	T_{amb} = −40 °C to +85 °C
PCAL6416AEX1	PCAL6416AEX1Z	X2QFN24	Reel 7” Q2/T3 *Standard mark SMD	5000	T_{amb} = −40 °C to +85 °C
PCAL6416AER	PCAL6416AERJ	UFBGA24[1]	Reel 13” Q1/T1 *Standard mark SMD	10000	T_{amb} = −40 °C to +85 °C
	PCAL6416AERX	UFBGA24[1]	Reel 7” Q1/T1 *Standard mark SMD	3000	T_{amb} = −40 °C to +85 °C
PCAL6416AHF	PCAL6416AHF,128	HWQFN24	Reel 13” Q2/T3 *Standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCAL6416APW	PCAL6416APW,118	TSSOP24	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

[1] XFBGA24/UFBGA24 packages are discontinued with lifetime buy March 2017; new designs must use X2QFN24 package

4. Block diagram



All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCAL6416A (positive logic)

5. Pinning information

5.1 Pinning

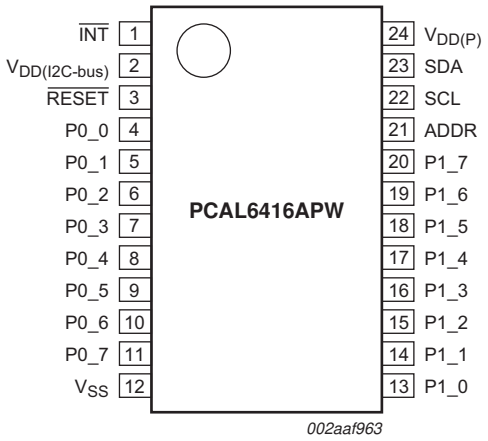
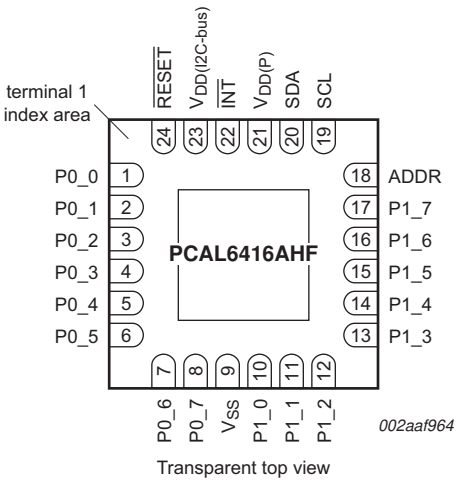


Fig 2. Pin configuration for TSSOP24



The exposed center pad, if used, must be connected only as a secondary ground or must be left electrically open.

Fig 3. Pin configuration for HWQFN24

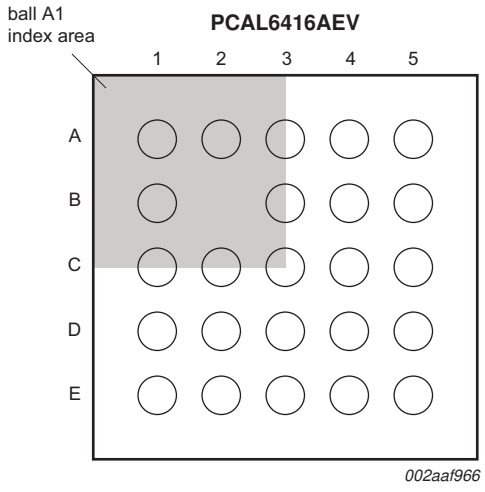


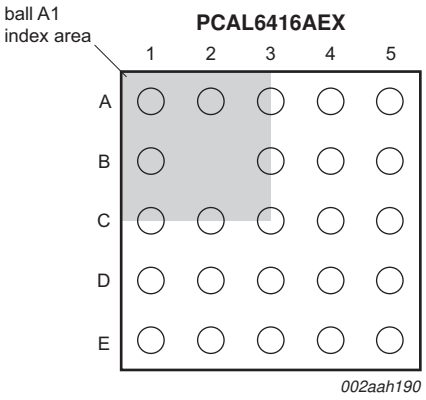
Fig 4. Pin configuration for VFBGA24 (3 mm × 3 mm)

	1	2	3	4	5
A	P0_0	RESET	INT	SDA	SCL
B	P0_2		VDD(I2C-bus)	VDD(P)	ADDR
C	P0_3	P0_4	P0_1	P1_7	P1_6
D	P0_5	P0_7	P1_2	P1_4	P1_5
E	P0_6	VSS	P1_0	P1_1	P1_3

002aag244

An empty cell indicates no ball is populated at that grid point.

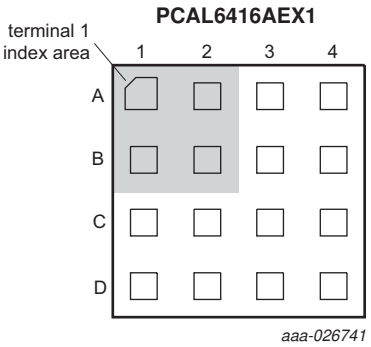
Fig 5. Ball mapping for 3 mm × 3 mm VFBGA24 (transparent top view)



Transparent top view

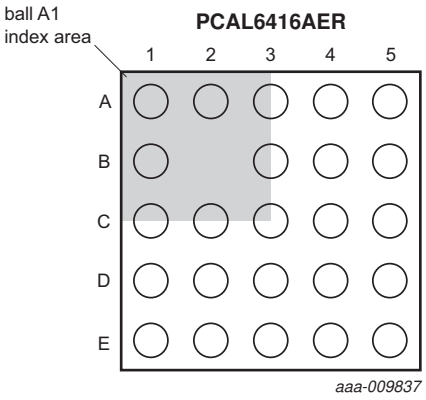
XFBGA24 with 0.175 mm ball size.

Fig 6. Pin configuration for XFBGA24 (2 mm × 2 mm); EX option



Transparent top view

Fig 7. Pin configuration for X2QFN24 (2 mm × 2 mm); EX1 land grid array option



Transparent top view

UFBGA24 with 0.24 mm ball size.

Fig 8. Pin configuration for UFBGA24 (2 mm × 2 mm); ER option

	1	2	3	4	5
A	$\overline{\text{RESET}}$	$V_{DD(I2C\text{-}bus)}$	$V_{DD(P)}$	SCL	ADDR
B	P0_0		$\overline{\text{INT}}$	SDA	P1_7
C	P0_2	P0_3	P0_1	P1_6	P1_5
D	P0_4	P0_7	P1_0	P1_4	P1_3
E	P0_5	P0_6	V_{SS}	P1_1	P1_2

002aah145

An empty cell indicates no ball is populated at that grid point.

Fig 9. Ball mapping for 2 mm × 2 mm XFBGA24, X2QFN24 and UFBGA24 (transparent top view)

5.2 Pin description

Table 3. Pin description

Symbol	Pin				Description
	TSSOP24	HWQFN24	VFBGA24	UFBGA24, XFBGA24, X2QFN24	
$\overline{INT}$	1	22	A3	B3	Interrupt output. Connect to $V_{DD(I2C\text{-}bus)}$ or $V_{DD(P)}$ through a pull-up resistor.
$V_{DD(I2C\text{-}bus)}$	2	23	B3	A2	Supply voltage of I²C-bus. Connect directly to the V_{DD} of the external I²C master. Provides voltage-level translation.
$\overline{RESET}$	3	24	A2	A1	Active LOW reset input. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor if no active connection is used.
P0_0[1]	4	1	A1	B1	Port 0 input/output 0.
P0_1[1]	5	2	C3	C3	Port 0 input/output 1.
P0_2[1]	6	3	B1	C1	Port 0 input/output 2.
P0_3[1]	7	4	C1	C2	Port 0 input/output 3.
P0_4[1]	8	5	C2	D1	Port 0 input/output 4.
P0_5[1]	9	6	D1	E1	Port 0 input/output 5.
P0_6[1]	10	7	E1	E2	Port 0 input/output 6.
P0_7[1]	11	8	D2	D2	Port 0 input/output 7.
V_{SS}	12	9	E2	E3	Ground.
P1_0[2]	13	10	E3	D3	Port 1 input/output 0.
P1_1[2]	14	11	E4	E4	Port 1 input/output 1.
P1_2[2]	15	12	D3	E5	Port 1 input/output 2.
P1_3[2]	16	13	E5	D5	Port 1 input/output 3.
P1_4[2]	17	14	D4	D4	Port 1 input/output 4.
P1_5[2]	18	15	D5	C5	Port 1 input/output 5.
P1_6[2]	19	16	C5	C4	Port 1 input/output 6.
P1_7[2]	20	17	C4	B5	Port 1 input/output 7.
ADDR	21	18	B5	A5	Address input. Connect directly to $V_{DD(P)}$ or ground.
SCL	22	19	A5	A4	Serial clock bus. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
SDA	23	20	A4	B4	Serial data bus. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
$V_{DD(P)}$	24	21	B4	A3	Supply voltage of PCAL6416A for Port P.

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-on, all I/O are configured as input.

[2] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-on, all I/O are configured as input.

6. Voltage translation

Table 4 shows how to set up V_{DD} levels for the necessary voltage translation between the I²C-bus and the PCAL6416A.

Table 4. Voltage translation

$V_{DD(I2C-bus)}$ (SDA and SCL of I²C master)	$V_{DD(P)}$ (Port P)
1.8 V	1.8 V
1.8 V	2.5 V
1.8 V	3.3 V
1.8 V	5 V
2.5 V	1.8 V
2.5 V	2.5 V
2.5 V	3.3 V
2.5 V	5 V
3.3 V	1.8 V
3.3 V	2.5 V
3.3 V	3.3 V
3.3 V	5 V
5 V	1.8 V
5 V	2.5 V
5 V	3.3 V
5 V	5 V

7. Functional description

Refer to Figure 1 “Block diagram of PCAL6416A (positive logic)”.

7.1 Device address

The address of the PCAL6416A is shown in Figure 10.

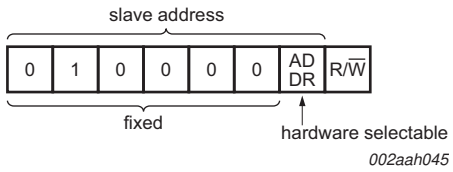


Fig 10. PCAL6416A address

ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

7.2 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C-bus slave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

7.3 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCAL6416A. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. Bit 6 in conjunction with the lower three bits of the Command byte are used to point to the extended features of the device (Agile IO). This register is write only.

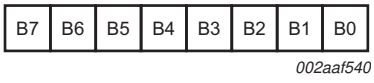


Fig 11. Pointer register bits

Table 6. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111
0	1	0	0	0	0	0	0	40h	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	0	1	41h	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	1	0	42h	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	0	1	1	43h	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	1	0	0	44h	Input latch register 0	read/write byte	0000 0000
0	1	0	0	0	1	0	1	45h	Input latch register 1	read/write byte	0000 0000
0	1	0	0	0	1	1	0	46h	Pull-up/pull-down enable register 0	read/write byte	0000 0000
0	1	0	0	0	1	1	1	47h	Pull-up/pull-down enable register 1	read/write byte	0000 0000
0	1	0	0	1	0	0	0	48h	Pull-up/pull-down selection register 0	read/write byte	1111 1111
0	1	0	0	1	0	0	1	49h	Pull-up/pull-down selection register 1	read/write byte	1111 1111
0	1	0	0	1	0	1	0	4Ah	Interrupt mask register 0	read/write byte	1111 1111
0	1	0	0	1	0	1	1	4Bh	Interrupt mask register 1	read/write byte	1111 1111
0	1	0	0	1	1	0	0	4Ch	Interrupt status register 0	read byte	0000 0000
0	1	0	0	1	1	0	1	4Dh	Interrupt status register 1	read byte	0000 0000
0	1	0	0	1	1	1	1	4Fh	Output port configuration register	read/write byte	0000 0000

[1] Undefined.

7.4 Register descriptions

7.4.1 Input port register pair (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 8.2.

Table 7. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 8. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

7.4.2 Output port register pair (02h, 03h)

The Output port registers (registers 2 and 3) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 9. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 10. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

7.4.3 Polarity inversion register pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 11. Polarity inversion port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 12. Polarity inversion port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

7.4.4 Configuration register pair (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 13. Configuration port 0 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 14. Configuration port 1 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

7.4.5 Output drive strength register pairs (40h, 41h, 42h, 43h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 41 CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41 CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See Section 9.2 “Output drive strength control” for more details. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 15. Current control port 0 register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 16. Current control port 0 register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 17. Current control port 1 register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 18. Current control port 1 register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

7.4.6 Input latch register pair (44h, 45h)

The input latch registers (registers 44 and 45) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 18.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is

cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port register bit 4 register should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 19. Input latch port 0 register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 20. Input latch port 1 register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

7.4.7 Pull-up/pull-down enable register pair (46h, 47h)

These registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 7.4.11). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 21. Pull-up/pull-down enable port 0 register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 22. Pull-up/pull-down enable port 1 register (address 47h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

7.4.8 Pull-up/pull-down selection register pair (48h, 49h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 23. Pull-up/pull-down selection port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 24. Pull-up/pull-down selection port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

7.4.9 Interrupt mask register pair (4Ah, 4Bh)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 25. Interrupt mask port 0 register (address 4Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 26. Interrupt mask port 1 register (address 4Bh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

7.4.10 Interrupt status register pair (4Ch, 4Dh)

These read-only registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register pair write operation is described in Section 8.1. A register pair read operation is described in Section 8.2.

Table 27. Interrupt status port 0 register (address 4Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 28. Interrupt status port 1 register (address 4Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

7.4.11 Output port configuration register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 12). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (4Fh) before the configuration register (06h and 07h) sets the port pins as outputs.

ODEN0 configures Port 0_x and ODEN1 configures Port 1_x.

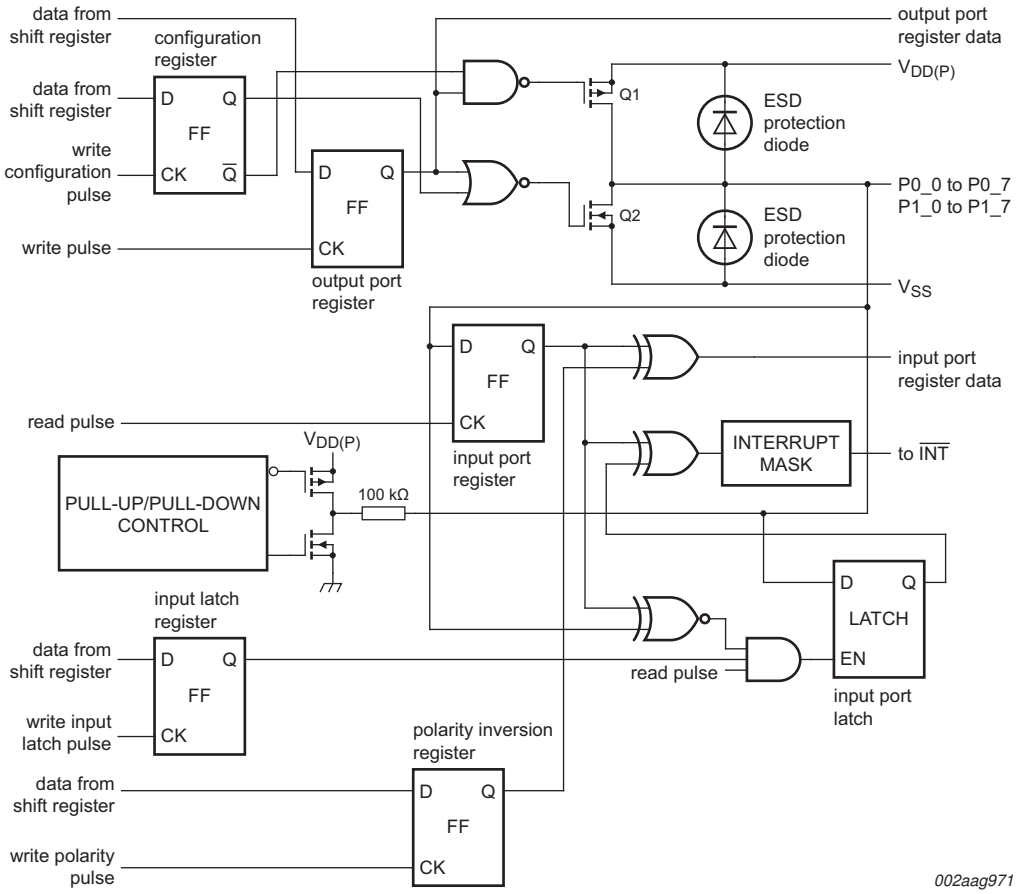
Table 29. Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

7.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above $V_{DD(P)}$ to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig 12. Simplified schematic of the I/Os (P0_0 to P0_7, P1_0 to P1_7)

7.6 Power-on reset

When power (from 0 V) is applied to $V_{DD(P)}$, an internal power-on reset holds the PCAL6416A in a reset condition until $V_{DD(P)}$ has reached V_{POR}. At that time, the reset condition is released and the PCAL6416A registers and I²C-bus/SMBus state machine initializes to their default states. After that, $V_{DD(P)}$ must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. See Section 9.3 “Power-on reset requirements”.

7.7 Reset input ($\overline{RESET}$)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin LOW for a minimum of $t_{w(rst)}$. The PCAL6416A registers and I²C-bus/SMBus state machine are changed to their default state once $\overline{RESET}$ is LOW (0). When $\overline{RESET}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to $V_{DD(I2C-bus)}$ if no active connection is used.

7.8 Interrupt output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{INT}$ is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt (see Figure 18). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to $V_{DD(P)}$ or $V_{DD(I2C\text{-}bus)}$, depending on the application. $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information.

When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

8. Bus transactions

The PCAL6416A is an I²C-bus slave device. Data is exchanged between the master and PCAL6416A through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Write commands

Data is transmitted to the PCAL6416A by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 10 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

Twenty-two registers within the PCAL6416A are configured to operate as eleven register pairs. The eleven pairs are input port, output port, polarity inversion, configuration, output drive strength (two 16-bit registers), input latch, pull-up/pull-down enable, pull-up/pull-down selection, interrupt mask, and interrupt status registers. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 13 and Figure 14). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers.

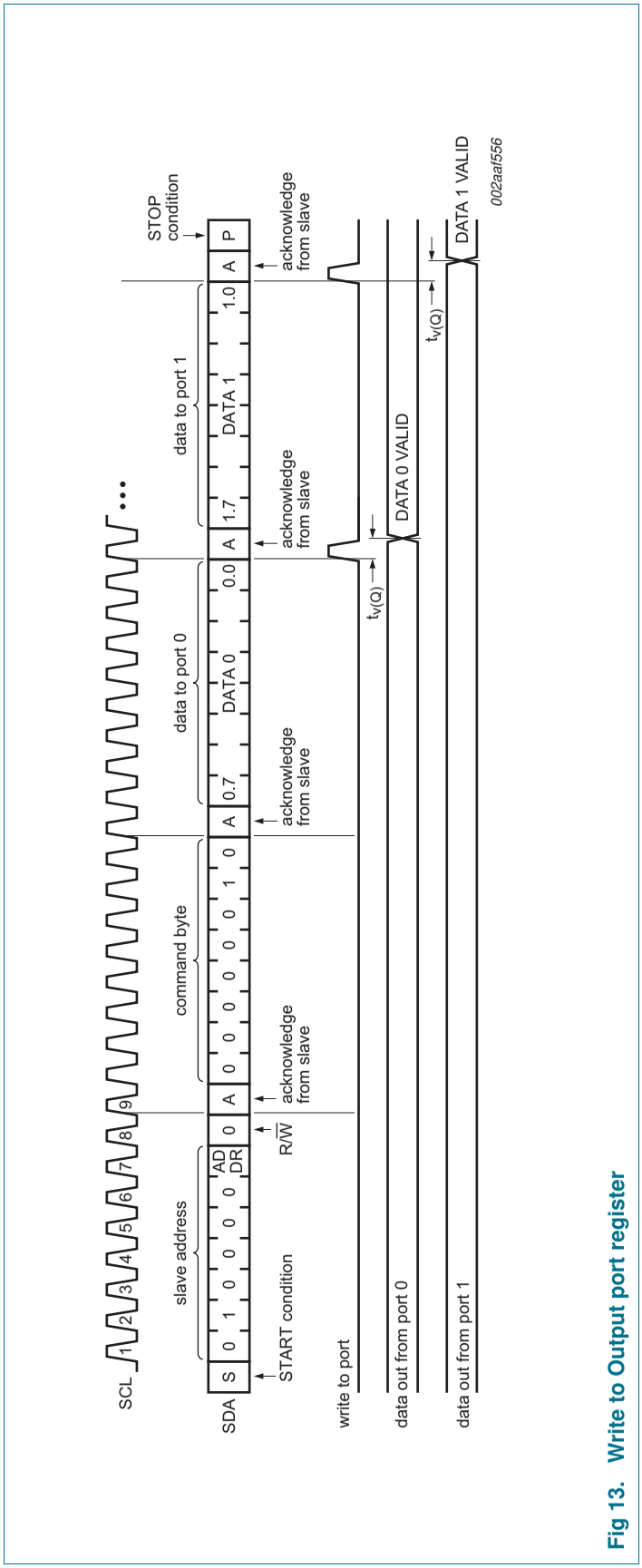


Fig 13. Write to Output port register

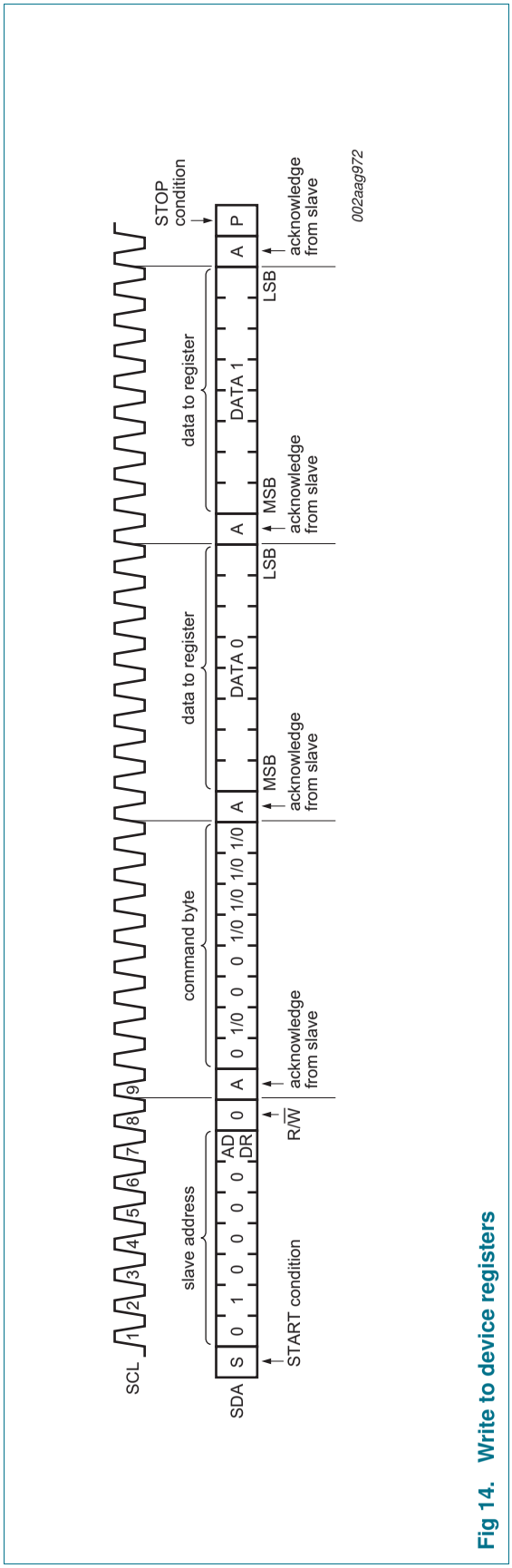


Fig 14. Write to device registers

8.2 Read commands

To read data from the PCAL6416A, the bus master must first send the PCAL6416A address with the least significant bit set to a logic 0 (see Figure 10 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the PCAL6416A (see Figure 15 and Figure 18). Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.

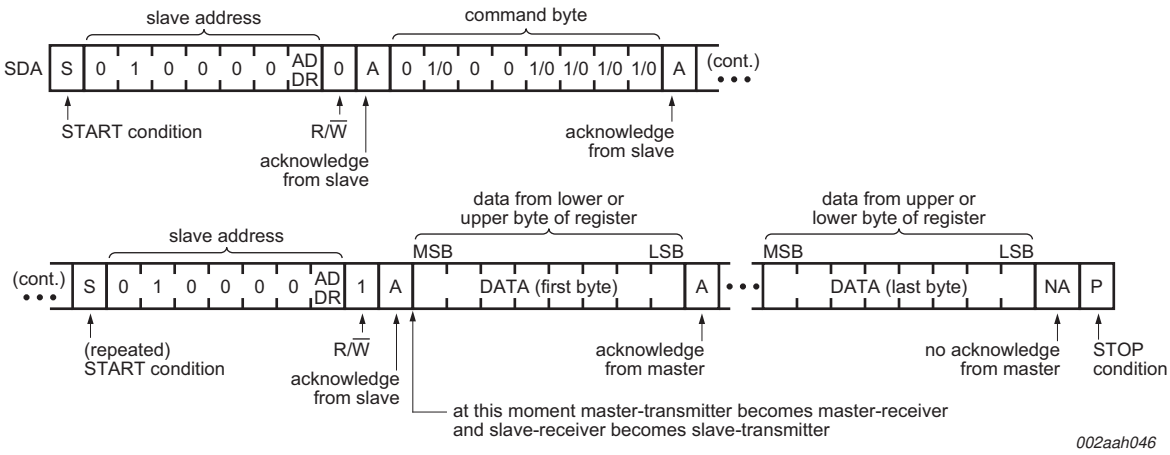
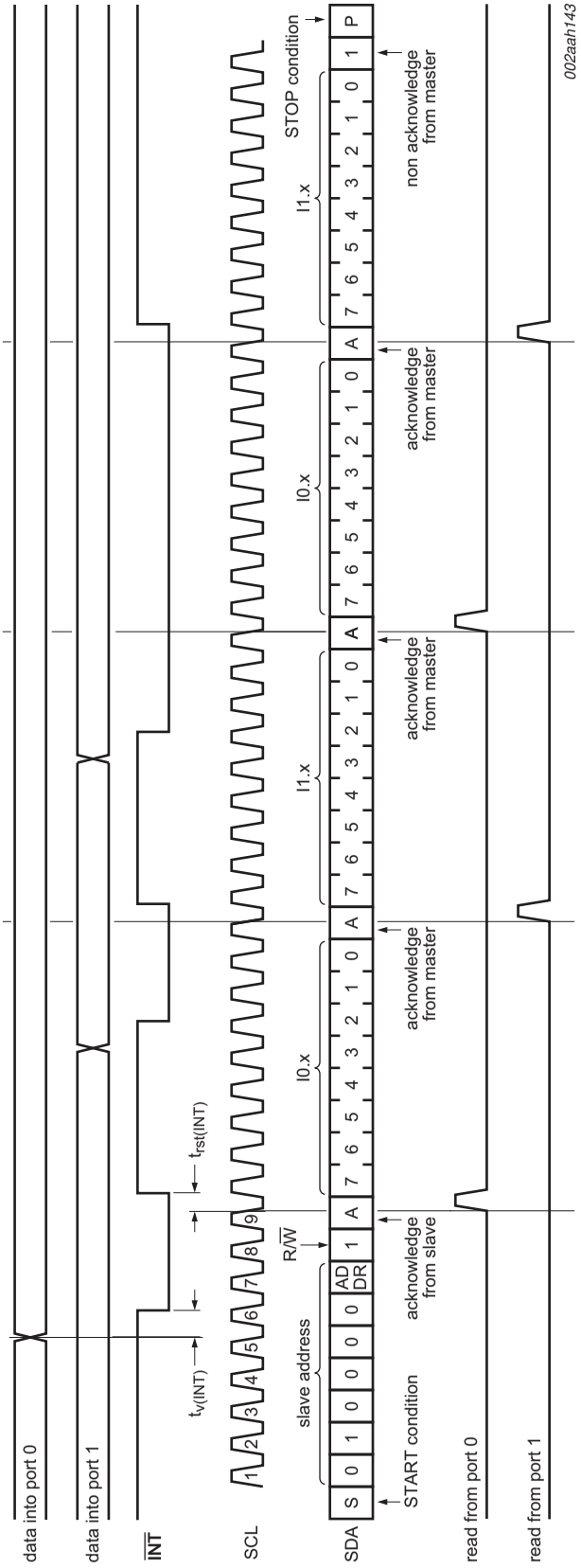


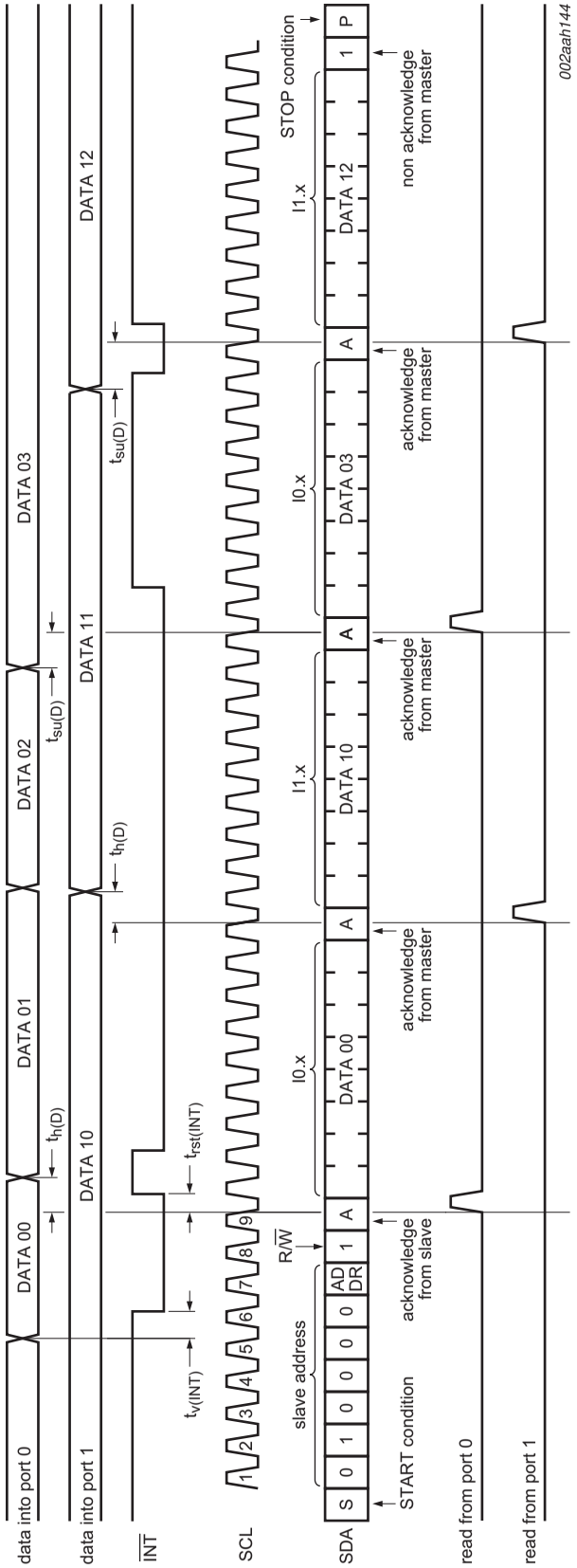
Fig 15. Read from device registers



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see Figure 15).

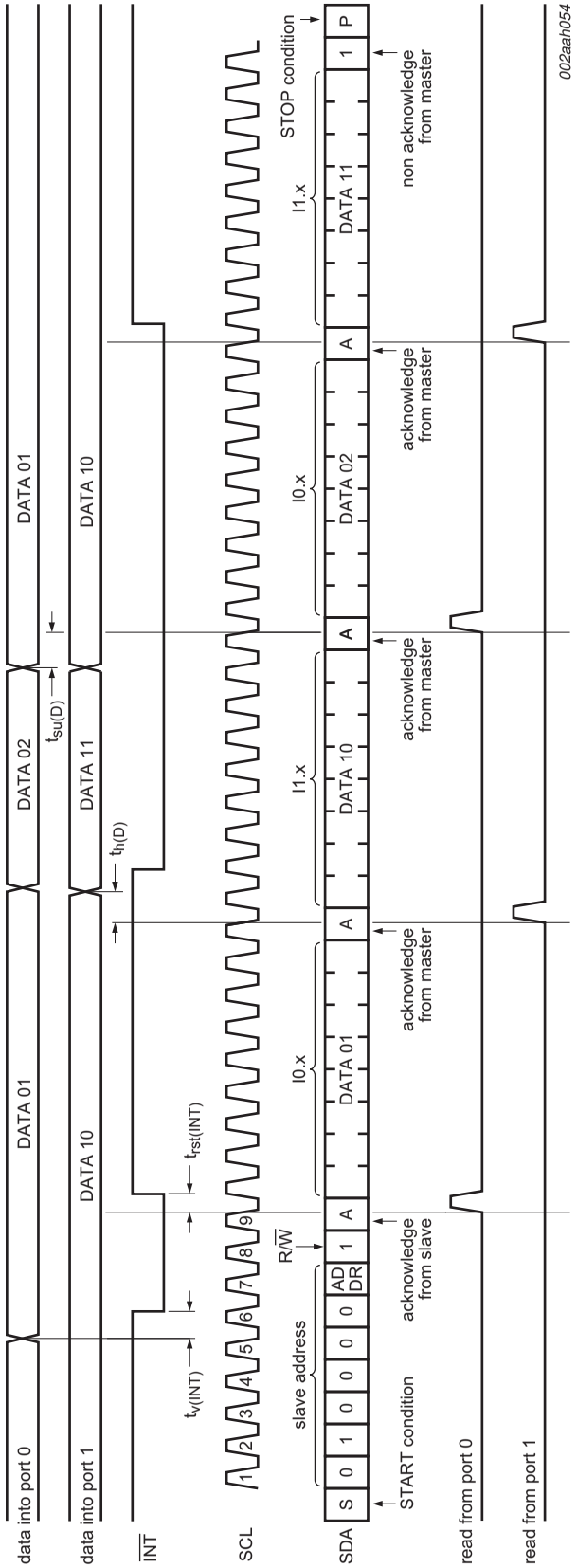
Fig 16. Read input port register (non-latched), scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see Figure 15).

Fig 17. Read input port register (non-latched), scenario 2

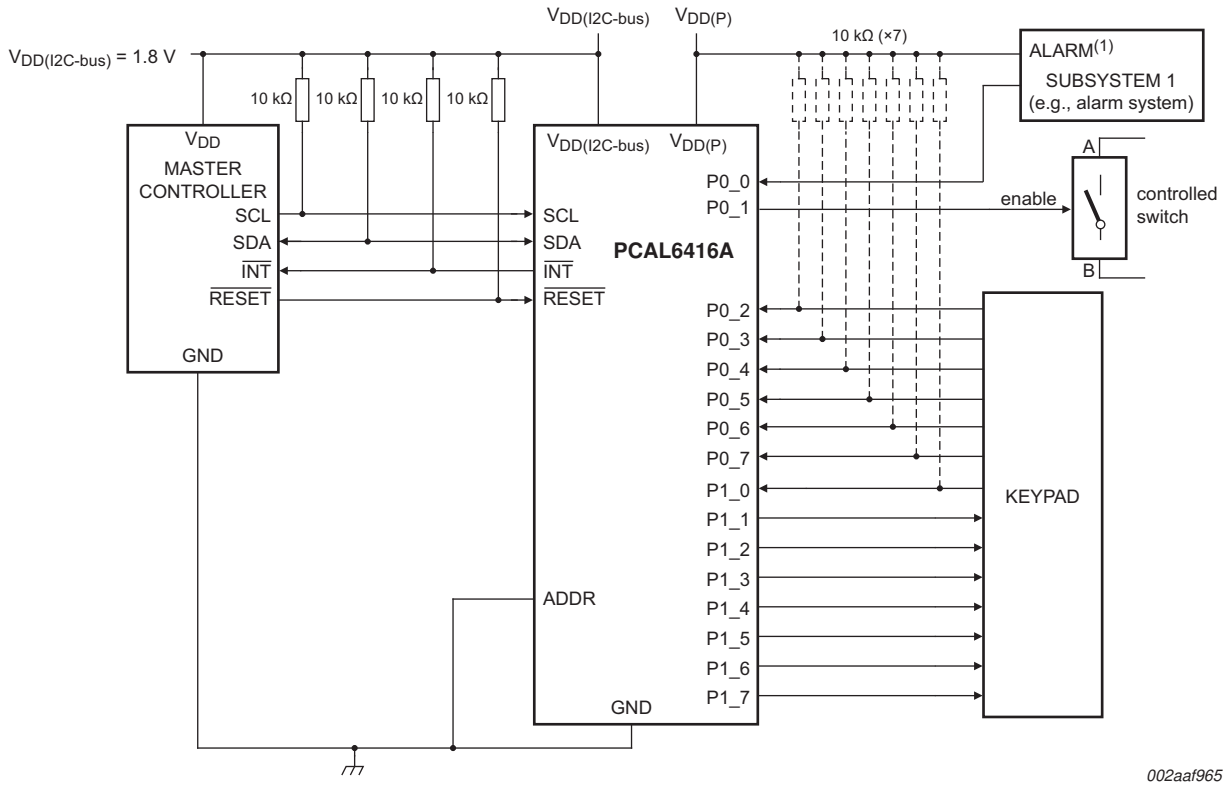


Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see Figure 15).

Fig 18. Read input port register (latch enabled), scenario 3

9. Application design-in information



Device address configured as 0100 000x for this example.

P0_0 and P0_2 through P1_0 are configured as inputs.

P0_1 and P1_1 through P1_7 are configured as outputs.

(1) External resistors are required for inputs (on P port) that may float. Also, internal pull-up or pull-down may be used to eliminate the need for external components. If a driver to an input will never let the input float, a resistor is not needed. If an output in the P port is configured as a push-pull output there is no need for external pull-up resistors. If an output in the P port is configured as an open-drain output, external pull-up resistors are required.

Fig 19. Typical application

9.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 19. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than $V_{DD(P)}$. The supply current, $I_{DD(P)}$, increases as V_I becomes lower than $V_{DD(P)}$.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 20 shows a high value resistor in parallel with the LED. Figure 21 shows $V_{DD(P)}$ less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above $V_{DD(P)}$ and prevents additional supply current consumption when the LED is off.

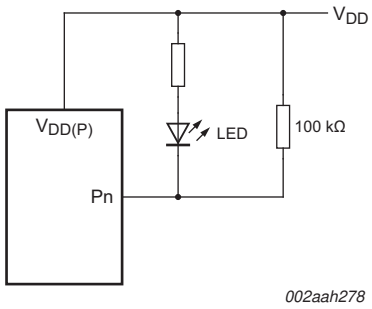


Fig 20. High value resistor in parallel with the LED

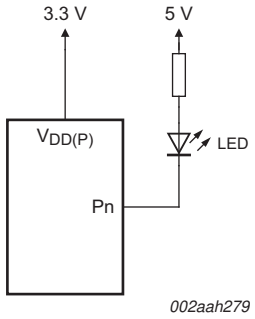


Fig 21. Device supplied by a lower voltage

9.2 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 22 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 10b, then only two of the fingers are active, reducing the current drive capability by 50 %.

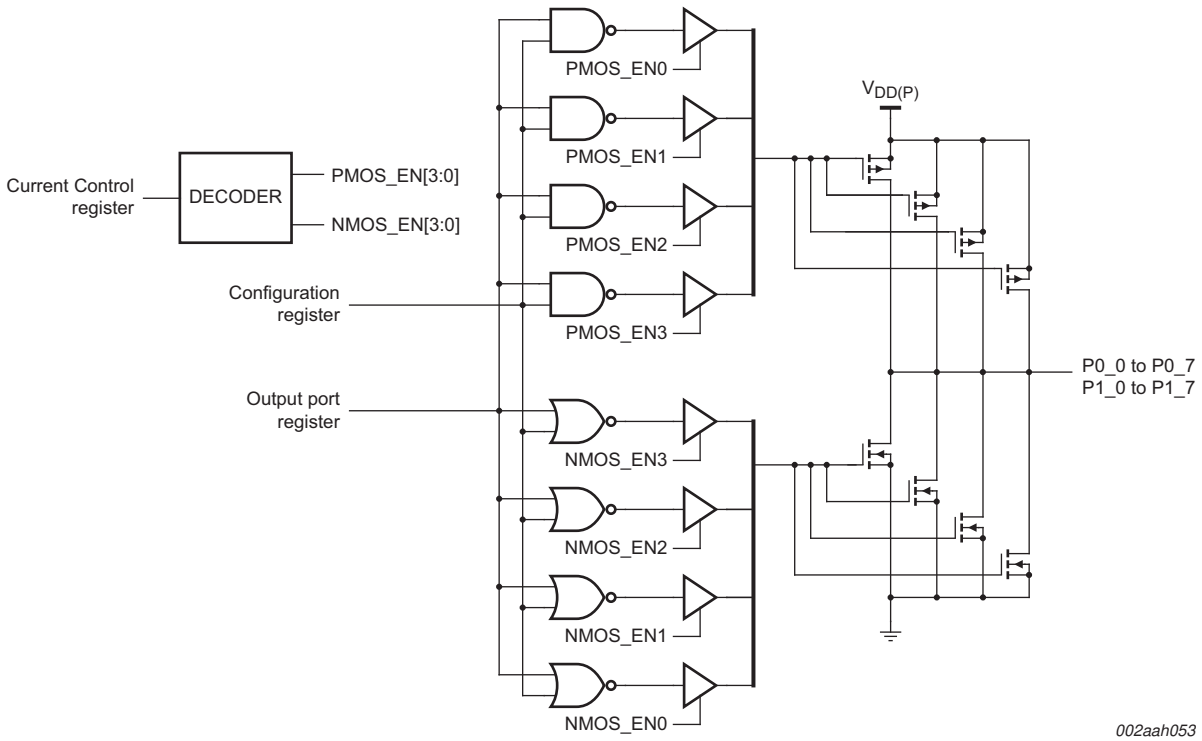


Fig 22. Simplified output stage