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PCAL6524

Ultra low-voltage translating 24-bit Fm+ I²C-bus/SMBus I/O expander with Agile I/O features, interrupt output and reset

Rev. 1 — 24 November 2016 Product data sheet

1. General description

The PCAL6524 is a 24-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Fast-mode Plus (Fm+) I²C-bus interface. The ultra low-voltage interface allows for direct connection to a microcontroller operating down to 0.8 V.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level down to 0.8 V to I/O devices operating at a different voltage level 1.65 V to 5.5 V. The PCAL6524 has built-in level shifting feature that makes these devices extremely flexible in mixed power supply systems where communication between incompatible I/O voltages is required, allowing seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL6524: $V_{DD(I2C\text{-}bus)}$ and $V_{DD(P)}$. $V_{DD(I2C\text{-}bus)}$ provides the supply voltage for the interface at the master side (for example, a microcontroller) and the $V_{DD(P)}$ provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCAL6524 is provided through $V_{DD(I2C\text{-}bus)}$. $V_{DD(I2C\text{-}bus)}$ should be connected to the V_{DD} of the external SCL/SDA lines. This indicates the V_{DD} level of the I²C-bus to the PCAL6524, while the voltage level on Port P of the PCAL6524 is determined by the $V_{DD(P)}$.

The PCAL6524 fully meets the Fm+ I²C-bus specification at speeds to 1 MHz and implements Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

Additional Agile I/O Plus features include I²C software reset and device ID. Interrupts can be specified by level or edge, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.

The power-on reset puts the registers in their default state and initializes the I²C-bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part. The system master can also accomplish a reset via an I²C command and initialize all registers to their default state.

The PCAL6524 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state. As well, the $\overline{\text{INT}}$ output can be specified to activate on input pin edges. There are a large number of interrupt mask functions available to maximize flexibility.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without communication via the I²C-bus. Thus, the PCAL6524 can remain a simple slave device. The input latch feature holds or latches the input pin state and keeps the logic values that created the interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I²C-bus address and allow up to four devices to share the same I²C-bus or SMBus.

2. Features and benefits

- I²C-bus to parallel port expander
- 1 MHz Fast-mode Plus I²C-bus
- Operating power supply voltage range of 0.8 V to 3.6 V on the I²C-bus side
- Allows bidirectional voltage-level translation and GPIO expansion between 0.8 V to 3.6 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V, 5.5 V Port P
- Low standby current consumption: 2.0 μA typical at 3.3 V $V_{DD(P)}$
- Schmitt trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.05 V (typical) at 0.8 V
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
- 5.5 V tolerant I/O ports and 3.6 V tolerant I²C-bus pins
- Active LOW reset input ($\overline{\text{RESET}}$)
- Open-drain active LOW interrupt output ($\overline{\text{INT}}$)
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP32, HUQFN32, VFBGA36

2.1 Agile I/O features

- Output port configuration: bank selectable or pin selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/pull-down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

2.2 Additional Agile I/O Plus features

- Interrupt edge specification on a bit-by-bit basis
- Interrupt individual clear without disturbing other events
- Read all interrupt events without clear
- Switch debounce hardware
- General call software reset
- I²C software Device ID function

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCAL6524HE	L6524	HUQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.56 mm	SOT1426-1
PCAL6524DR	PCAL6524	TSSOP32[1]	plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm	SOT487-1
PCAL6524EV	524	VFBGA36	plastic very fine-pitch ball grid array package, body 2.6 x 2.6 mm	SOT1851-1

[1] Under development. Please contact your local NXP sales office for availability.

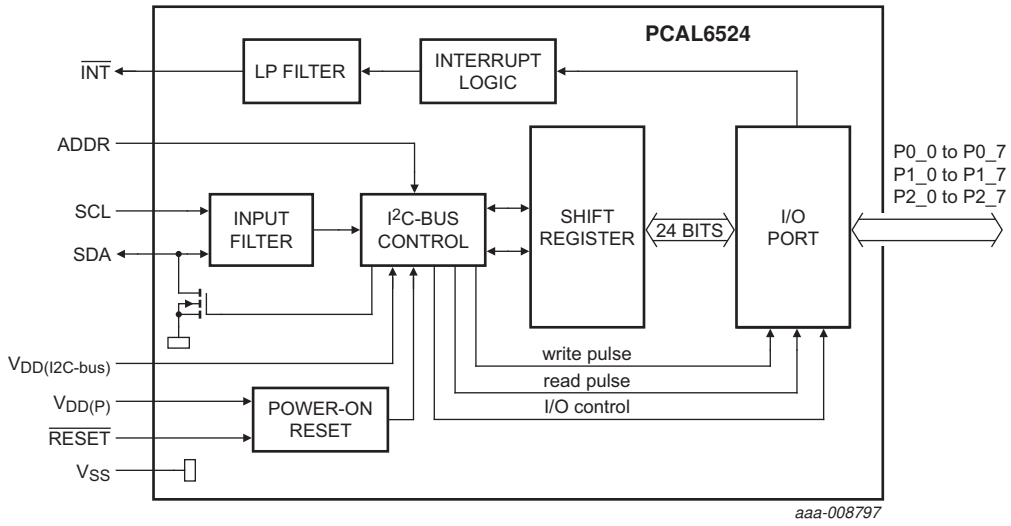
3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCAL6524HE	PCAL6524HEHP	HUQFN32	Reel 13” Q2/T3 *standard mark SMD	5000	T_{amb} = −40 °C to +85 °C
PCAL6524DR	PCAL6524DRJ	TSSOP32[1]	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCAL6524EV	PCAL6524EVJ	VFBGA36	Reel 13” Q1/T1 *standard mark SMD	5000	T_{amb} = −40 °C to +85 °C

[1] Under development. Please contact your local NXP sales office for availability.

4. Block diagram



All I/Os are set to inputs at reset.

Fig 1. Block diagram (positive logic)

5. Pinning information

5.1 Pinning

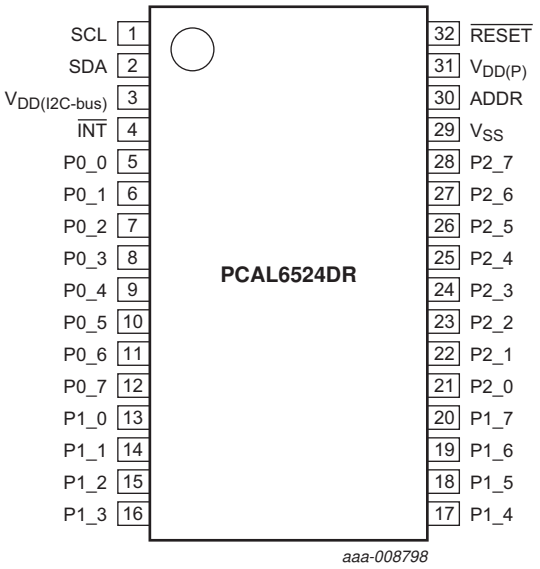


Fig 2. Pin configuration for TSSOP32

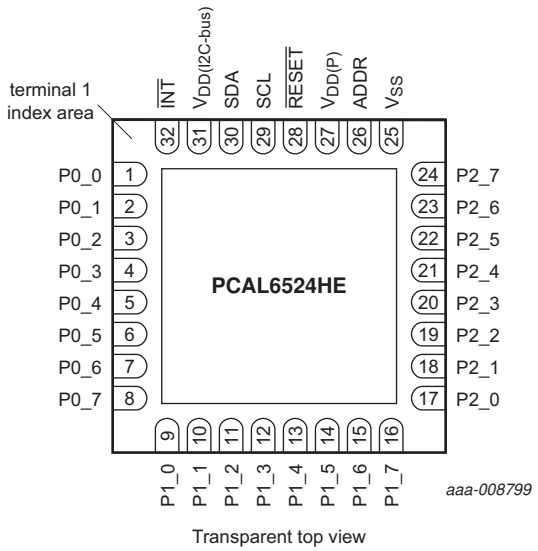


Fig 3. Pin configuration for HUQFN32

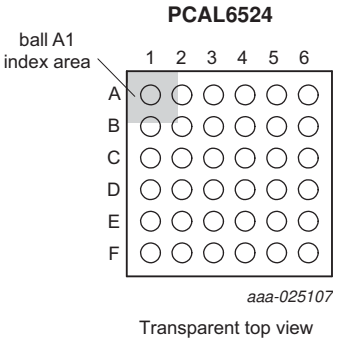


Fig 4. Pin configuration for VFBGA36

5.2 Pin description

Table 3. Pin description

Symbol	Pin				Description
	VFBGA36	TSSOP32	HUQFN32	Type	
SCL	A3	1	29	I	Serial clock line. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
SDA	A2	2	30	I/O	Serial data line. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
$V_{DD(I2C\text{-}bus)}$	A1	3	31	power supply	Supply voltage of I²C-bus. Connect directly to the V_{DD} of the external I²C-bus master. Provides voltage-level translation.
$\overline{INT}$	C4	4	32	O	Interrupt output. Connect to $V_{DD(I2C\text{-}bus)}$ or $V_{DD(P)}$ through a pull-up resistor.
P0_0[1]	B1	5	1	I/O	Port 0 input/output 0.
P0_1[1]	D4	6	2	I/O	Port 0 input/output 1.
P0_2[1]	C1	7	3	I/O	Port 0 input/output 2.
P0_3[1]	D2	8	4	I/O	Port 0 input/output 3.
P0_4[1]	D1	9	5	I/O	Port 0 input/output 4.
P0_5[1]	E1	10	6	I/O	Port 0 input/output 5.
P0_6[1]	D3	11	7	I/O	Port 0 input/output 6.
P0_7[1]	F1	12	8	I/O	Port 0 input/output 7.
P1_0[2]	E2	13	9	I/O	Port 1 input/output 0.
P1_1[2]	F2	14	10	I/O	Port 1 input/output 1.
P1_2[2]	E3	15	11	I/O	Port 1 input/output 2.
P1_3[2]	F3	16	12	I/O	Port 1 input/output 3.
P1_4[2]	F4	17	13	I/O	Port 1 input/output 4.
P1_5[2]	E4	18	14	I/O	Port 1 input/output 5.
P1_6[2]	F5	19	15	I/O	Port 1 input/output 6.
P1_7[2]	E5	20	16	I/O	Port 1 input/output 7.
P2_0[3]	F6	21	17	I/O	Port 2 input/output 0.
P2_1[3]	E6	22	18	I/O	Port 2 input/output 1.
P2_2[3]	D5	23	19	I/O	Port 2 input/output 2.
P2_3[3]	D6	24	20	I/O	Port 2 input/output 3.
P2_4[3]	C5	25	21	I/O	Port 2 input/output 4.
P2_5[3]	C6	26	22	I/O	Port 2 input/output 5.
P2_6[3]	B5	27	23	I/O	Port 2 input/output 6.
P2_7[3]	B6	28	24	I/O	Port 2 input/output 7.
V_{SS}	A6	29	25	ground	Supply ground.
ADDR	A5	30	26	I	Address input. Connect directly to $V_{DD(I2C\text{-}bus)}$, ground, SCL or SDA.
$V_{DD(P)}$	A4	31	27	power supply	Supply voltage of PCAL6524 for Port P. 0.1 uF bypass capacitor required on this supply located as close to package as practical.

Table 3. Pin description *...continued*

Symbol	Pin				Description
	VFBGA36	TSSOP32	HUQFN32	Type	
$\overline{\text{RESET}}$	B4	32	28	I	Active LOW reset input. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor if no active connection is used.
n.c.	B2, B3, C2, C3	-	-	n.c.	Not connected

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-on, all I/Os are configured as inputs.

[2] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-on, all I/Os are configured as inputs.

[3] Pins P2_0 to P2_7 correspond to bits P2.0 to P2.7. At power-on, all I/Os are configured as inputs.

6. Functional description

Refer to Figure 1 “Block diagram (positive logic)”.

6.1 Device address

Following a START condition, the bus master must send the target slave address followed by a read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation bit. The slave address of the PCAL6524 is shown in Figure 5. Slave address pin ADDR chooses one of four slave addresses. Table 4 shows all four slave addresses by connecting the ADDR pin to SCL, SDA, V_{SS}, or V_{DD}.

Table 4. PCAL6524 address map

ADDR	Device family high-order address bits					Variable portion of address		Address
	A6	A5	A4	A3	A2	A1	A0	
SCL	0	1	0	0	0	0	0	40h
SDA	0	1	0	0	0	0	1	42h
V_{SS}	0	1	0	0	0	1	0	44h
V_{DD}	0	1	0	0	0	1	1	46h

The last bit of the first byte defines the reading from or writing to the PCAL6524. When set to logic 1 a read is selected, while logic 0 selects a write operation.

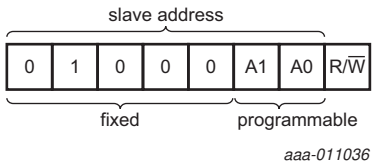


Fig 5. PCAL6524 address

6.2 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C-bus slave address	L	H	L	L	L	A1	A0	R/$\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

6.3 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the device.

- General Call address: allows to reset the device through the I²C-bus upon reception of the right I²C-bus sequence. See Section 6.3.1 “Software Reset” for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See Section 6.3.2 “Device ID (PCAL6524 ID field)” for more information.

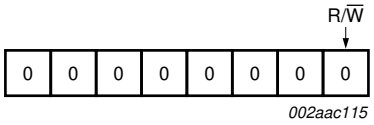


Fig 6. General Call address

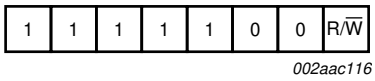


Fig 7. Device ID address

6.3.1 Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address ‘0000 000’ with the R/$\overline{W}$ bit set to 0 (write) is sent by the I²C-bus master.
3. The device acknowledges after seeing the General Call address ‘0000 0000’ (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

   If more than 1 byte of data is sent, the device does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 8.

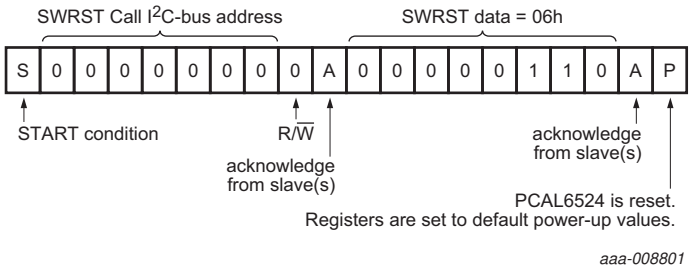


Fig 8. Software Reset sequence

6.3.2 Device ID (PCAL6524 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 0 (write): '1111 1000'.
3. The master sends the I²C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
4. The master sends a Re-START command.

   Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.
5. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 1 (read): '1111 1001'.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCAL6524, the Device ID is as shown in Figure 9.

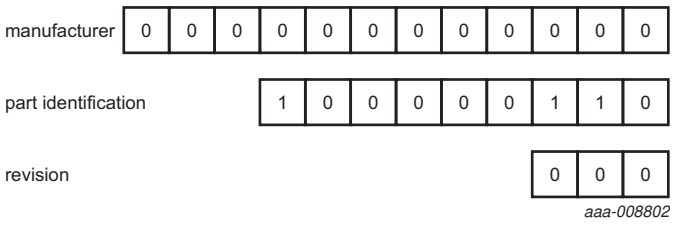
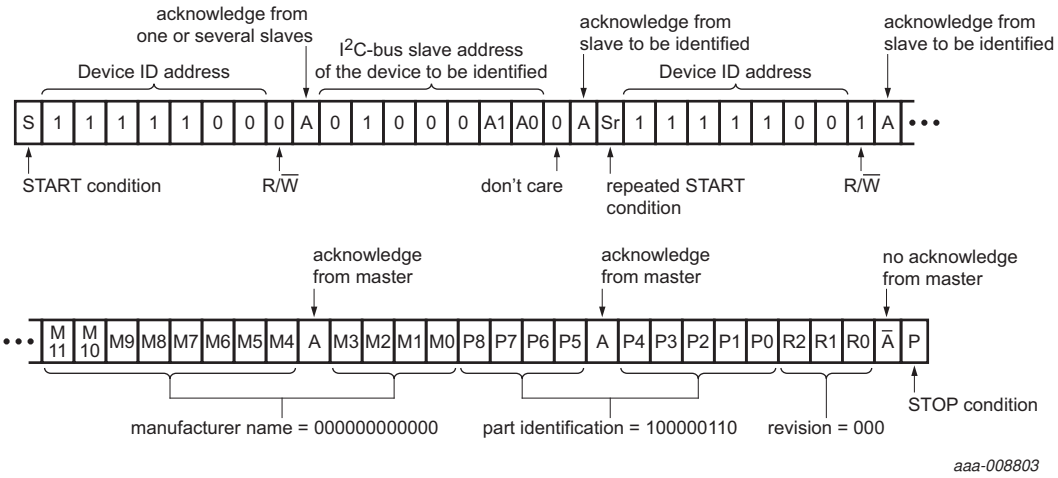


Fig 9. PCAL6524 Device ID field



If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

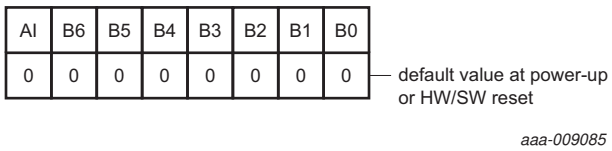
Fig 10. Device ID field reading

6.4 Pointer register and command byte

Following the successful acknowledgement of the slave address byte, the bus master sends a command byte, which is write only and stored in the pointer register in the PCAL6524. The lowest 7 bits (B[6:0] in Table 6) are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in Figure 11. At power-up, hardware or software reset, the pointer register defaults to 00h, with the AI bit set to '0' and the lowest seven bits set to '000 0000'.

When the Auto-Increment bit is set (AI = 1), the seven low-order bits of the pointer register are automatically incremented after a read or write until a STOP condition is encountered. This allows the user to program the registers sequentially without modifying the pointer register. The contents of these bits will roll over to '000 0000' after the last register (address = 76h) is accessed. Unimplemented register addresses (reserved registers) are skipped. If more than 52 bytes are written, the address will loop back to the register which is indicated by the seven low-order bits in the pointer register, and previously-written data will be overwritten. A STOP condition will keep the pointer register value in the last read or write location.

When the Auto-Increment bit is cleared (AI = 0), the 2 least significant bits are automatically incremented after a read or write for 3-register group which allows the user to program each of the 3-register group sequentially. If more than 3 bytes of data are read or written when AI is 0, previous data in the selected registers will be overwritten. For example: if input port 1 is read first, the next 2nd byte will be input port 2, and next 3nd byte will be input port 0, there is no limit on the number of data bytes for this read operation. There are two special 6-register groups: output drive strength (40h~45h) and interrupt edge (60h~65h) registers will allow user to program each of the 6-register group sequentially. Only Output port configuration register location (5Ch) remains in the same location after a successive read or write.



AI = Auto-Increment

Fig 11. Pointer register bits

Table 6. Command byte

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx[1]
0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx[1]
0	0	0	0	0	1	0	02h	Input port 2	read byte	xxxx xxxx[1]
0	0	0	0	0	1	1	03h	reserved[3]	reserved	reserved
0	0	0	0	1	0	0	04h	Output port 0	read/write byte	1111 1111
0	0	0	0	1	0	1	05h	Output port 1	read/write byte	1111 1111
0	0	0	0	1	1	0	06h	Output port 2	read/write byte	1111 1111
0	0	0	0	1	1	1	07h	reserved[3]	reserved	reserved
0	0	0	1	0	0	0	08h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	1	0	0	1	09h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	1	0	1	0	0Ah	Polarity Inversion port 2	read/write byte	0000 0000
0	0	0	1	0	1	1	0Bh	reserved[3]	reserved	reserved
0	0	0	1	1	0	0	0Ch	Configuration port 0	read/write byte	1111 1111
0	0	0	1	1	0	1	0Dh	Configuration port 1	read/write byte	1111 1111
0	0	0	1	1	1	0	0Eh	Configuration port 2	read/write byte	1111 1111
-	-	-	-	-	-	-	0Fh to 3Fh	reserved[3]	reserved	reserved
1	0	0	0	0	0	0	40h	Output drive strength register port 0A	read/write byte	1111 1111
1	0	0	0	0	0	1	41h	Output drive strength register port 0B	read/write byte	1111 1111
1	0	0	0	0	1	0	42h	Output drive strength register port 1A	read/write byte	1111 1111
1	0	0	0	0	1	1	43h	Output drive strength register port 1B	read/write byte	1111 1111
1	0	0	0	1	0	0	44h	Output drive strength register port 2A	read/write byte	1111 1111
1	0	0	0	1	0	1	45h	Output drive strength register port 2B	read/write byte	1111 1111
1	0	0	0	1	1	0	46h	reserved[3]	reserved	reserved
1	0	0	0	1	1	1	47h	reserved[3]	reserved	reserved
1	0	0	1	0	0	0	48h	Input latch register port 0	read/write byte	0000 0000
1	0	0	1	0	0	1	49h	Input latch register port 1	read/write byte	0000 0000
1	0	0	1	0	1	0	4Ah	Input latch register port 2	read/write byte	0000 0000
1	0	0	1	0	1	1	4Bh	reserved[3]	reserved	reserved
1	0	0	1	1	0	0	4Ch	Pull-up/pull-down enable register port 0	read/write byte	0000 0000
1	0	0	1	1	0	1	4Dh	Pull-up/pull-down enable register port 1	read/write byte	0000 0000
1	0	0	1	1	1	0	4Eh	Pull-up/pull-down enable register port 2	read/write byte	0000 0000
1	0	0	1	1	1	1	4Fh	reserved[3]	reserved	reserved
1	0	1	0	0	0	0	50h	Pull-up/pull-down selection register port 0	read/write byte	1111 1111
1	0	1	0	0	0	1	51h	Pull-up/pull-down selection register port 1	read/write byte	1111 1111
1	0	1	0	0	1	0	52h	Pull-up/pull-down selection register port 2	read/write byte	1111 1111

Table 6. Command byte *...continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	0	1	0	0	1	1	53h	reserved[3]	reserved	reserved
1	0	1	0	1	0	0	54h	Interrupt mask register port 0	read/write byte	1111 1111
1	0	1	0	1	0	1	55h	Interrupt mask register port 1	read/write byte	1111 1111
1	0	1	0	1	1	0	56h	Interrupt mask register port 2	read/write byte	1111 1111
1	0	1	0	1	1	1	57h	reserved[3]	reserved	reserved
1	0	1	1	0	0	0	58h	Interrupt status register port 0	read byte	0000 0000
1	0	1	1	0	0	1	59h	Interrupt status register port 1	read byte	0000 0000
1	0	1	1	0	1	0	5Ah	Interrupt status register port 2	read byte	0000 0000
1	0	1	1	0	1	1	5Bh	reserved[3]	reserved	reserved
1	0	1	1	1	0	0	5Ch[2]	Output port configuration register	read/write byte	0000 0000
1	0	1	1	1	0	1	5Dh	reserved[3]	reserved	reserved
1	0	1	1	1	1	0	5Eh	reserved[3]	reserved	reserved
1	0	1	1	1	1	1	5Fh	reserved[3]	reserved	reserved
1	1	0	0	0	0	0	60h	Interrupt edge register port 0A	read/write byte	0000 0000
1	1	0	0	0	0	1	61h	Interrupt edge register port 0B	read/write byte	0000 0000
1	1	0	0	0	1	0	62h	Interrupt edge register port 1A	read/write byte	0000 0000
1	1	0	0	0	1	1	63h	Interrupt edge register port 1B	read/write byte	0000 0000
1	1	0	0	1	0	0	64h	Interrupt edge register port 2A	read/write byte	0000 0000
1	1	0	0	1	0	1	65h	Interrupt edge register port 2B	read/write byte	0000 0000
1	1	0	0	1	1	0	66h	reserved[3]	reserved	reserved
1	1	0	0	1	1	1	67h	reserved[3]	reserved	reserved
1	1	0	1	0	0	0	68h	Interrupt clear register port 0	write byte	0000 0000
1	1	0	1	0	0	1	69h	Interrupt clear register port 1	write byte	0000 0000
1	1	0	1	0	1	0	6Ah	Interrupt clear register port 2	write byte	0000 0000
1	1	0	1	0	1	1	6Bh	reserved[3]	reserved	reserved
1	1	0	1	1	0	0	6Ch	Input status port 0	read byte	xxxx xxxx[1]
1	1	0	1	1	0	1	6Dh	Input status port 1	read byte	xxxx xxxx[1]
1	1	0	1	1	1	0	6Eh	Input status port 2	read byte	xxxx xxxx[1]
1	1	0	1	1	1	1	6Fh	reserved[3]	reserved	reserved
1	1	1	0	0	0	0	70h	Individual pin output port 0 configuration register	read/write byte	0000 0000
1	1	1	0	0	0	1	71h	Individual pin output port 1 configuration register	read/write byte	0000 0000
1	1	1	0	0	1	0	72h	Individual pin output port 2 configuration register	read/write byte	0000 0000
1	1	1	0	0	1	1	73h	reserved[3]	reserved	reserved
1	1	1	0	1	0	0	74h	Switch debounce enable 0	read/write byte	0000 0000
1	1	1	0	1	0	1	75h	Switch debounce enable 1	read/write byte	0000 0000

Table 6. Command byte *...continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	1	1	0	1	1	0	76h	Switch debounce count	read/write byte	0000 0000
-	-	-	-	-	-	-	77h to 7Fh	reserved[3]	reserved	reserved

[1] Undefined.

[2] Successive read and write accesses to remain at this register address.

[3] These registers marked “reserved” should not be written, and the master will not be acknowledged when accessed.

6.5 Register descriptions

6.5.1 Input port registers (00h, 01h, 02h)

The Input port registers (registers 00h, 01h, 02h) reflect the incoming logic levels of the pins. The Input port registers are read only; writes to these registers have no effect and the transaction will be acknowledged (ACK). The default value 'X' is determined by the externally applied logic level. If a pin is configured as an output (registers 04h, 05h, 06h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (register 5Ch and registers 70h, 71h, 72h), the input port value is forced to 0. An Input port register group read operation is performed as described in Section 7.2.

After reading input port registers, all interrupts will be cleared.

Table 7. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 8. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Table 9. Input port 2 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	I2.7	I2.6	I2.5	I2.4	I2.3	I2.2	I2.1	I2.0
Default	X	X	X	X	X	X	X	X

6.5.2 Output port registers (04h, 05h, 06h)

The Output port registers (registers 04h, 05h, 06h) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register group write is described in Section 7.1 and a register group read is described in Section 7.2.

Table 10. Output port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 11. Output port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Table 12. Output port 2 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	O2.7	O2.6	O2.5	O2.4	O2.3	O2.2	O2.1	O2.0
Default	1	1	1	1	1	1	1	1

6.5.3 Polarity inversion registers (08h, 09h, 0Ah)

The Polarity inversion registers (registers 08h, 09h, 0Ah) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register group write is described in Section 7.1 and a register group read is described in Section 7.2.

Table 13. Polarity inversion port 0 register (address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 14. Polarity inversion port 1 register (address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Table 15. Polarity inversion port 2 register (address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	N2.7	N2.6	N2.5	N2.4	N2.3	N2.2	N2.1	N2.0
Default	0	0	0	0	0	0	0	0

6.5.4 Configuration registers (0Ch, 0Dh, 0Eh)

The Configuration registers (registers 0Ch, 0Dh, 0Eh) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register group write is described in Section 7.1 and a register group read is described in Section 7.2.

Table 16. Configuration port 0 register (address 0Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 17. Configuration port 1 register (address 0Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Table 18. Configuration port 2 register (address 0Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
Default	1	1	1	1	1	1	1	1

6.5.5 Output drive strength registers (40h, 41h, 42h, 43h, 44h, 45h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 41h CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41h CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See Section 8.1 “Output drive strength control” for more details. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 19. Current control port 0A register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 20. Current control port 0B register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 21. Current control port 1A register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 22. Current control port 1B register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

Table 23. Current control port 2A register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.3		CC2.2		CC2.1		CC2.0	
Default	1	1	1	1	1	1	1	1

Table 24. Current control port 2B register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.7		CC2.6		CC2.5		CC2.4	
Default	1	1	1	1	1	1	1	1

6.5.6 Input latch registers (48h, 49h, 4Ah)

The input latch registers (registers 48h, 49h, 4Ah) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0, 1 and 2). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 21.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port register bit 4 register should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is cleared if the input latch register changes from latched to non-latched configuration and I/O pin returns to its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 25. Input latch port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 26. Input latch port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

Table 27. Input latch port 2 register (address 4Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	L2.7	L2.6	L2.5	L2.4	L2.3	L2.2	L2.1	L2.0
Default	0	0	0	0	0	0	0	0

6.5.7 Pull-up/pull-down enable registers (4Ch, 4Dh, 4Eh)

The pull-up and pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 6.5.11 and Section 6.5.15). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 28. Pull-up/pull-down enable port 0 register (address 4Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 29. Pull-up/pull-down enable port 1 register (address 4Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

Table 30. Pull-up/pull-down enable port 2 register (address 4Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	PE2.7	PE2.6	PE2.5	PE2.4	PE2.3	PE2.2	PE2.1	PE2.0
Default	0	0	0	0	0	0	0	0

6.5.8 Pull-up/pull-down selection registers (50h, 51h, 52h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 31. Pull-up/pull-down selection port 0 register (address 50h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 32. Pull-up/pull-down selection port 1 register (address 51h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

Table 33. Pull-up/pull-down selection port 2 register (address 52h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD2.7	PUD2.6	PUD2.5	PUD2.4	PUD2.3	PUD2.2	PUD2.1	PUD2.0
Default	1	1	1	1	1	1	1	1

6.5.9 Interrupt mask registers (54h, 55h, 56h)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 34. Interrupt mask port 0 register (address 54h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 35. Interrupt mask port 1 register (address 55h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

Table 36. Interrupt mask port 2 register (address 56h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M2.7	M2.6	M2.5	M2.4	M2.3	M2.2	M2.1	M2.0
Default	1	1	1	1	1	1	1	1

6.5.10 Interrupt status registers (58h, 59h, 5Ah)

The read-only interrupt status registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register group read operation is described in Section 7.2.

Table 37. Interrupt status port 0 register (address 58h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 38. Interrupt status port 1 register (address 59h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

Table 39. Interrupt status port 2 register (address 5Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S2.7	S2.6	S2.5	S2.4	S2.3	S2.2	S2.1	S2.0
Default	0	0	0	0	0	0	0	0

6.5.11 Output port configuration register (5Ch)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 12). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (5Ch) before the Configuration register (0Ch, 0Dh, 0Eh) sets the port pins as outputs.

ODEN0 configures Port 0_x, ODEN1 configures Port 1_x, and ODEN2 configures Port 2_x.

Individual pins may be programmed as open-drain or push-pull by programming Individual Pin Output Configuration registers (70h, 71h, 72h). See Section 6.5.15 for more information.

A register group read or write operation is not allowed on this register. Successive read or write accesses will remain at this register address.

Table 40. Output port configuration register (address 5Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					ODEN2	ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

6.5.12 Interrupt edge registers (60h, 61h, 62h and 63h, 64h, 65h)

The interrupt edge registers determine what action on an input pin will cause an interrupt along with the Interrupt Mask registers (54h, 55h and 56h). If the Interrupt is enabled (set '0' in the Mask register) and the action at the corresponding pin matches the required activity, the $\overline{INT}$ output will become active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input port (00h, 01h or 02h) which can be latched with a corresponding '1' set in the Input Latch register (48h, 49h, 4Ah). If the Interrupt edge register entry is set to 11b, any edge, positive- or negative-going, causes an interrupt event. If an entry is 01b, only a positive-going edge will cause an interrupt event, while a 10b will require a negative-going edge to cause an interrupt event. These edge interrupt events are latched, regardless of the status of the Input Latch register (48h, 49h, 4Ah). These edged interrupts can be cleared in a number of ways: Reading input port registers (00h, 01h, 02h); setting the Interrupt Mask register (54h, 55h, 56h) to 1 (masked); setting the Interrupt Clear register (68h, 69h, 6Ah) to 1 (this is a write-only register); resetting the Interrupt Edge register (60h to 65h) back to 0. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 41. Interrupt edge port 0A register (address 60h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Table 42. Interrupt edge port 0B register (address 61h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Table 43. Interrupt edge port 1A register (address 62h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Table 44. Interrupt edge port 1B register (address 63h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.7		IE1.6		IE1.5		IE1.4	
Default	0	0	0	0	0	0	0	0

Table 45. Interrupt edge port 2A register (address 64h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.3		IE2.2		IE2.1		IE2.0	
Default	0	0	0	0	0	0	0	0

Table 46. Interrupt edge port 2B register (address 65h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.7		IE2.6		IE2.5		IE2.4	
Default	0	0	0	0	0	0	0	0

Table 47. Interrupt edge bits (IEx.x)

Bit 1	Bit 0	Description
0	0	level-triggered interrupt
0	1	positive-going (rising) edge triggered interrupt
1	0	negative-going (falling) edge triggered interrupt
1	1	any edge (positive or negative-going) triggered interrupt

6.5.13 Interrupt clear registers (68h, 69h, 6Ah)

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the $\overline{INT}$ will be cleared. After writing a logic 1 the bit returns to logic 0. A register group write operation is described in Section 7.1.

Table 48. Interrupt clear port 0 register (address 68h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

Table 49. Interrupt clear port 1 register (address 69h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC1.7	IC1.6	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	0	0	0	0	0	0	0	0

Table 50. Interrupt clear port 2 register (address 6Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC2.7	IC2.6	IC2.5	IC2.4	IC2.3	IC2.2	IC2.1	IC2.0
Default	0	0	0	0	0	0	0	0

6.5.14 Input status registers (6Ch, 6Dh, 6Eh)

The read-only input status registers function exactly like Input Port 0, 1 and 2 (00h, 01h, 02h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the Configuration register (0Ch, 0Dh, 0Eh), and is also configured as open-drain (register 5Ch and 70h, 71h, 72h), the read for that pin will always return 0, otherwise that state of that pin is returned. A register group read operation is described in Section 7.2.

Table 51. Input status port 0 register (address 6Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II0.7	II0.6	II0.5	II0.4	II0.3	II0.2	II0.1	II0.0
Default	X	X	X	X	X	X	X	X

Table 52. Input status port 1 register (address 6Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II1.7	II1.6	II1.5	II1.4	II1.3	II1.2	II1.1	II1.0
Default	X	X	X	X	X	X	X	X

Table 53. Input status port 2 register (address 6Eh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II2.7	II2.6	II2.5	II2.4	II2.3	II2.2	II2.1	II2.0
Default	X	X	X	X	X	X	X	X

6.5.15 Individual pin output configuration registers (70h, 71h, 72h)

The individual pin output configuration registers modify output configuration (push-pull or open-drain) set by the Output Port Configuration register (5Ch).

If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the IOCRx register will reverse the output state of that pin only to open-drain. When ODENx bit is set at logic 1 (open-drain), a logic 1 in IOCRx will set that pin to push-pull.

The recommended command sequence to program the output pin is to program ODENx (5Ch), the IOCRx, and finally the Configuration register (0Ch, 0Dh, 0Eh) to set the pins as outputs. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 54. Individual pin output configuration register 0 (address 70h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

Table 55. Individual pin output configuration register 1 (address 71h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR1.7	IOCR1.6	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	0	0	0	0	0	0	0	0

Table 56. Individual pin output configuration register 2 (address 72h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR2.7	IOCR2.6	IOCR2.5	IOCR2.4	IOCR2.3	IOCR2.2	IOCR2.1	IOCR2.0
Default	0	0	0	0	0	0	0	0

6.5.16 Switch debounce enable registers (74h, 75h)

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P0_0 is designated as the oscillator input. If P0_0 is not configured as input and if SD0.0 is not set to logic 1, then switch debounce logic is not connected to any pin. See Section 6.10 “Switch debounce circuitry” for additional information about Switch debounce logic functionality.

Table 57. Switch debounce enable Port 0 register (address 74h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

Table 58. Switch debounce enable Port 1 register (address 75h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD1.7	SD1.6	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	0	0	0	0	0	0	0	0

6.5.17 Switch debounce count register (76h)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P0_0, determines the debounce time (for example, the debounce time will be 10 μs if this register is set to 0Ah and external oscillator frequency is 1 MHz). See Section 6.10 “Switch debounce circuitry” for further information.

Table 59. Switch debounce count register (address 76h) bit description [1]

Bit	7	6	5	4	3	2	1	0
Symbol	SDC0.7	SDC0.6	SDC0.5	SDC0.4	SDC0.3	SDC0.2	SDC0.1	SDC0.0
Default	0	0	0	0	0	0	0	0

[1] The switch debounce logic is disabled if this register is set to 00h.