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PCAL9535A

Low-voltage 16-bit I²C-bus I/O port with interrupt and Agile I/O

Rev. 2 — 23 January 2015

Product data sheet

1. General description

The PCAL9535A is a low-voltage 16-bit General Purpose Input/Output (GPIO) expander with interrupt and reset for I²C-bus/SMBus applications. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs, fan control, etc.

In addition to providing a flexible set of GPIOs, the wide V_{DD} range of 1.65 V to 5.5 V allows the PCAL9535A to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCAL9535A contains the PCA9535 register set of four pairs of 8-bit Configuration, Input, Output, and Polarity Inversion registers, and additionally, the PCAL9535A has Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

The PCAL9535A is a pin-to-pin replacement to the PCA9535 and PCA9535A, however, the PCAL9535A powers up with all I/O interrupts masked. This mask default allows for a board bring-up free of spurious interrupts at power-up.

The PCAL9535A open-drain interrupt (\overline{INT}) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

\overline{INT} can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCAL9535A can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) select the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus.



2. Features and benefits

- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
 - ◆ 1.5 μ A (typical at 5 V V_{DD})
 - ◆ 1.0 μ A (typical at 3.3 V V_{DD})
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
 - ◆ $V_{hys} = 0.10 \times V_{DD}$ (typical)
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output (\overline{INT})
- 400 kHz Fast-mode I²C-bus
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection exceeds JESD22
 - ◆ 2000 V Human Body Model (A114-A)
 - ◆ 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP24, HVQFN24

2.1 Agile I/O features

- Pin to pin replacement for PCA9535 and PCA9535A with interrupts disabled at power-up
 - ◆ Software backward compatible with PCA9535 and PCA9535A
- Output port configuration: bank selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
 - ◆ Output drive strength: four programmable drive strengths to reduce rise and fall times in low capacitance applications
 - ◆ Input latch: Input Port register values changes are kept until the Input Port register is read
 - ◆ Pull-up/pull-down enable: floating input or pull-up/down resistor enable
 - ◆ Pull-up/pull-down selection: 100 k Ω pull-up/down resistor selection
 - ◆ Interrupt mask: mask prevents the generation of the interrupt when input changes state

3. Ordering information

Table 1. Ordering information

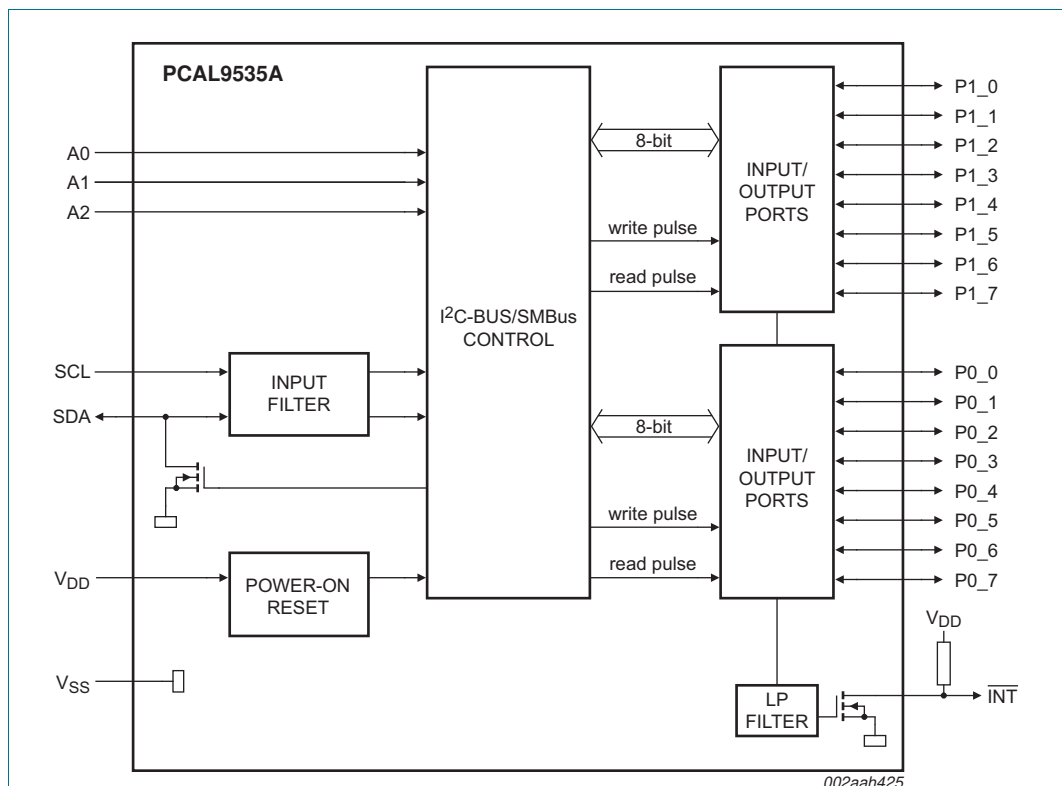
Type number	Topside marking	Package		Version
		Name	Description	
PCAL9535AHF	L35A	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm	SOT994-1
PCAL9535APW	PCAL9535A	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCAL9535AHF	PCAL9535AHF,128	HWQFN24	Reel pack, SMD, 13-inch, Turned	6000	-40 °C to +85 °C
PCAL9535APW	PCAL9535APW,118	TSSOP24	Reel pack, SMD, 13-inch	2500	-40 °C to +85 °C

4. Block diagram

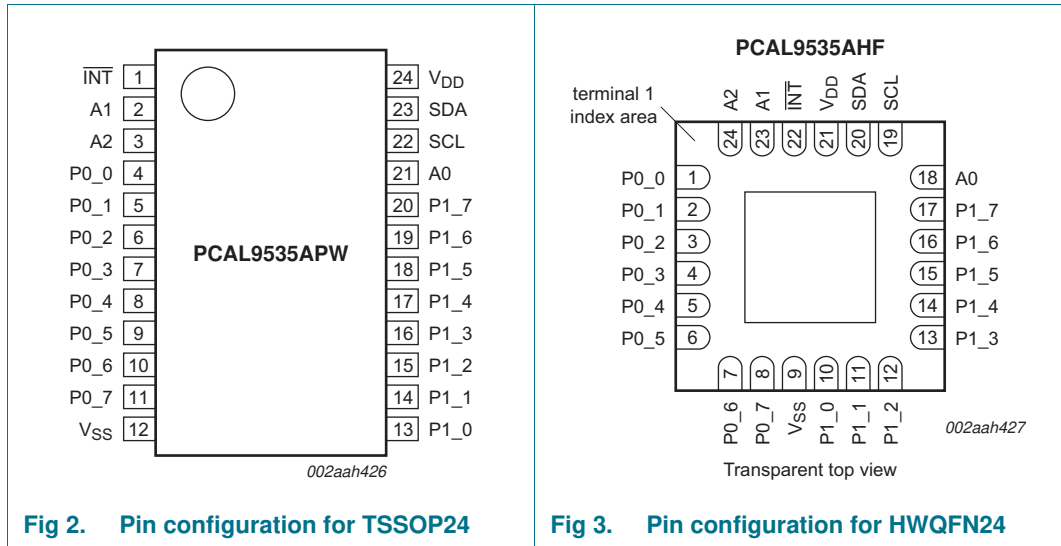


Remark: All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCAL9535A

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	TSSOP24	HWQFN24		
$\overline{\text{INT}}$	1	22	O	Interrupt output. Connect to V _{DD} through a pull-up resistor.
A1	2	23	I	Address input 1. Connect directly to V _{DD} or V _{SS} .
A2	3	24	I	Address input 2. Connect directly to V _{DD} or V _{SS} .
P0_0 ^[2]	4	1	I/O	Port 0 input/output 0.
P0_1 ^[2]	5	2	I/O	Port 0 input/output 1.
P0_2 ^[2]	6	3	I/O	Port 0 input/output 2.
P0_3 ^[2]	7	4	I/O	Port 0 input/output 3.
P0_4 ^[2]	8	5	I/O	Port 0 input/output 4.
P0_5 ^[2]	9	6	I/O	Port 0 input/output 5.
P0_6 ^[2]	10	7	I/O	Port 0 input/output 6.
P0_7 ^[2]	11	8	I/O	Port 0 input/output 7.
V _{SS}	12	9 ^[1]	power	Ground.
P1_0 ^[3]	13	10	I/O	Port 1 input/output 0.
P1_1 ^[3]	14	11	I/O	Port 1 input/output 1.
P1_2 ^[3]	15	12	I/O	Port 1 input/output 2.
P1_3 ^[3]	16	13	I/O	Port 1 input/output 3.
P1_4 ^[3]	17	14	I/O	Port 1 input/output 4.
P1_5 ^[3]	18	15	I/O	Port 1 input/output 5.
P1_6 ^[3]	19	16	I/O	Port 1 input/output 6.

Table 3. Pin description ...continued

Symbol	Pin		Type	Description
	TSSOP24	HWQFN24		
P1_7 ^[3]	20	17	I/O	Port 1 input/output 7.
A0	21	18	I	Address input 0. Connect directly to V _{DD} or V _{SS} .
SCL	22	19	I	Serial clock bus. Connect to V _{DD} through a pull-up resistor.
SDA	23	20	I/O	Serial data bus. Connect to V _{DD} through a pull-up resistor.
V _{DD}	24	21	power	Supply voltage.

- [1] HWQFN24 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.
- [2] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-up, all I/O are configured as high-impedance inputs.
- [3] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-up, all I/O are configured as high-impedance inputs.

6. Functional description

Refer to [Figure 1 “Block diagram of PCAL9535A”](#).

6.1 Device address

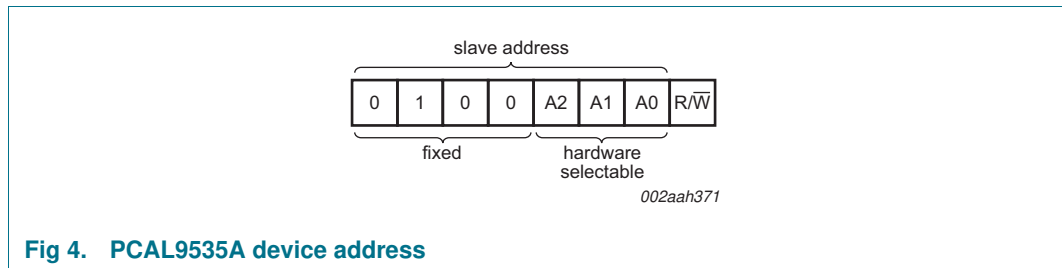


Fig 4. PCAL9535A device address

A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/W) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

6.2 Registers

6.2.1 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCAL9535A. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. Bit 6 in conjunction with the lower four bits of the Command byte are used to point to the extended features of the device (Agile I/O). This register is write only.

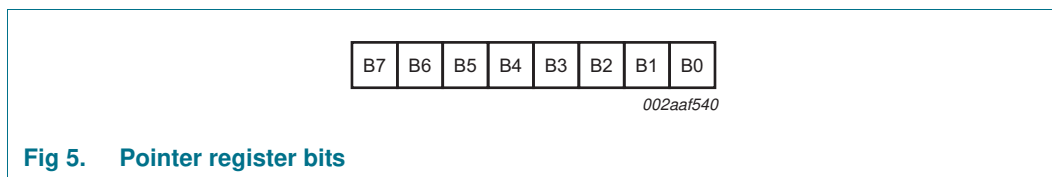


Table 4. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx ^[1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111
0	1	0	0	0	0	0	0	40h	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	0	1	41h	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	1	0	42h	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	0	1	1	43h	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	1	0	0	44h	Input latch register 0	read/write byte	0000 0000
0	1	0	0	0	1	0	1	45h	Input latch register 1	read/write byte	0000 0000
0	1	0	0	0	1	1	0	46h	Pull-up/pull-down enable register 0	read/write byte	0000 0000
0	1	0	0	0	1	1	1	47h	Pull-up/pull-down enable register 1	read/write byte	0000 0000
0	1	0	0	1	0	0	0	48h	Pull-up/pull-down selection register 0	read/write byte	1111 1111
0	1	0	0	1	0	0	1	49h	Pull-up/pull-down selection register 1	read/write byte	1111 1111
0	1	0	0	1	0	1	0	4Ah	Interrupt mask register 0	read/write byte	1111 1111
0	1	0	0	1	0	1	1	4Bh	Interrupt mask register 1	read/write byte	1111 1111
0	1	0	0	1	1	0	0	4Ch	Interrupt status register 0	read byte	0000 0000
0	1	0	0	1	1	0	1	4Dh	Interrupt status register 1	read byte	0000 0000
0	1	0	0	1	1	1	1	4Fh	Output port configuration register	read/write byte	0000 0000

[1] Undefined.

6.2.2 Input port register pair (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in [Section 7.2 "Reading the port registers"](#).

Table 5. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

6.2.3 Output port register pair (02h, 03h)

The Output port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 7. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

6.2.4 Polarity inversion register pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the Input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 9. Polarity inversion port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10. Polarity inversion port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

6.2.5 Configuration register pair (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 11. Configuration port 0 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12. Configuration port 1 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

6.2.6 Output drive strength register pairs (40h, 41h, 42h, 43h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example, Port 0.7 is controlled by register 41 bits CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41 CC0.6(bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25x, 01b = 0.50x, 10b = 0.75x, or 11b = 1x of the maximum drive capability of the I/O. See [Section 8.2 “Output drive strength control”](#). A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 13. Current control port 0 register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 14. Current control port 0 register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 15. Current control port 1 register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 16. Current control port 1 register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

6.2.7 Input latch register pair (44h, 45h)

The input latch registers (registers 44 and 45) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change of the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state in the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See [Figure 12 “Read input port register \(latch enabled\), scenario 3”](#).

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is

cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port 0 register bit 4 register should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration. If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 17. Input latch port 0 register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 18. Input latch port 1 register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

6.2.8 Pull-up/pull-down enable register pair (46h, 47h)

These registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see [Section 6.2.12](#)). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 19. Pull-up/pull-down enable port 0 register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 20. Pull-up/pull-down enable port 1 register (address 47h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

6.2.9 Pull-up/pull-down selection register pair (48h, 49h)

The I/O port can be configured to have a pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 k Ω pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 k Ω pull-down resistor for that I/O pin. If the pull-up/pull-down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 k Ω with minimum of 50 k Ω and maximum of 150 k Ω . A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 21. Pull-up/pull-down selection port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 22. Pull-up/pull-down selection port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

6.2.10 Interrupt mask register pair (4Ah, 4Bh)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 23. Interrupt mask port 0 register (address 4Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 24. Interrupt mask port 1 register (address 4Bh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

6.2.11 Interrupt status register pair (4Ch, 4Dh)

These read-only registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

Table 25. Interrupt status port 0 register (address 4Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 26. Interrupt status port 1 register (address 4Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

6.2.12 Output port configuration register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see [Figure 6](#)). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence to program this register (4Fh) before the configuration registers (06h, 07h) sets the port pins as outputs.

ODEN0 configures Port 0_x and ODEN1 configures Port 1_x.

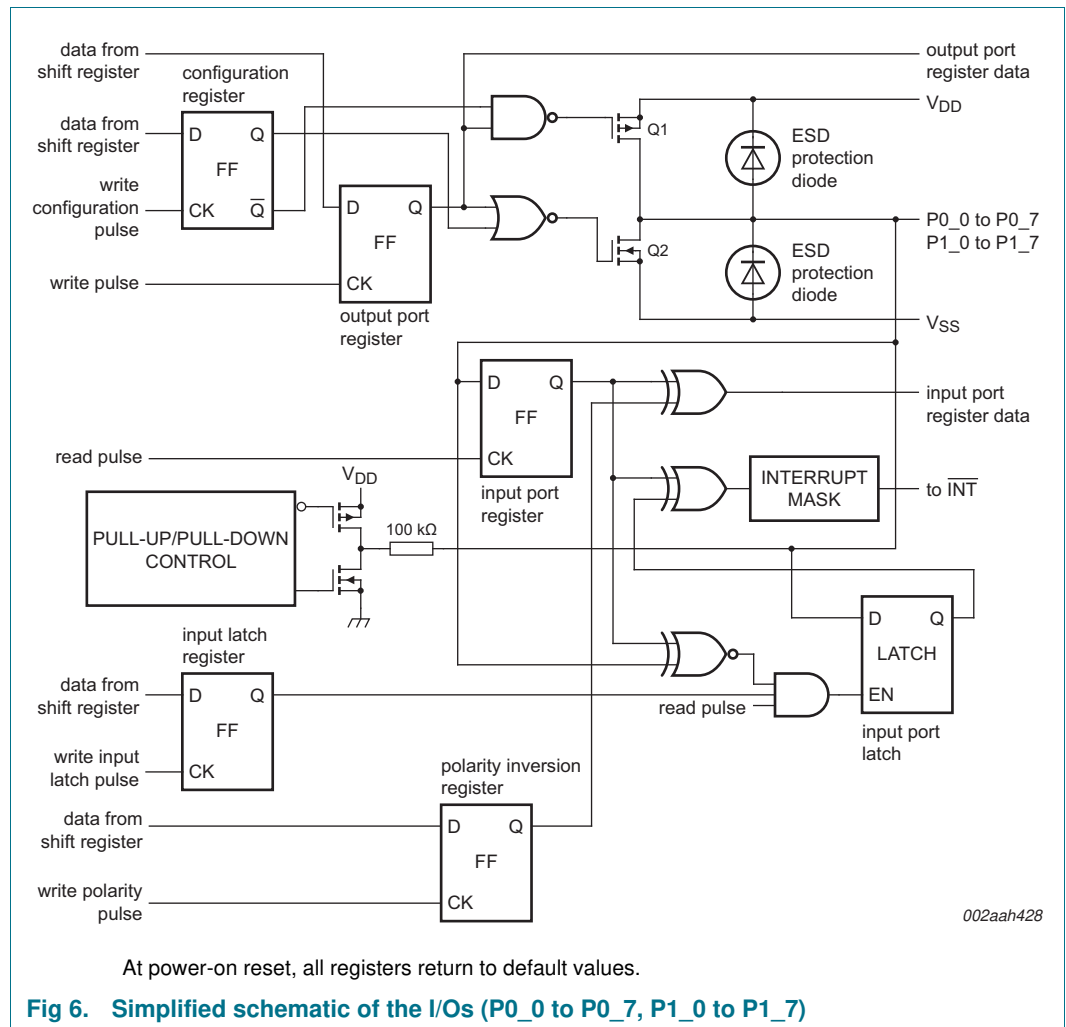
Table 27. Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

6.3 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{DD} or V_{SS} . The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



6.4 Power-on reset

When power (from 0 V) is applied to V_{DD} , an internal power-on reset holds the PCAL9535A in a reset condition until V_{DD} has reached V_{POR} . At that time, the reset condition is released and the PCAL9535A registers and I²C-bus/SMBus state machine initializes to their default states. After that, V_{DD} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle. See [Section 8.3 “Power-on reset requirements”](#).

6.5 Interrupt output

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{V(INT)}$, the signal \overline{INT} is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt (see [Figure 10](#)). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as \overline{INT} .

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The \overline{INT} output has an open-drain structure and requires pull-up resistor to V_{DD} .

When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

7. Bus transactions

The PCAL9535A is an I²C-bus slave device. Data is exchanged between the master and PCAL9535A through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Writing to the port registers

Data is transmitted to the PCAL9535A by sending the device address and setting the least significant bit to a logic 0 (see [Figure 4 “PCAL9535A device address”](#)). The command byte is sent after the address and determines which register will receive the data following the command byte.

Twenty-two registers within the PCAL9535A are configured to operate as eleven register pairs. The eleven pairs are input port, output port, polarity inversion, configuration, output drive strength (two 16-bit registers), input latch, pull-up/pull-down enable, pull-up/pull-down selection, interrupt mask, and interrupt status registers. After sending data to one register, the next data byte is sent to the other register in the pair (see [Figure 7](#) and [Figure 8](#)). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers, or the host can simply update a single register.

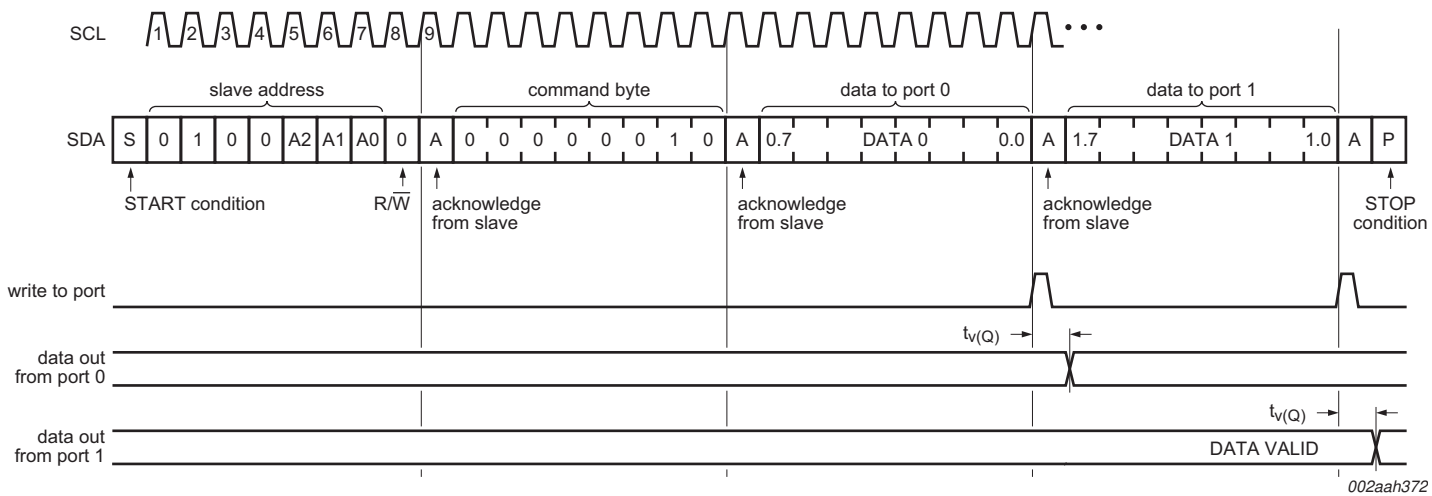


Fig 7. Write to output port registers

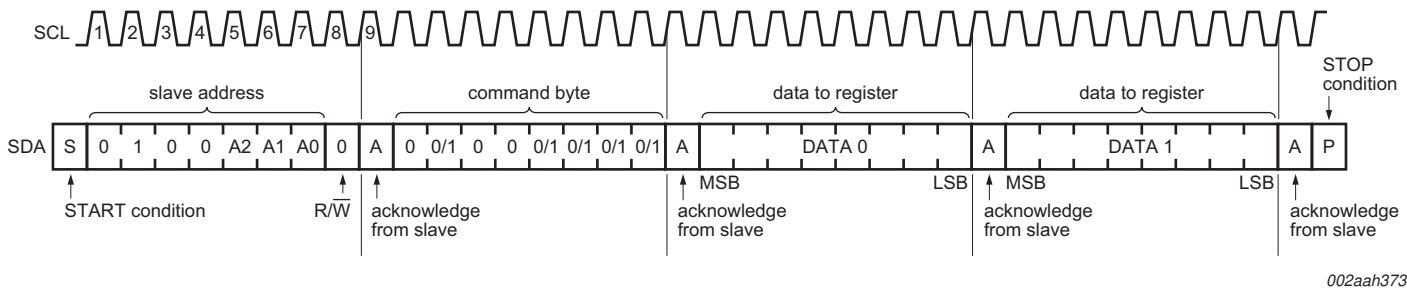
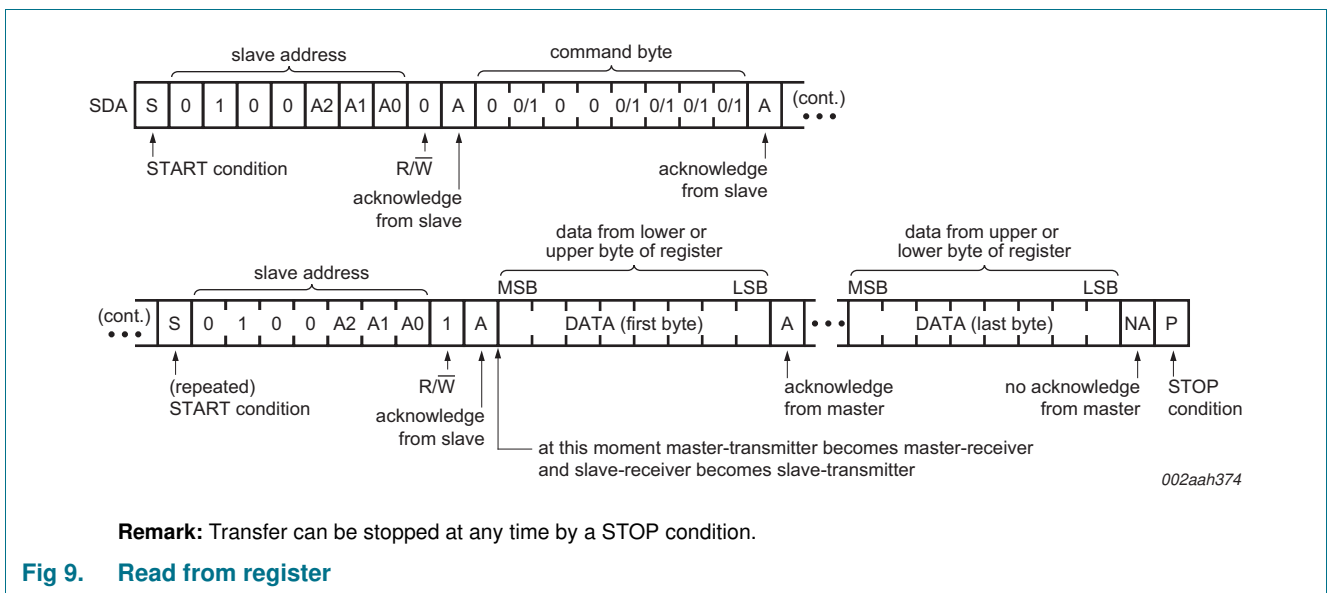


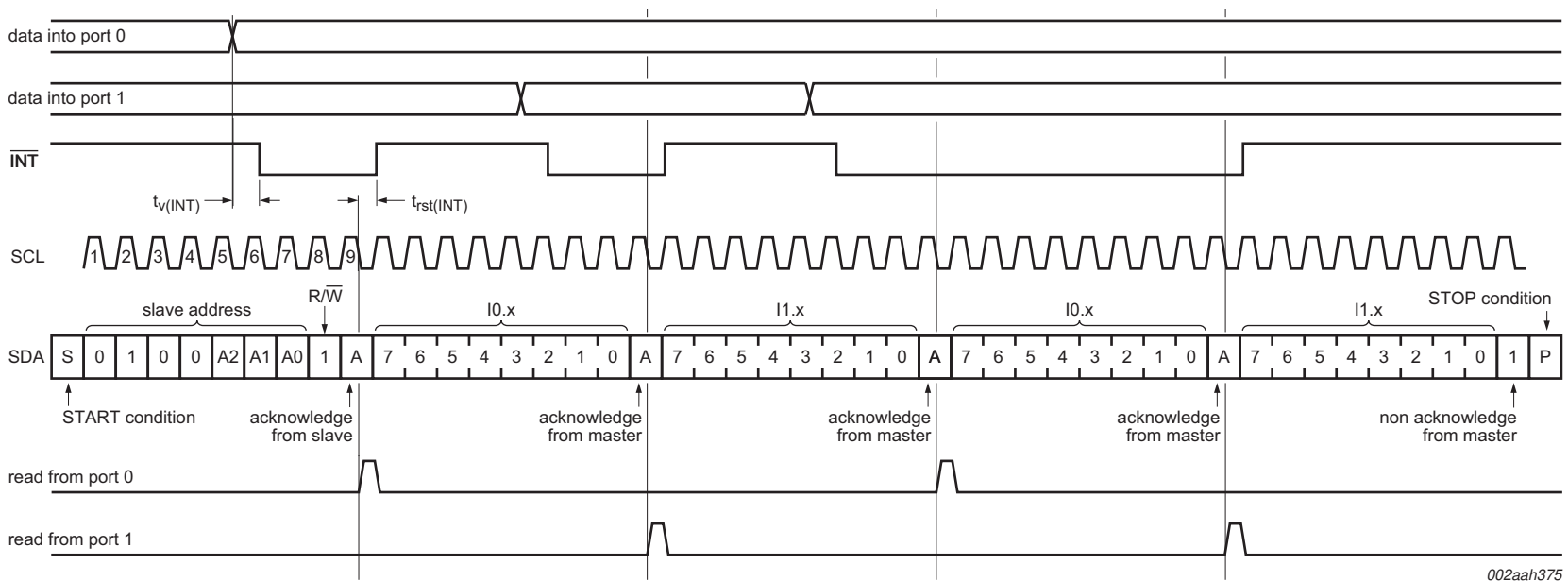
Fig 8. Write to Control registers

7.2 Reading the port registers

In order to read data from the PCAL9535A, the bus master must first send the PCAL9535A address with the least significant bit set to a logic 0 (see [Figure 4](#) “PCAL9535A device address”). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the PCAL9535A (see [Figure 9](#), [Figure 10](#) and [Figure 11](#)). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

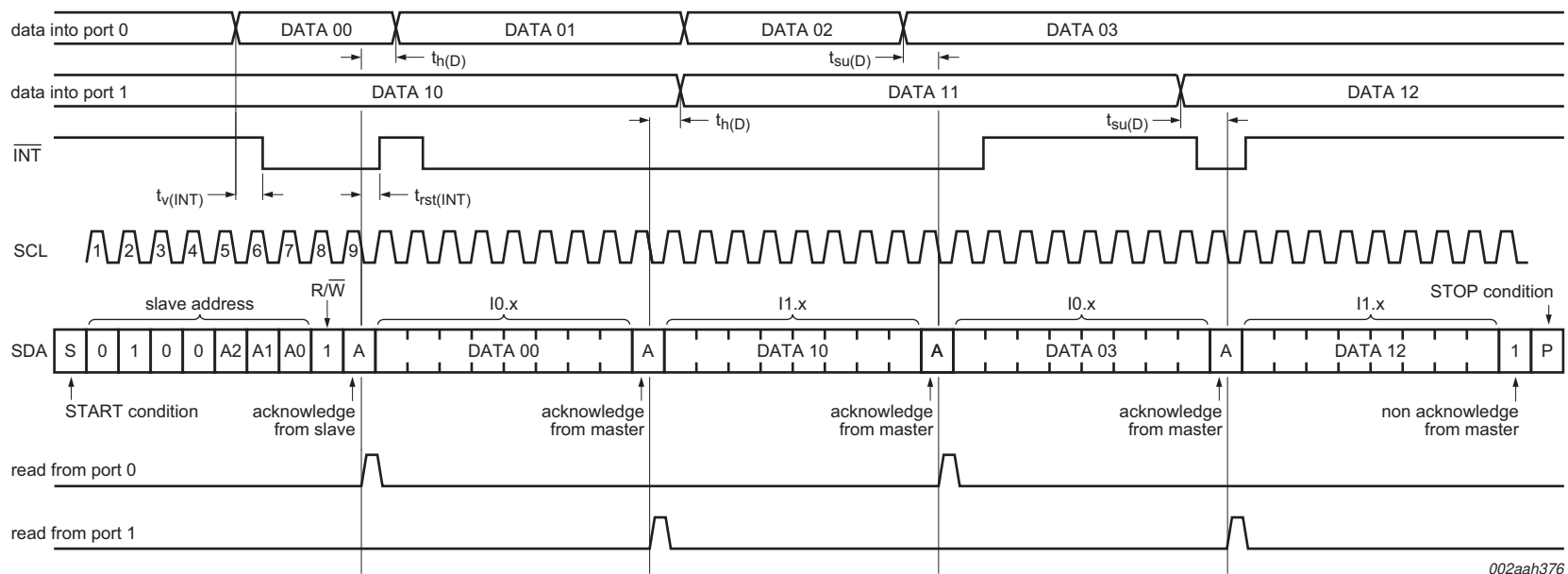
After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.





Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

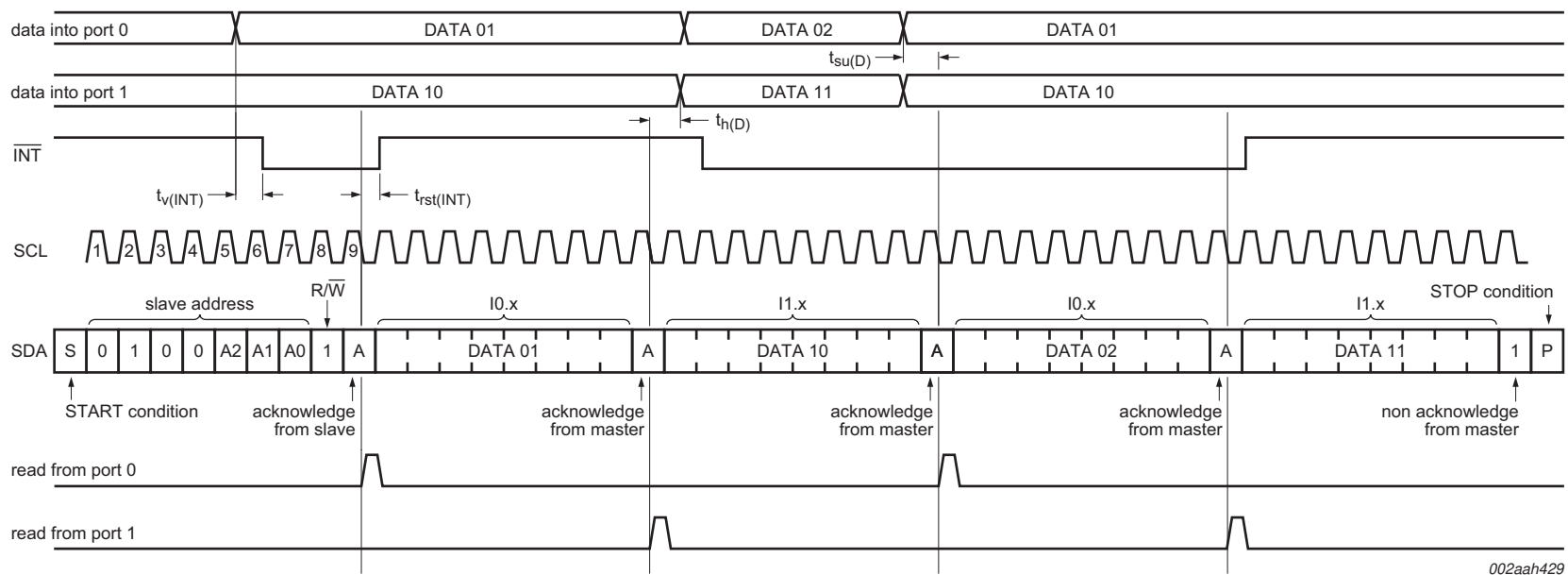
Fig 10. Read input port register (input latch disabled), scenario 1



002aah376

Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

Fig 11. Read input port register (non-latched), scenario 2

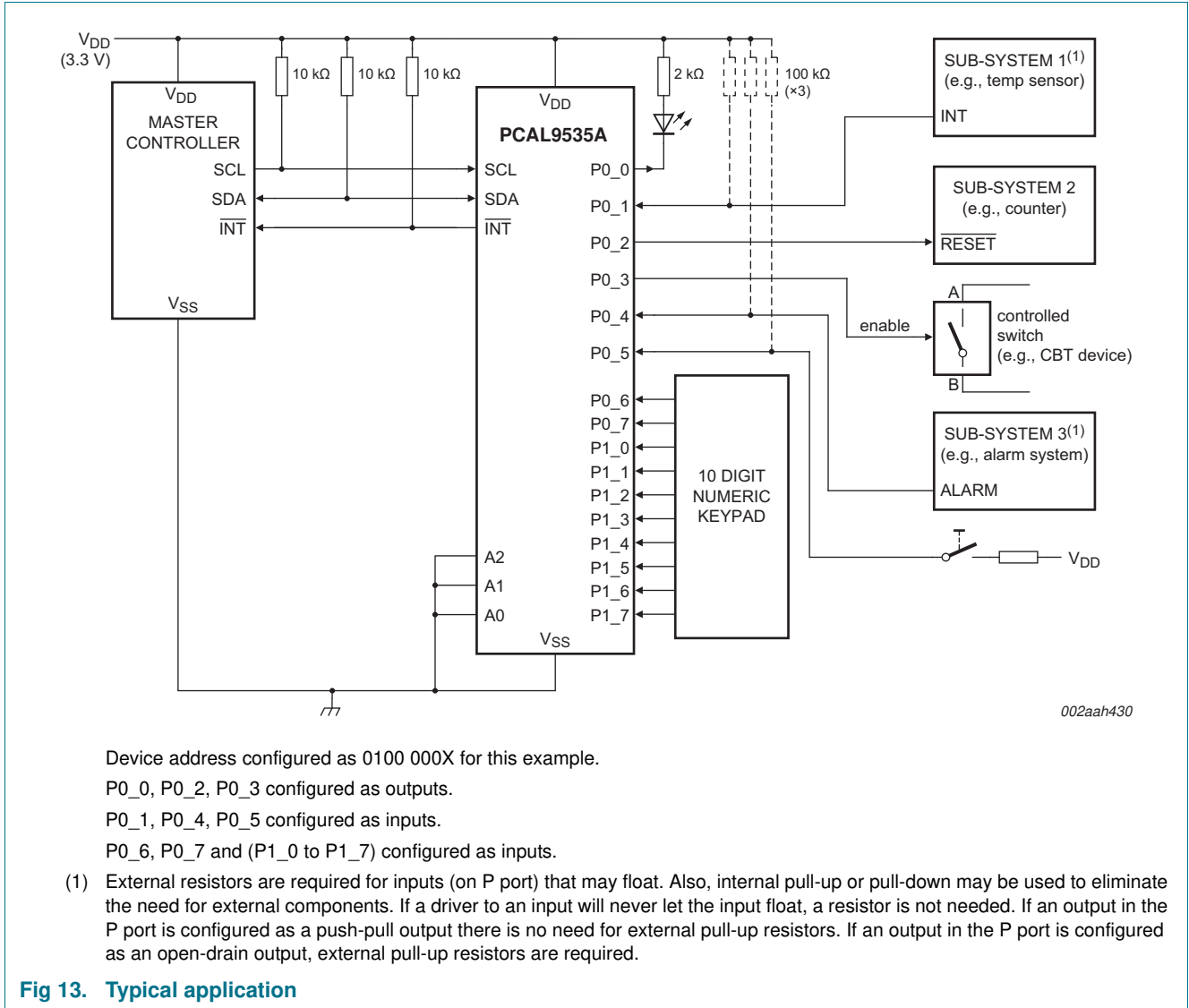


002aah429

Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

Fig 12. Read input port register (latch enabled), scenario 3

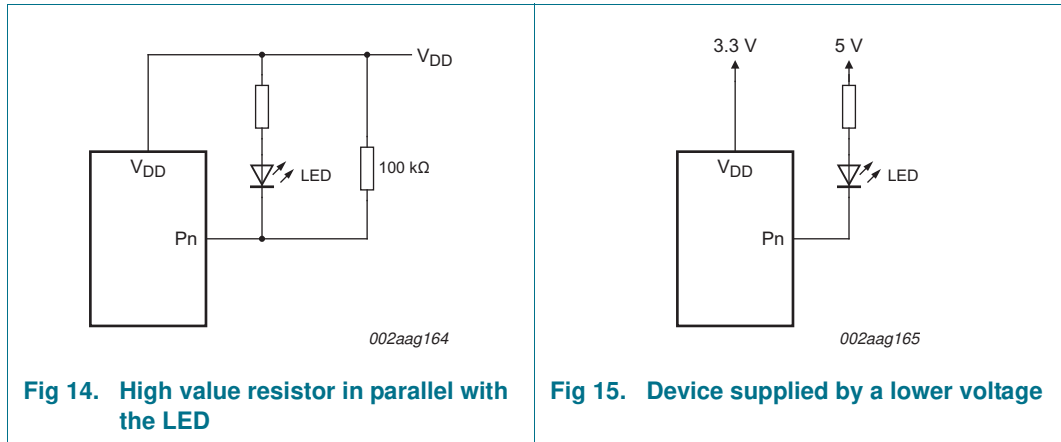
8. Application design-in information



8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.



8.2 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or ‘fingers’ that drive the I/O pad.

Figure 16 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 10b, then only two of the fingers are active, reducing the current drive capability by 50 %.

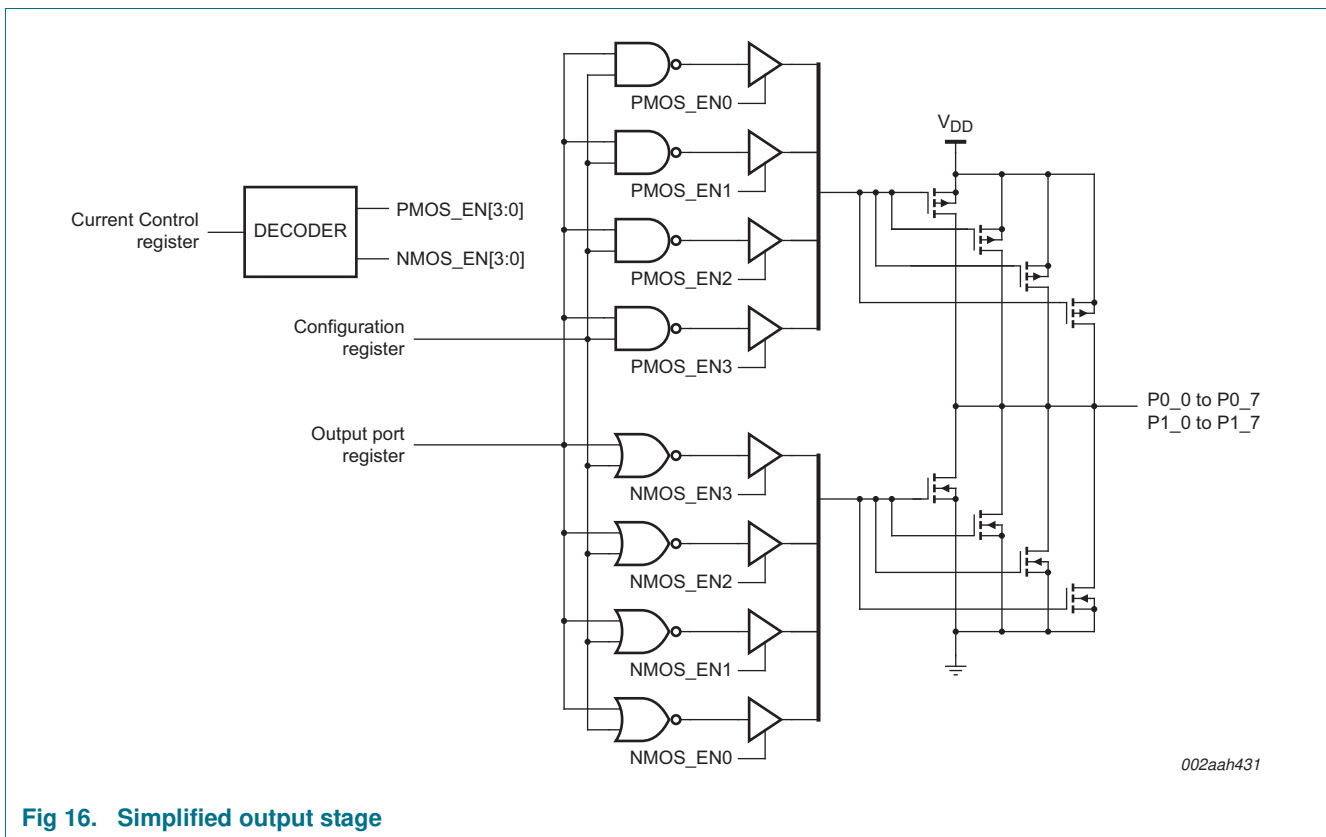


Fig 16. Simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Current Control registers allows the user to mitigate SSN issues without the need of additional external components.

8.3 Power-on reset requirements

In the event of a glitch or data corruption, PCAL9535A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 17](#) and [Figure 18](#).

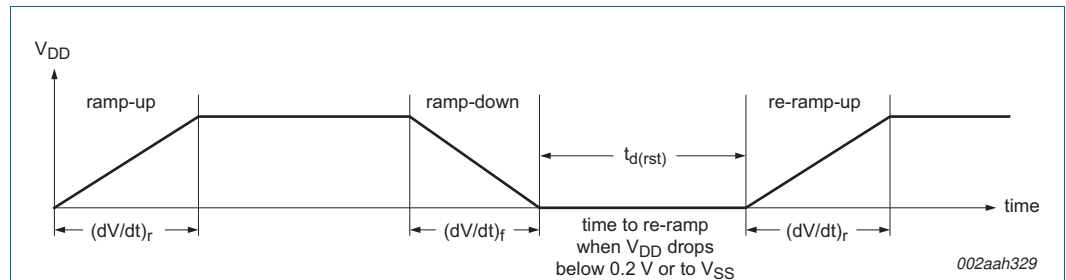


Fig 17. V_{DD} is lowered below 0.2 V or to 0 V and then ramped up to V_{DD}

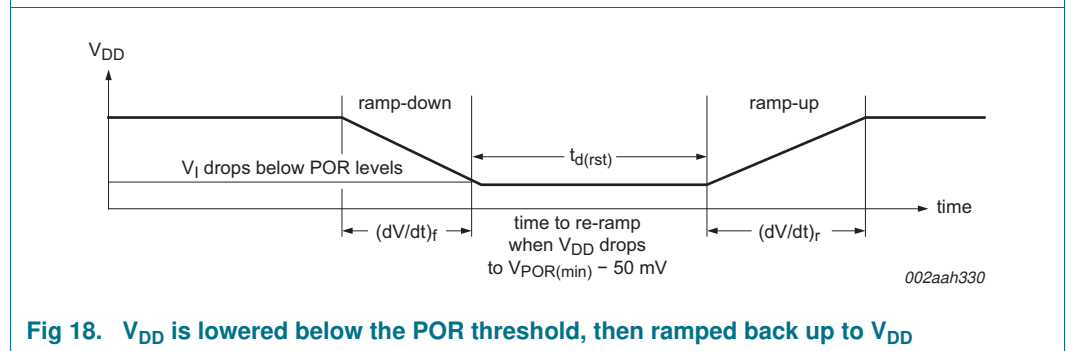


Fig 18. V_{DD} is lowered below the POR threshold, then ramped back up to V_{DD}

[Table 28](#) specifies the performance of the power-on reset feature for PCAL9535A for both types of power-on reset.

Table 28. Recommended supply sequencing and ramp rates
T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
(dV/dt) _f	fall rate of change of voltage	Figure 17	0.1	-	2000	ms
(dV/dt) _r	rise rate of change of voltage	Figure 17	0.1	-	2000	ms
t _{d(rst)}	reset delay time	Figure 17 ; re-ramp time when V _{DD} drops below 0.2 V or to V _{SS}	1	-	-	μs
		Figure 18 ; re-ramp time when V _{DD} drops to V _{POR(min)} - 50 mV	1	-	-	μs
ΔV _{DD(gl)}	glitch supply voltage difference	Figure 19	[1]	-	1	V
t _{w(gl)VDD}	supply voltage glitch pulse width	Figure 19	[2]	-	10	μs
V _{POR(trip)}	power-on reset trip voltage	falling V _{DD}	0.7	-	-	V
		rising V _{DD}	-	-	1.4	V

- [1] Level that V_{DD} can glitch down to with a ramp rate of 0.4 μs/V, but not cause a functional disruption when t_{w(gl)VDD} < 1 μs.
- [2] Glitch width that will not cause a functional disruption when ΔV_{DD(gl)} = 0.5 × V_{DD}.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t_{w(gl)VDD}) and glitch height (ΔV_{DD(gl)}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 19](#) and [Table 28](#) provide more information on how to measure these specifications.

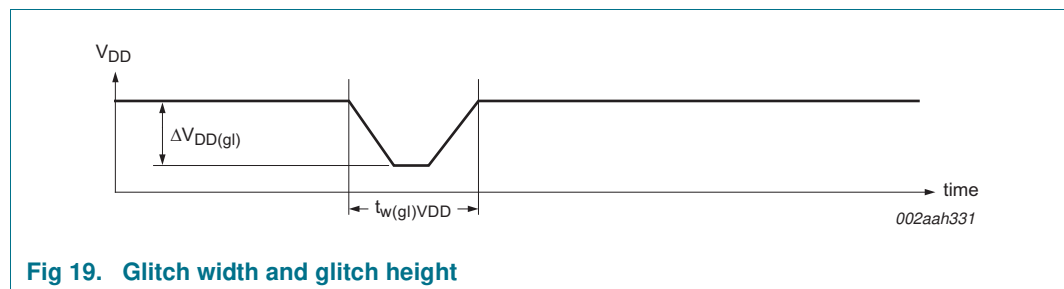


Fig 19. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. [Figure 20](#) and [Table 28](#) provide more details on this specification.

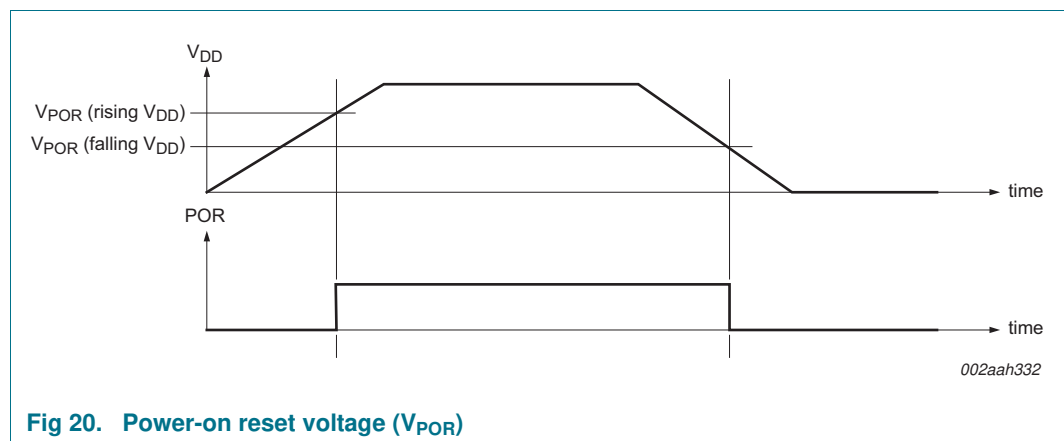


Fig 20. Power-on reset voltage (V_{POR})

8.4 Device current consumption with internal pull-up and pull-down resistors

The PCAL9535A integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails). Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in registers 48h and 49h, while the resistor is connected by the enable registers 46h and 47h. The configuration of the resistors is shown in [Figure 6](#).

If the resistor is configured as a pull-up, that is, connected to V_{DD} , a current will flow from the V_{DD} pin through the resistor to ground when the pin is held LOW. This current will appear as additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, current will flow from the power supply through the pin to the V_{SS} pin. While this current will not be measured as part of I_{DD} , one must be mindful of the 200 mA limiting value through V_{SS} .

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 k Ω with a nominal 100 k Ω value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See [Figure 24](#) for a graph of supply current versus the number of pull-up resistors.

9. Limiting values

Table 29. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+6.5	V
V _I	input voltage		[1] -0.5	+6.5	V
V _O	output voltage		[1] -0.5	+6.5	V
I _{IK}	input clamping current	A0, A1, A2, SCL; V _I < 0 V	-	±20	mA
I _{OK}	output clamping current	$\overline{\text{INT}}$; V _O < 0 V	-	±20	mA
I _{IOK}	input/output clamping current	P port; V _O < 0 V or V _O > V _{DD}	-	±20	mA
		SDA; V _O < 0 V or V _O > V _{DD}	-	±20	mA
I _{OL}	LOW-level output current	continuous; I/O port	-	50	mA
		continuous; SDA, $\overline{\text{INT}}$	-	25	mA
I _{OH}	HIGH-level output current	continuous; P port	-	25	mA
I _{DD}	supply current		-	160	mA
I _{SS}	ground supply current		-	200	mA
P _{tot}	total power dissipation		-	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _{j(max)}	maximum junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

10. Recommended operating conditions

Table 30. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		1.65	5.5	V
V _{IH}	HIGH-level input voltage	SCL, SDA	0.7 × V _{DD}	5.5	V
		A0, A1, A2, P1_7 to P0_0	0.7 × V _{DD}	5.5	V
V _{IL}	LOW-level input voltage	SCL, SDA	-0.5	0.3 × V _{DD}	V
		A0, A1, A2, P1_7 to P0_0	-0.5	0.3 × V _{DD}	V
I _{OH}	HIGH-level output current	P1_7 to P0_0	-	10	mA
I _{OL}	LOW-level output current	P1_7 to P0_0	-	25	mA
T _{amb}	ambient temperature	operating in free air	-40	+85	°C

11. Thermal characteristics

Table 31. Thermal characteristics

Symbol	Parameter	Conditions	Max	Unit
Z _{th(j-a)}	transient thermal impedance from junction to ambient	TSSOP24 package	[1] 88	K/W
		HWQFN24 package	[1] 66	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.