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PCAL9554B; PCAL9554C

Low-voltage 8-bit I²C-bus and SMBus low power I/O port with interrupt, weak pull-up and Agile I/O

Rev. 4 — 19 December 2014 Product data sheet

1. General description

The PCAL9554B and PCAL9554C are a low-voltage 8-bit General Purpose Input/Output (GPIO) expanders with interrupt and weak pull-up for I²C-bus/SMBus applications. The only difference between the PCAL9554B and PCAL9554C is their I²C-bus fixed address, allowing a larger number of the same device on the I²C-bus with no chance of address conflicts. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs, fan control, etc.

In addition to providing a flexible set of GPIOs, the wide V_{DD} range of 1.65 V to 5.5 V allows the PCAL9554B/PCAL9554C to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCAL9554B/PCAL9554C contains the PCA9554A register set of four 8-bit Configuration, Input, Output, and Polarity Inversion registers, and additionally, the PCAL9554B/PCAL9554C has Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

The PCAL9554B is a pin-for-pin replacement for the PCA9554, while the PCAL9554C replaces the PCA9554A, however both versions power-up with all I/O interrupted masked. This mask default allows for a board bring-up free of spurious interrupts at power-up.

The PCAL9554B/PCAL9554C open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCAL9554B or PCAL9554C can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

Three hardware pins (A0, A1, A2) select the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus. The PCAL9554B and PCAL9554C differ only in their base I²C-bus addresses permitting a total of 16 of the same devices on the I²C-bus, minimizing the chance of address conflict, even in the most complex system.

2. Features and benefits

- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 1.5 μA (typical at 5 V V_{DD})
  - 1.0 μA (typical at 3.3 V V_{DD})
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - $V_{hys} = 0.10 \times V_{DD}$ (typical)
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output ($\overline{INT}$)
- 400 kHz Fast-mode I²C-bus
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection exceeds JESD22
  - 2000 V Human Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP16 and HVQFN16

2.1 Agile I/O features

- Pin to pin replacement for PCA9554 and PCA9554B, PCA9554A and PCA9554C with interrupts disabled at power-up
  - Software backward compatible with PCA9554 and PCA9554B, PCA9554A and PCA9554C
- Output port configuration: bank selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pull-up/pull-down enable: floating input or pull-up/down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state

3. Ordering information

Table 1. Ordering information

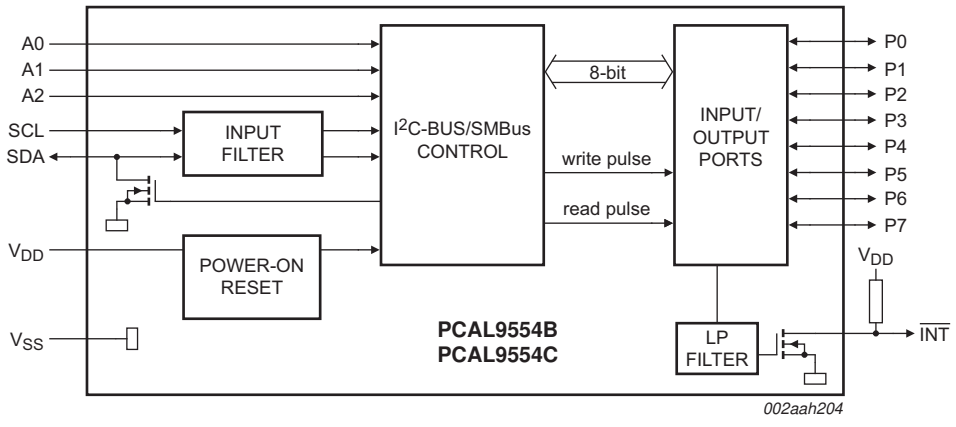
Type number	Topside mark	Package		
		Name	Description	Version
PCAL9554BBS	L4B	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCAL9554BPW	PL9554B	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCAL9554CBS	L4C	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCAL9554CPW	PL9554C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCAL9554BBS	PCAL9554BBSHP	HVQFN16	Reel 13” Q2/T3 *Standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCAL9554BPW	PCAL9554BPWJ	TSSOP16	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCAL9554CBS	PCAL9554CBSHP	HVQFN16	Reel 13” Q2/T3 *Standard mark SMD	6000	T_{amb} = −40 °C to +85 °C
PCAL9554CPW	PCAL9554CPWJ	TSSOP16	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCAL9554B/PCAL9554C

5. Pinning information

5.1 Pinning

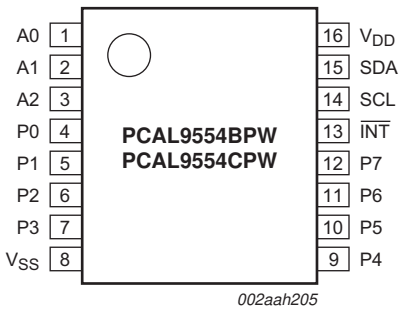


Fig 2. Pin configuration for TSSOP16

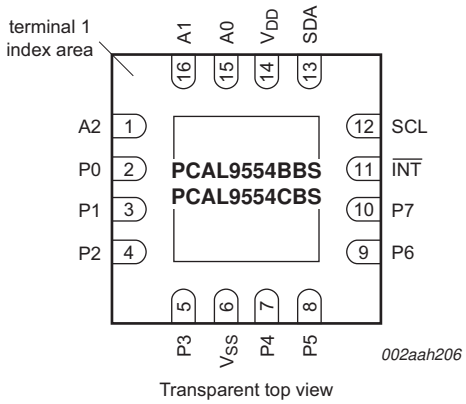


Fig 3. Pin configuration for HVQFN16

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP16	HVQFN16	
A0	1	15	address input 0
A1	2	16	address input 1
A2	3	1	address input 2
P0[1]	4	2	Port P input/output 0
P1[1]	5	3	Port P input/output 1
P2[1]	6	4	Port P input/output 2
P3[1]	7	5	Port P input/output 3
V_{SS}	8	6[2]	supply ground
P4[1]	9	7	Port P input/output 4
P5[1]	10	8	Port P input/output 5
P6[1]	11	9	Port P input/output 6
P7[1]	12	10	Port P input/output 7
$\overline{INT}$	13	11	interrupt output (open-drain)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V_{DD}	16	14	supply voltage

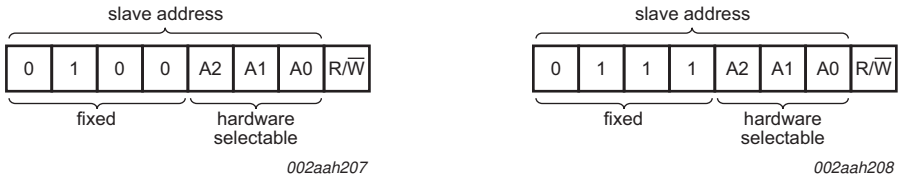
[1] All I/O are configured as input at power-on.

[2] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6. Functional description

Refer to Figure 1 “Block diagram of PCAL9554B/PCAL9554C”.

6.1 Device address



a. PCAL9554B address

b. PCAL9554C address

Fig 4. Device address

A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

6.2 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCAL9554B/PCAL9554C. Two bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. Bit 6 in conjunction with the lower three bits of the Command byte are used to point to the extended features of the device (Agile I/O). This register is write only.

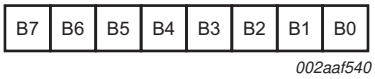


Fig 5. Pointer register bits

Table 4. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Output port	read/write byte	1111 1111
0	0	0	0	0	0	1	0	02h	Polarity Inversion	read/write byte	0000 0000
0	0	0	0	0	0	1	1	03h	Configuration	read/write byte	1111 1111
0	1	0	0	0	0	0	0	40h	Output drive strength 0	read/write byte	1111 1111
0	1	0	0	0	0	0	1	41h	Output drive strength 1	read/write byte	1111 1111
0	1	0	0	0	0	1	0	42h	Input latch	read/write byte	0000 0000
0	1	0	0	0	0	1	1	43h	Pull-up/pull-down enable	read/write byte	1111 1111
0	1	0	0	0	1	0	0	44h	Pull-up/pull-down selection	read/write byte	1111 1111
0	1	0	0	0	1	0	1	45h	Interrupt mask	read/write byte	1111 1111
0	1	0	0	0	1	1	0	46h	Interrupt status	read byte	0000 0000
0	1	0	0	1	1	1	1	4Fh	Output port configuration	read/write byte	0000 0000

[1] Undefined.

6.3 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C-bus slave address	L	H	L/H	L/H	A2	A1	A0	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

6.4 Register descriptions

6.4.1 Input port register (00h)

The Input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port register is read only; writes to this register have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 7.2 "Read commands".

Table 6. Input port register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

6.4.2 Output port register (01h)

The Output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from this register reflect the value that was written to this register, **not** the actual pin value.

Table 7. Output port register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

6.4.3 Polarity inversion register (02h)

The Polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Table 8. Polarity inversion register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

6.4.4 Configuration register (03h)

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 9. Configuration register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

6.4.5 Output drive strength registers (40h, 41h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example, Port 7 is controlled by register 41 CC7 (bits [7:6]), Port 6 is controlled by register 41 CC6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See Section 8.2 "Output drive strength control" for more details.

Table 10. Current control register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC3		CC2		CC1		CC0	
Default	1	1	1	1	1	1	1	1

Table 11. Current control register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC7		CC6		CC5		CC4	
Default	1	1	1	1	1	1	1	1

6.4.6 Input latch register (42h)

The Input latch register enables and disables the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input port register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 11. For example, if the P4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port register will read '1'. The next read of the input port register bit 4 should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input port register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input port register reflects the latched logic level.

Table 12. Input latch register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	L7	L6	L5	L4	L3	L2	L1	L0
Default	0	0	0	0	0	0	0	0

6.4.7 Pull-up/pull-down enable register (43h)

This register allows the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 6.4.11). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor.

Table 13. Pull-up/pull-down enable register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	1	1	1	1	1	1	1	1

The default value enables pull-up resistors on all I/O pins to match with the non-Agile I/O devices PCA9554B and PCA9554C.

6.4.8 Pull-up/pull-down selection register (44h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ.

Table 14. Pull-up/pull-down selection register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD7	PUD6	PUD5	PUD4	PUD3	PUD2	PUD1	PUD0
Default	1	1	1	1	1	1	1	1

6.4.9 Interrupt mask register (45h)

Interrupt mask register is set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin ($\overline{INT}$) will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted.

Table 15. Interrupt mask register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	M7	M6	M5	M4	M3	M2	M1	M0
Default	1	1	1	1	1	1	1	1

6.4.10 Interrupt status register (46h)

This read-only register is used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0.

Table 16. Interrupt status register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	S7	S6	S5	S4	S3	S2	S1	S0
Default	0	0	0	0	0	0	0	0

6.4.11 Output port configuration register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 6). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active). The recommended command sequence is to program this register (4Fh) before the Configuration register (03h) sets the port pins as outputs.

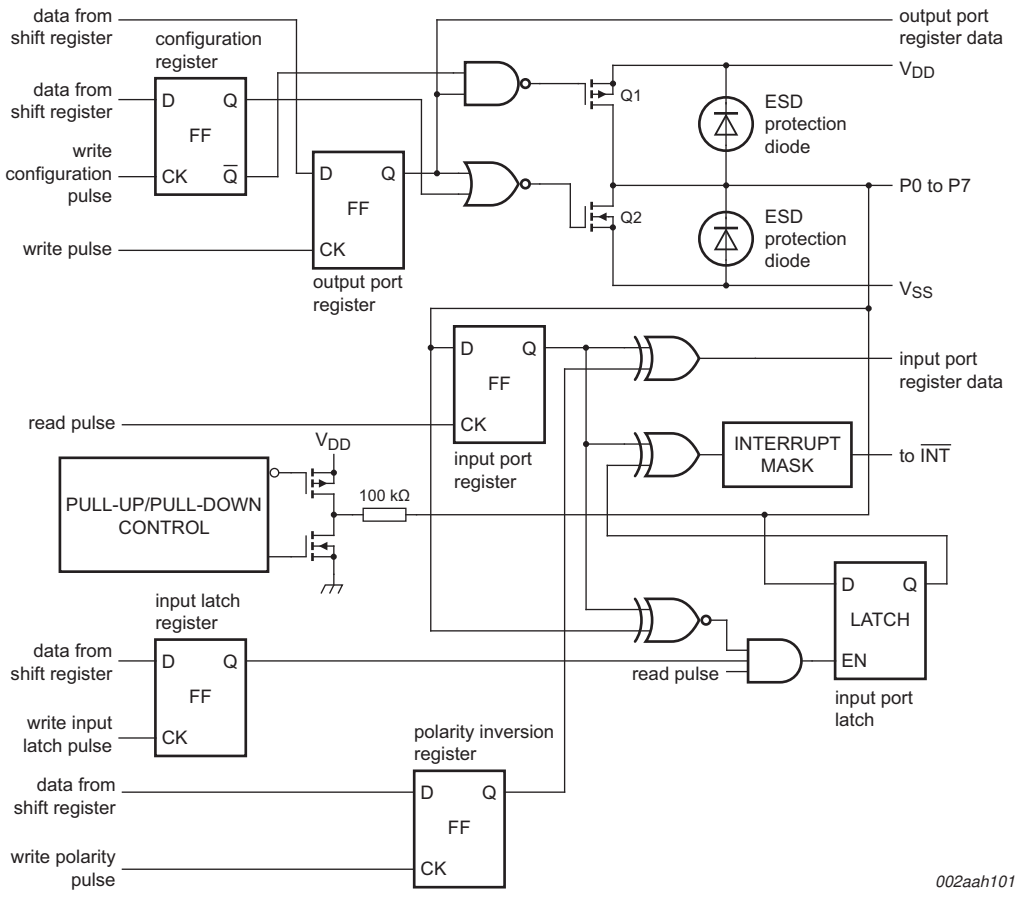
Table 17. Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							ODEN0
Default	0	0	0	0	0	0	0	0

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{DD} or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig 6. Simplified schematic of the I/Os (P0 to P7)

6.6 Power-on reset

When power (from 0 V) is applied to V_{DD}, an internal power-on reset holds the PCAL9554B/PCAL9554C in a reset condition until V_{DD} has reached V_{POR}. At that time, the reset condition is released and the PCAL9554B/PCAL9554C registers and I²C-bus/SMBus state machine initialize to their default states. After that, V_{DD} must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. See Section 8.4 “Power-on reset requirements”.

6.7 Interrupt output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt (see Figure 10). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input port register.

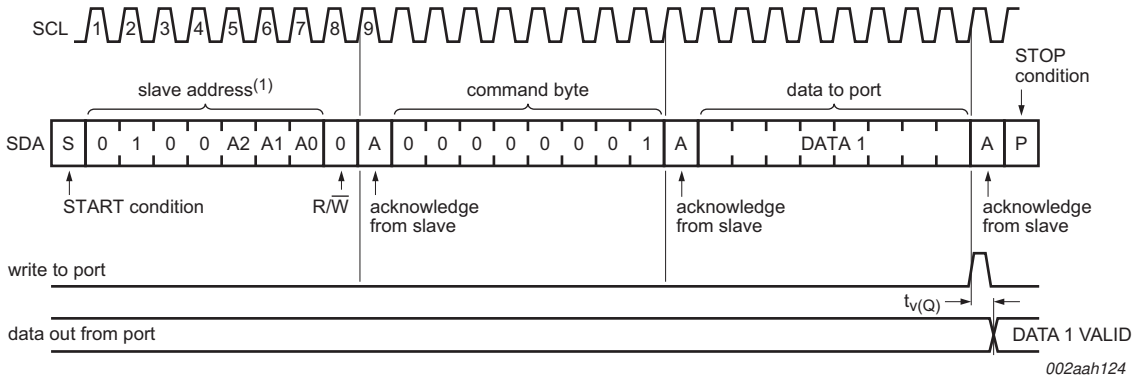
The $\overline{INT}$ output has an open-drain structure and requires a pull-up resistor to V_{DD}. $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information. When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

7. Bus transactions

The PCAL9554B/PCAL9554C is an I²C-bus slave device. Data is exchanged between the master and PCAL9554B/PCAL9554C through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

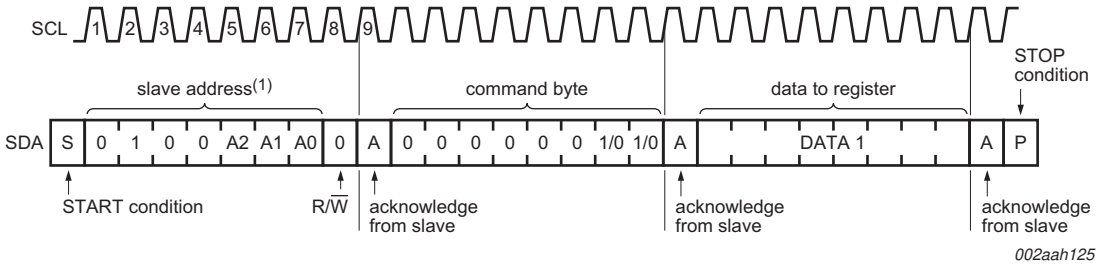
7.1 Write commands

Data is transmitted to the PCAL9554B/PCAL9554C by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.



(1) PCAL9554B address shown. Address for PCAL9554C is 0111,A2,A1,A0.

Fig 7. Write to Output port register



(1) PCAL9554B address shown. Address for PCAL9554C is 0111,A2,A1,A0.

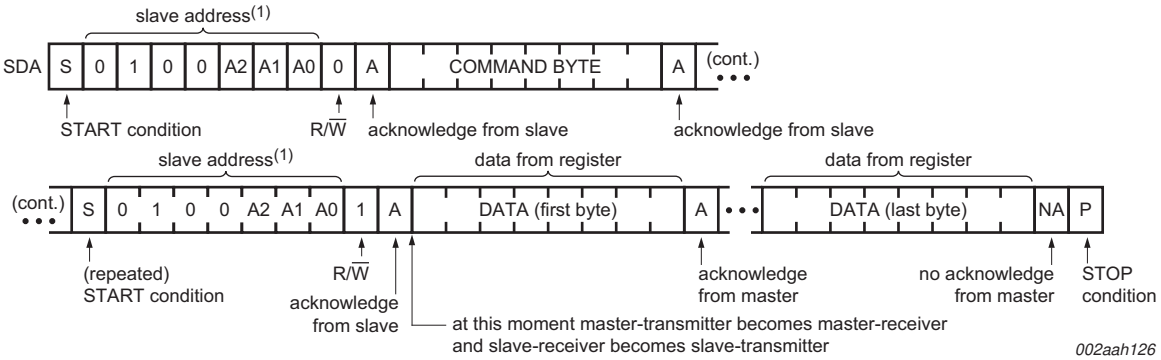
Fig 8. Write to Configuration or Polarity inversion registers

7.2 Read commands

To read data from the PCAL9554B/PCAL9554C, the bus master must first send the PCAL9554B/PCAL9554C address with the least significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is to be accessed.

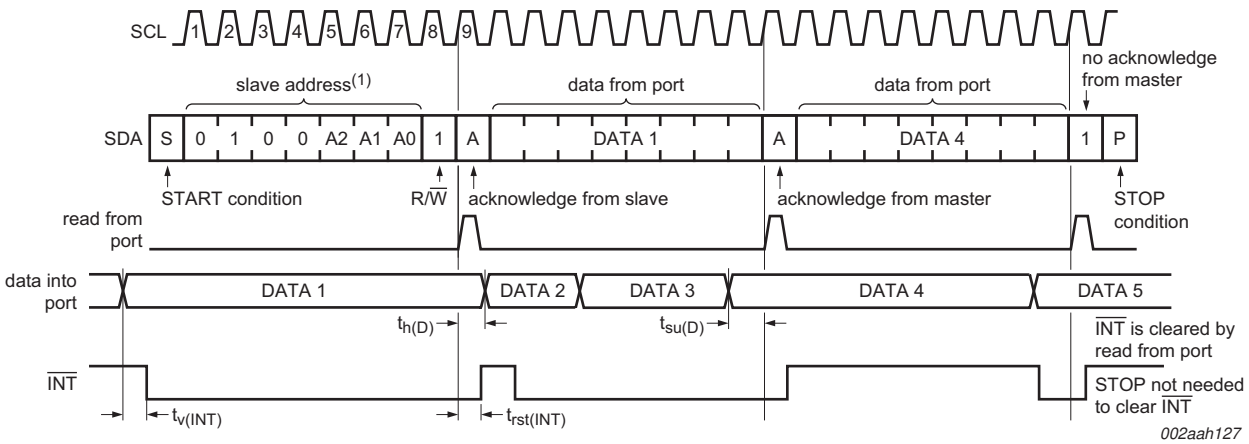
After a restart the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCAL9554B/PCAL9554C (see Figure 9 and Figure 10).

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.



(1) PCAL9554B address shown. Address for PCAL9554C is 0111,A2,A1,A0.

Fig 9. Read from register

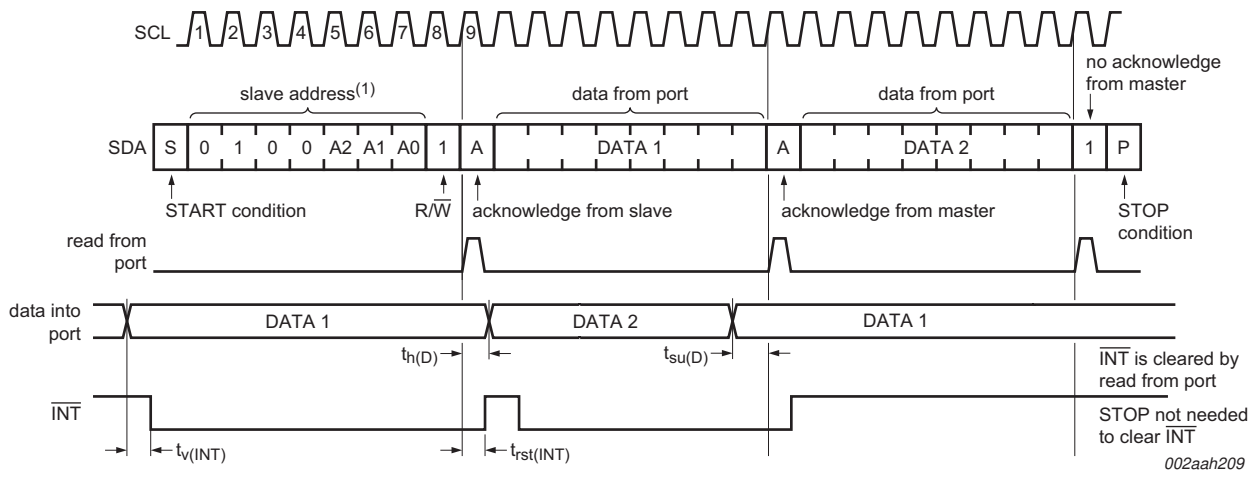


Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 9).

(1) PCAL9554B address shown. Address for PCAL9554C is 0111,A2,A1,A0.

Fig 10. Read Input port register (non-latched)



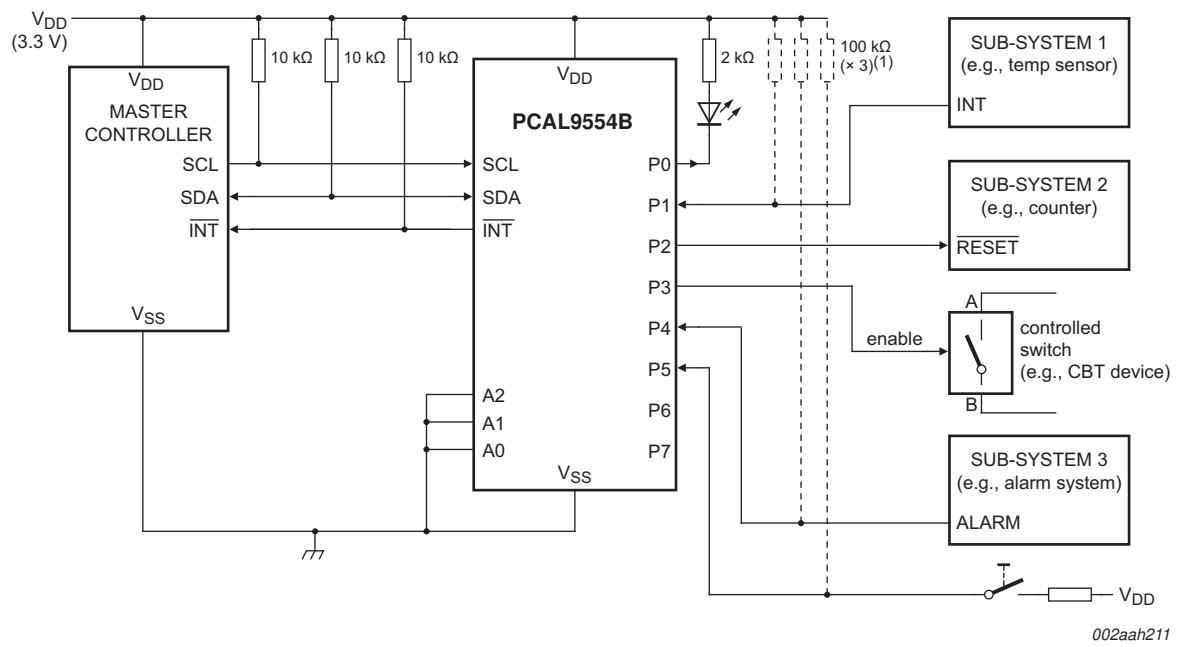
Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 9).

(1) PCAL9554B address shown. Address for PCAL9554C is 0111,A2,A1,A0.

Fig 11. Read Input port register (latch enabled)

8. Application design-in information



Device address is 0100 000x for this example using PCAL9554B (address for PCAL9554C is 0111 000x).

P0, P2, P3 configured as outputs.

P1, P4, P5 configured as inputs.

P6, P7 are not used and need 100 kΩ pull-up resistors to protect them from floating or the internal pull-up or pull-down selected.

(1) No resistors are required for inputs (on P port) that may float due to the weak pull-up integrated into the device.

Fig 12. Typical application

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 12. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 13 shows a high value resistor in parallel with the LED, which is not needed with the PCAL9554B or PCAL9554C that integrate a weak pull-up resistor on all pins. Figure 14 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

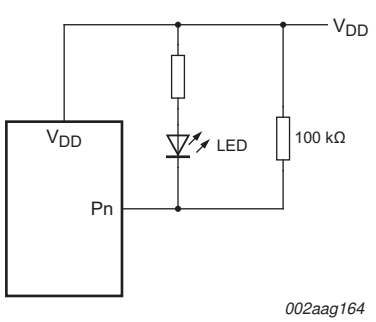


Fig 13. High value resistor in parallel with the LED

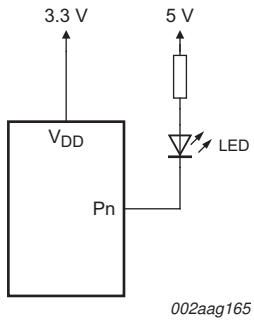


Fig 14. Device supplied by a lower voltage

8.2 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 15 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 10b, then only two of the fingers are active, reducing the current drive capability by 50 %.

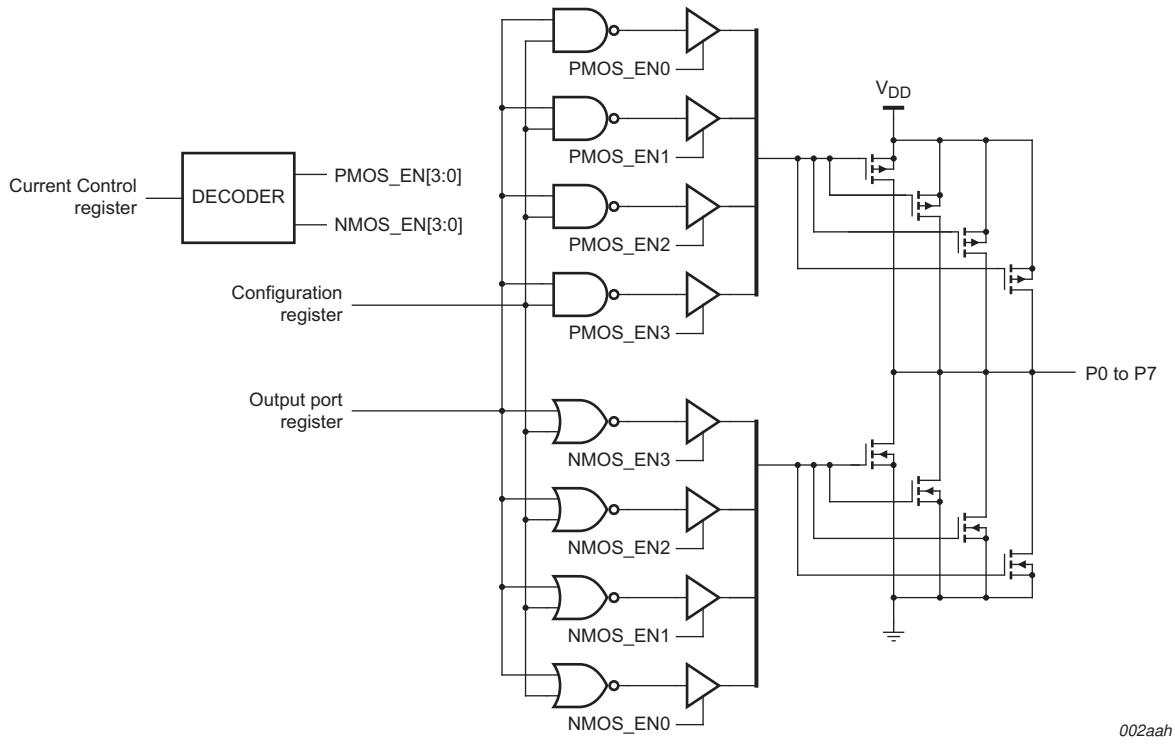


Fig 15. Simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Current Control registers allows the user to mitigate SSN issues without the need of additional external components.

8.3 12 V tolerant I/Os

The PCAL9554B/PCAL9554C device SCR group reference diode can go up to 10 V before latch back to 8 V. The ESD gate oxide will protect the device, but not if used continually. Therefore, to achieve 12 V tolerant I/Os, the external protection circuitry (diode) must be used as shown in Figure 16.

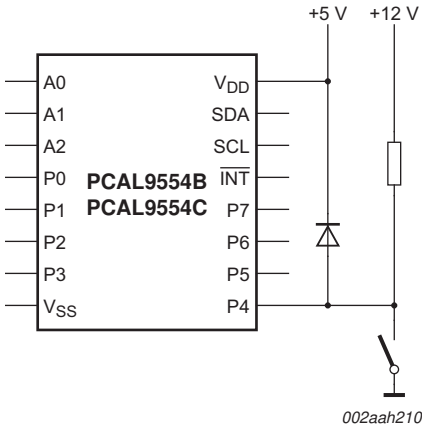


Fig 16. External protection circuitry

8.4 Power-on reset requirements

In the event of a glitch or data corruption, PCAL9554B/PCAL9554C can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 17 and Figure 18.

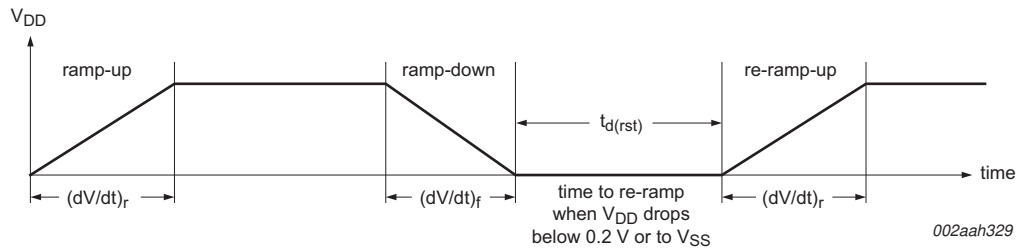


Fig 17. V_{DD} is lowered below 0.2 V or 0 V and then ramped up to V_{DD}

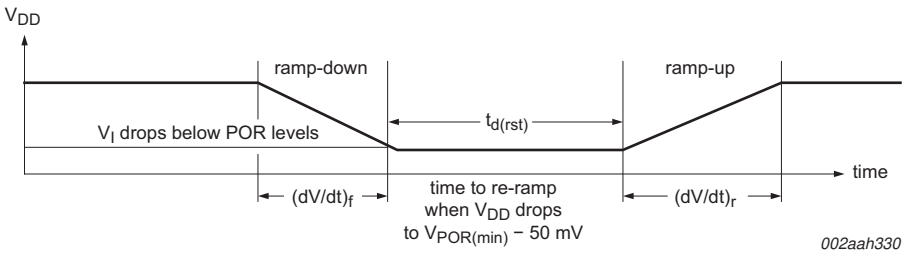


Fig 18. V_{DD} is lowered below the POR threshold, then ramped back up to V_{DD}

Table 18 specifies the performance of the power-on reset feature for PCAL9554B/PCAL9554C for both types of power-on reset.

Table 18. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 17		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 17		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 17; re-ramp time when V_{DD} drops to V_{SS}		1	-	-	µs
		Figure 18; re-ramp time when V_{DD} drops to $V_{POR(min)}$ − 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 19	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 19	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling V_{DD}		0.7	-	-	V
		rising V_{DD}		-	-	1.4	V

[1] Level that V_{DD} can glitch down to with a ramp rate of 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 19 and Table 18 provide more information on how to measure these specifications.

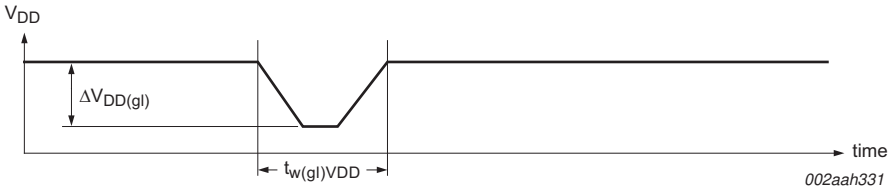


Fig 19. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 20 and Table 18 provide more details on this specification.

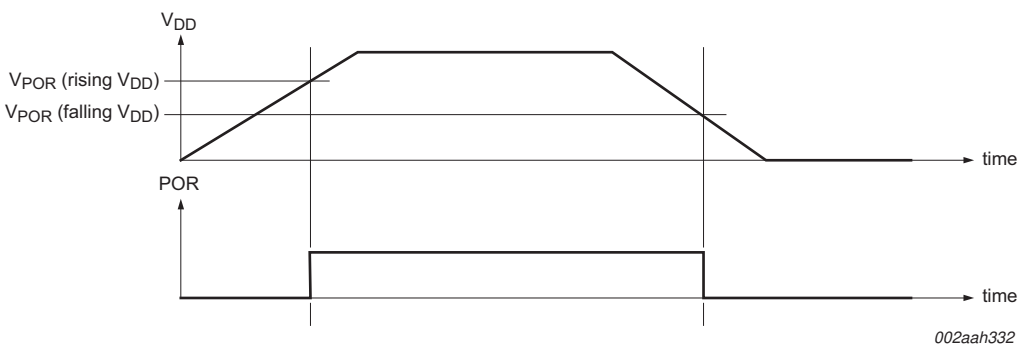


Fig 20. Power-on reset voltage (V_{POR})

8.5 Device current consumption with internal pull-up and pull-down resistors

The PCAL9554B; PCAL9554C integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails. Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in register 44h, while the resistor is connected by the enable register 43h. The configuration of the resistors is shown in Figure 6.

If the resistor is configured as a pull-up, that is, connected to V_{DD}, a current will flow from the V_{DD} pin through the resistor to ground when the pin is held LOW. This current will appear as additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, current will flow from the power supply through the pin to the V_{SS} pin. While this current will not be measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See Figure 24 for a graph of supply current versus the number of pull-up resistors.

9. Limiting values

Table 19. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.5	V
V_I	input voltage		[1]	−0.5	+6.5	V
V_O	output voltage		[1]	−0.5	+6.5	V
I_{IK}	input clamping current	A0, A1, A2, SCL; $V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD}$		-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD}$		-	±20	mA
I_{OL}	LOW-level output current	continuous; I/O port		-	50	mA
		continuous; SDA, $\overline{INT}$		-	25	mA
I_{OH}	HIGH-level output current	continuous; P port		-	25	mA
I_{DD}	supply current			-	160	mA
I_{SS}	ground supply current			-	200	mA
P_{tot}	total power dissipation			-	200	mW
T_{stg}	storage temperature			−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

10. Recommended operating conditions

Table 20. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA	$0.7 \times V_{DD}$	5.5	V
		A0, A1, A2, P port	$0.7 \times V_{DD}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{DD}$	V
		A0, A1, A2, P port	−0.5	$0.3 \times V_{DD}$	V
I_{OH}	HIGH-level output current	P port	-	10	mA
I_{OL}	LOW-level output current	P port	-	25	mA
T_{amb}	ambient temperature	operating in free air	−40	+85	°C

11. Thermal characteristics

Table 21. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	HVQFN16 package	[1]	53	K/W
		TSSOP16 package	[1]	108	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

12. Static characteristics

Table 22. Static characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA	−1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD}$ or V_{SS}; I_O = 0 mA	-	1.1	1.4	V
V_{OH}	HIGH-level output voltage[2]	P port; I_{OH} = −8 mA; CCX = 11b				
		V_{DD} = 1.65 V	1.2	-	-	V
		V_{DD} = 2.3 V	1.8	-	-	V
		V_{DD} = 3 V	2.6	-	-	V
		V_{DD} = 4.5 V	4.1	-	-	V
		P port; I_{OH} = −2.5 mA and CCX = 00b; I_{OH} = −5 mA and CCX = 01b; I_{OH} = −7.5 mA and CCX = 10b; I_{OH} = −10 mA and CCX = 11b				
		V_{DD} = 1.65 V	1.1	-	-	V
		V_{DD} = 2.3 V	1.7	-	-	V
		V_{DD} = 3 V	2.5	-	-	V
		V_{DD} = 4.5 V	4.0	-	-	V
V_{OL}	LOW-level output voltage[2]	P port; I_{OL} = 8 mA; CCX = 11b				
		V_{DD} = 1.65 V	-	-	0.45	V
		V_{DD} = 2.3 V	-	-	0.25	V
		V_{DD} = 3 V	-	-	0.25	V
		V_{DD} = 4.5 V	-	-	0.2	V
		P port; I_{OL} = 2.5 mA and CCX = 00b; I_{OL} = 5 mA and CCX = 01b; I_{OL} = 7.5 mA and CCX = 10b; I_{OL} = 10 mA and CCX = 11b				
		V_{DD} = 1.65 V	-	-	0.5	V
		V_{DD} = 2.3 V	-	-	0.3	V
		V_{DD} = 3 V	-	-	0.25	V
		V_{DD} = 4.5 V	-	-	0.2	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 1.65 V to 5.5 V				
		SDA	3	-	-	mA
		$\overline{INT}$	3	15[3]	-	mA
I_I	input current	V_{DD} = 1.65 V to 5.5 V				
		SCL, SDA; $V_I = V_{DD}$ or V_{SS}	-	-	0.1	µA
		A0, A1, A2; $V_I = V_{DD}$ or V_{SS}	-	-	±1	µA
I_{IH}	HIGH-level input current	P port; $V_I = V_{DD}$; V_{DD} = 1.65 V to 5.5 V	-	-	1	µA
I_{IL}	LOW-level input current	P port; $V_I = V_{SS}$; V_{DD} = 1.65 V to 5.5 V	-	-	1	µA

Table 22. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	SDA, P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	10	25	µA
		V_{DD} = 2.3 V to 3.6 V	-	6.5	15	µA
		V_{DD} = 1.65 V to 2.3 V	-	4	9	µA
		SCL, SDA, P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	1.5	7	µA
		V_{DD} = 2.3 V to 3.6 V	-	1	3.2	µA
		V_{DD} = 1.65 V to 2.3 V	-	0.5	1.7	µA
		Active mode; P port, A0, A1, A2; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz, continuous register read				
		V_{DD} = 3.6 V to 5.5 V	-	60	125	µA
		V_{DD} = 2.3 V to 3.6 V	-	40	75	µA
		V_{DD} = 1.65 V to 2.3 V	-	20	45	µA
		with pull-ups enabled; P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port = V_{SS}; V_I on A0, A1, A2 = V_{DD} or V_{SS}; I_O = 0 mA; I/O = inputs with pull-up enabled; f_{SCL} = 0 kHz				
		V_{DD} = 1.65 V to 5.5 V	-	0.55	0.75	mA
ΔI_{DD}	additional quiescent supply current	SCL, SDA; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	25	µA
		P port, A0, A1; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	80	µA
C_i	input capacitance	V_I = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	6	7	pF
C_{io}	input/output capacitance	SDA, SCL; $V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7	8	pF
		P port; $V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7.5	8.5	pF
$R_{pu(int)}$	internal pull-up resistance	input/output	50	100	150	kΩ
$R_{pd(int)}$	internal pull-down resistance	input/output	50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at V_{DD} = 3.3 V and T_{amb} = 25 °C.

[2] The total current sourced by all I/Os must be limited to 160 mA, and total current sunk by all I/Os must be limited to 200 mA.

[3] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{DD} = 3.3 V. Typical value for V_{DD} < 2.5 V, V_{OL} = 0.6 V.

12.1 Typical characteristics

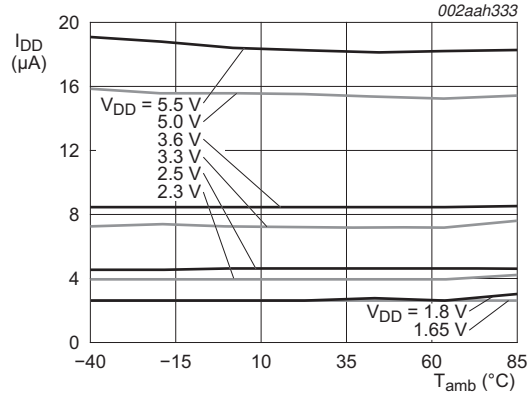


Fig 21. Supply current versus ambient temperature

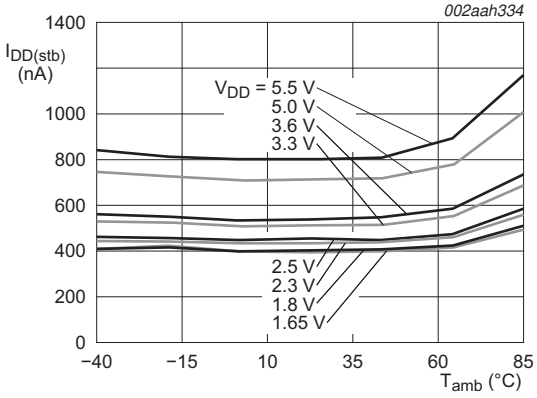


Fig 22. Standby supply current versus ambient temperature

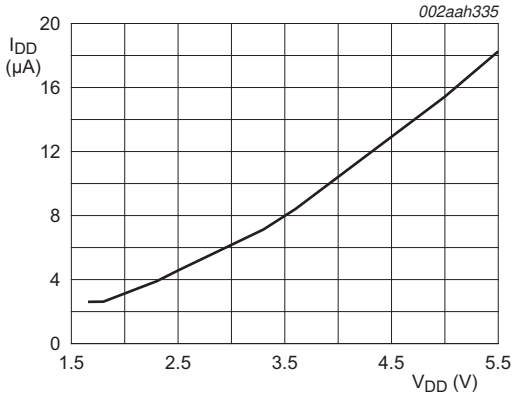


Fig 23. Supply current versus supply voltage

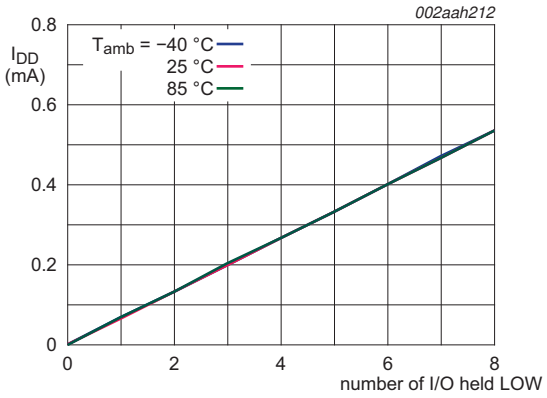
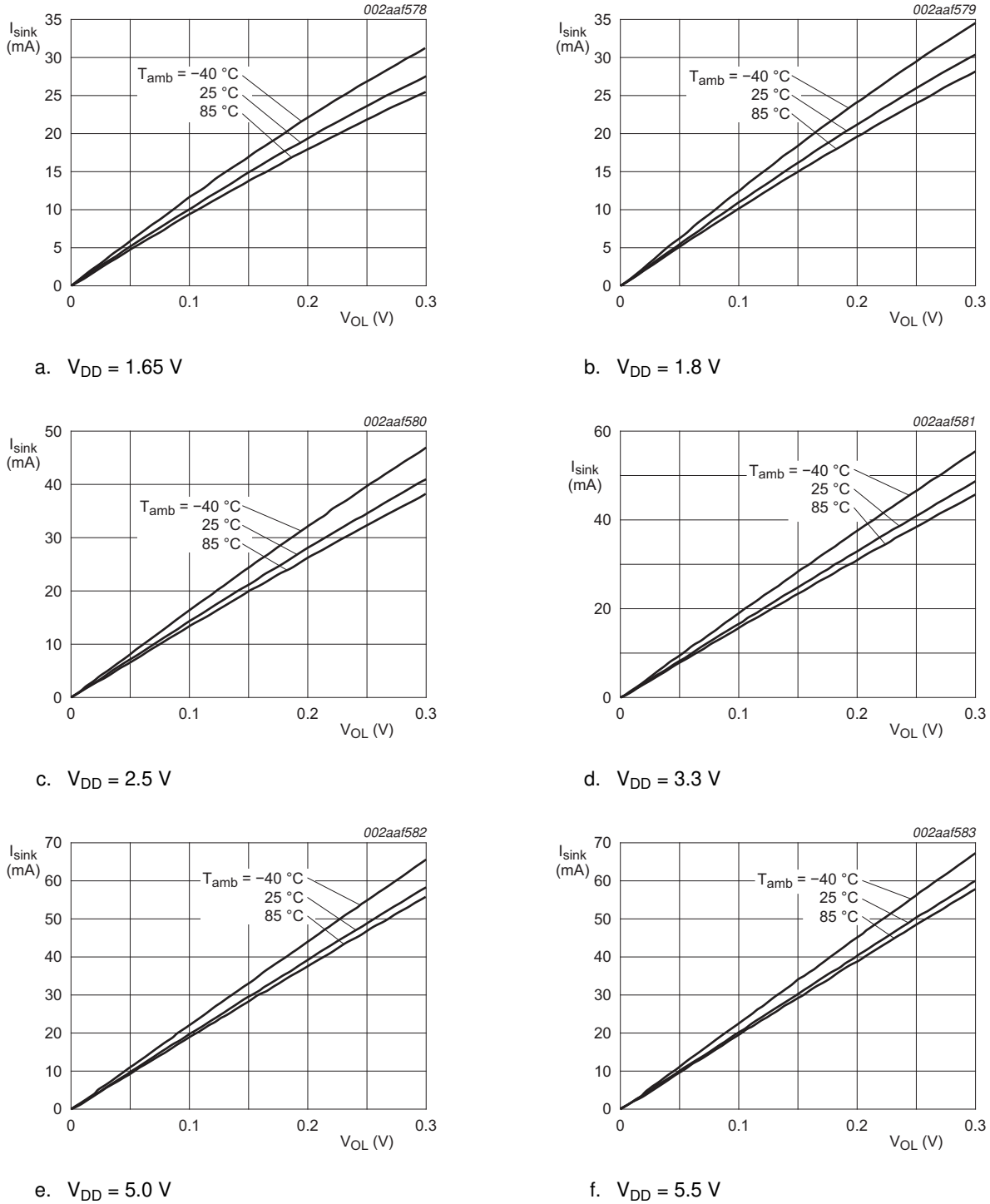


Fig 24. Supply current versus number of I/O held LOW



a. V_{DD} = 1.65 V

b. V_{DD} = 1.8 V

c. V_{DD} = 2.5 V

d. V_{DD} = 3.3 V

e. V_{DD} = 5.0 V

f. V_{DD} = 5.5 V

Fig 25. I/O sink current versus LOW-level output voltage with CCX.X = 11b