Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

mess • electronic

PICOCAP®

Data Sheet

PCapØ1

Single-chip Solution for Capacitance Measurement with Standard Firmware 03.01.02

July 15th , 2013

Document-No: DB_PCapØ1-0301_en V0.6

Published by acam-messelectronic gmbh

Legal note

The present manual (data sheet and guide) is still under development, which may result in corrections, modifications or additions. acam cannot be held liable for any of its contents, neither for accuracy, nor for completeness. The compiled information is believed correct, though some errors and omissions are likely. We welcome any notification, which will be integrated in succeeding releases.
The acam recommendations are believed useful, the firmware proposals and the schematics operable, nevertheless it is of the customer's sole responsibility to modify, test and validate them before setting up any production process.
acam products are not designed for use in medical, nuclear, military, aircraft, spacecraft or lifesupport devices. Nor are they suitable for applications where failure may provoke injury to people or heavy material damage. acam declines any liability with respect to such non-intended use, which remains under the customer's sole responsibility and risk. Military, spatial and nuclear use subject to German export regulations.
acam do not warrant, and it is not implied that the information and/or practice presented here is free from patent, copyright or similar protection. All registered names and trademarks are mentioned for reference only and remain the property of their respective owners. The acam logo and the PicoCap logo are registered trademarks of acam-messelectronic gmbh, Germany.

Support / Contact

For a complete listing of Direct Sales, Distributor and Sales Representative contacts, visit the acam web site at:

http://www.acam.de/sales/distributors/

For technical support you can contact the acam support team in the headquarters in Germany or the Distributor in your country. The contact details of acam in Germany are:

support@acam.de or by phone +49-7244-74190.

Content

1 System Overview

PCapØ1 is a dedicated Capacitance-to-Digital Conversion Digital Signal Processor. Its front end is based on acam's patented PICOCAP® principle. This conversion principle offers high resolution at conversion times as short as 2 µs. Customers benefit from outstanding flexibility for optimizing power consumption, resolution and speed.

The PCap01A can be used for grounded single and differential sensors as well as for floating single and differential sensors. With grounded capacitors the stray capacitance inside the chip will be compensated. With floating capacitors, further to the internal stray capacitance, the external stray capacitances as well get compensated. Additionally, the temperature can be measured by means of internal thermistors or external ones (platinum or others). Before loading some firmware to it, the chip is not completely operable. Data will end up in ALU instead of being transferred to processor and/or output. Under this circumstance, we chose to write a combined data sheet covering the hardware aspects as well as handling a very basic firmware called 03.01.xx; this basic or "standard" firmware calculates the capacitance and resistance ratios and transfers them to the data output ports, still without doing such further possible processing like filtering and linearization. It is provided free of charge with the chip, yet, it needs to be loaded via SPI or I2C.

For clarity, those aspects that are **standard-firmware related** have been marked with a **blue stripe in the margin**. User-written firmware may behave differently here.

Firmware Related

1.1 Features

- Digital measuring principle in CMOS technology
- Up to 8 capacitances in grounded mode
- Up to 4 capacitances in floating mode (potential- free and with zero bias voltage)
- Compensation of internal (grounded) and external parasitic capacities (floating)
- High resolution: up to 6 aF at 5 Hz and 10 pF base capacitance, or 17 bit resolution at 5 Hz with 100 pF base capacitance and 10 pF excitation
- High measurement rate: up to 500 kHz
- Extremely low current consumption possible:
  Down to 4 µA at 3 Hz with 13.4 bit resolution
- High stability with temperature, low offset drift (down to 30 aF per Kelvin), low gain drift when all compensation options are activated.

- Dedicated ports for precision temperature measurement (with Pt1000 sensors, the resolution is 0.005 K)
- Serial interfaces (SPI or I2C compatible)
- Self-boot capability
- Single power supply (2.1 to 3.6 V)
- No need for a clock
- RISC processor core using Harvard architecture:
  - 48 x 48 bit RAM Data
  - 4k x 8 bit volatile program memory for high-speed operation (40 to 100 MHz)
  - 4k x 8 bit non-volatile (OTP) program memory for normal speed operation (up to 40 MHz)

1.2 Applications

- Humidity sensors
- Position sensors
- Pressure sensors
- Force sensors
- Acceleration sensors
- Inclination sensors
- Tilt sensors
- Angle sensors
- Wireless applications
- Level sensors
- Microphones
- MEMS sensors

1.3 Block diagram

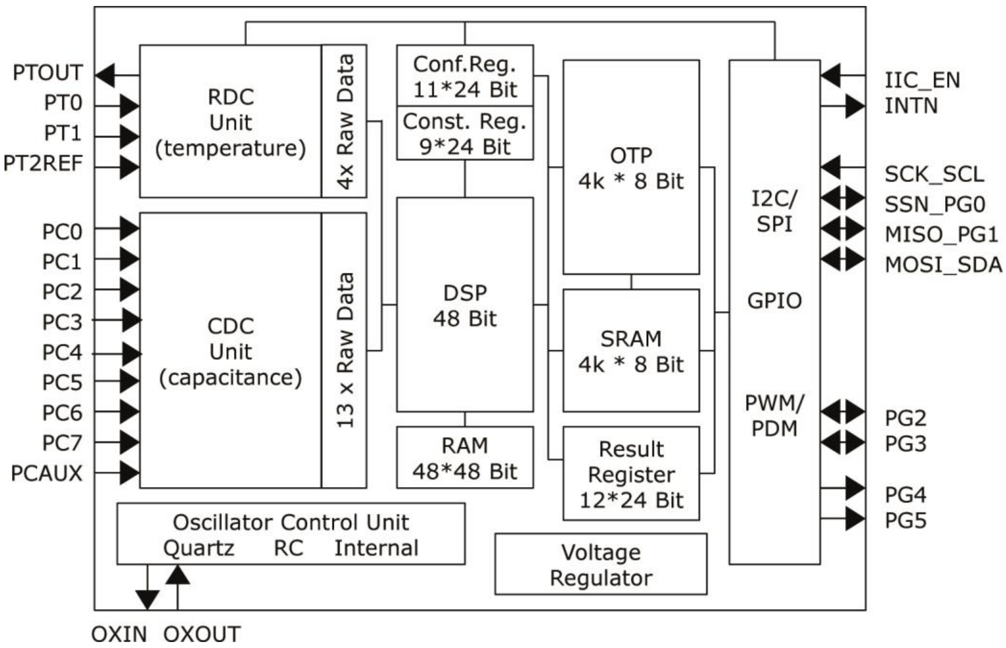


Figure 1-1: Block Diagram

1.4 Part Numbers

Ref.	Package	Name	Conditioning	MOQ
1613	-Dice-	PCap01A	Waffle Pack	100
1793	QFN32	PCap01AD	Tape-on-reel	500
1795	QFN24	PCap01AK	Tape-on-reel	500

Sample policy. Single Laboratory samples of packaged chips are available; concerning dice, however, MOQ applies.

2 Characteristics & Specifications

2.1 Electrical Characteristics

2.1.1 Absolute Maximum Ratings

Supply voltage V_{DD}-to-GND	- 0.3 to 4.0 V
Storage temperature Tstg	- 55 to 150 °C
ESD rating (HBM), each pin	> 2 kV
Junction temperature (Tj)	max. 125 °C
OTP Data Retention Period	10 years at 95 °C temperature

2.1.2 Recommended Operating Conditions

Table 2-1: Operating conditions

Quantity	Symbol	Remarks	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		2.1		3.6	V
Digital port voltage	$V_{io\_digital}$	Relative to ground	– 0.6	3.3	V_{DD} +0.6 ≤ 3.6	V
Digital ports switching level		HIGH ♑ LOW LOW ♑ HIGH		0.3 * V_{DD} 0.7 * V_{DD}		
Analog port voltage	V_{io_analog}		- 0.6		V_{DD} +0.6 ≤ 3.6	V
OTP Programming voltage	V_{OTP}	Between "VPP_OTP" port and ground.		6.5	7.0	V
SPI bus frequency	$f_{SPI\text{-}bus}$	Clock frequency for the 4-wire SPI bus operation	0		20	MHz
Buffer strength		e.g. for the MISO line			2.5	mA
I2C bus frequency		Speed (data rate) of the 2-wire I2C bus operation	0	100		kHz
OTP Bit hold time		Bit hold time for OTP write	30		500	µs
GPIO input rise time		Rise time of the input signal put to general-purpose I/O			t.b.d	ns
GPIO output rise time		Rise time of the output signal from a general-purpose I/O			t.b.d.	ns
CDC discharge time		MR1	0		40	µs
RDC discharge time			0		100	µs
Junction Temperature	T_j	Junction temperature must not exceed +125 °C	- 40		+ 125	°C
Ambient Temperature	T_a	At VDD = 2.4V -/+ 0.3V	- 40		+ 125	°C

Overclocking the I2C bus is technically possible but within the sole responsibility of the customer (a license may be necessary).

2.2 CDC Precision

2.2.1 RMS Noise and Resolution vs. Output Data Rate

Table 2-2 Typical Capacitive Noise & Resolution vs. Output Data Rate, 10 pF Base + 1 pF Span, fast settle, V = 3.0 V

Output Data Rate [Hz]	FLOATING Fully compensated			GROUNDED Internally compensated		
	RMS Noise [aF]	Eff. Resolution 10 pF base [Bits]	Eff. Resolution 1 pF span [Bits]	RMS Noise [aF]	Eff. Resolution 10 pF base [Bits]	Eff. Resolution 1 pF span [Bits]
5	6	20.7	17.3	6	20.7	17.3
10	13	19.6	16.2	11	19.8	16.5
25	20	18.9	15.6	17	19.2	15.8
100	39	18.0	14.6	22	18.8	15.5
250	72	17.1	13.8	29	18.4	15.1
1,000	157	16.0	12.6	66	17.2	13.9
3,500	290	15.1	11.8	139	16.1	12.8
7,000	420	14.5	11.2	176	15.8	12.5
10,000	495	14.3	11.0	246	15.3	12.0

Root mean-square (RMS) noise in aF as a function of output data rate in Hz, measured at 3.0 V supply voltage using the maximum possible sample size for in-chip averaging at the minimum possible cycle time. Bit values are calculated as a binary logarithm of noise (in attofarad) over the base and excitation capacitance values. The measurements have been done with the PCap01 evaluation board, with fixed COG ceramic capacitors.

Both, sensor and reference are connected “floating” or “grounded”, as indicated. When floating, compensation mechanisms for both internal and external stray capacitance are activated; when grounded, internal only.

Table 2-3 Typical Capacitive Noise & Resolution vs. Output Data Rate, 33 pF Base + 3.3 pF Span, fast settle, V = 3.0 V

Output Data Rate [Hz]	FLOATING Fully compensated			GROUNDED Internally compensated		
	RMS Noise [aF]	Eff. Resolution 33 pF base [Bits]	Eff. Resolution 3.3 pF span [Bits]	RMS Noise [aF]	Eff. Resolution 33 pF base [Bits]	Eff. Resolution 3.3 pF span [Bits]
5	18	20.8	17.5	12	21.4	18.1
10	26	20.3	17.0	16	21.0	17.7
25	42	19.6	16.3	28	20.2	16.8
100	79	18.7	15.4	50	19.3	16.0
250	134	17.9	14.6	75	18.7	15.4
1,000	321	16.6	13.3	176	17.5	14.2
3,500	546	15.9	12.6	325	16.6	13.3
7,000	756	15.4	12.1	508	16.0	12.7
10,000	1119	14.8	11.5	742	15.4	12.1

Table 2-4 Typical Capacitive Noise & Resolution vs. Output Data Rate, 100 pF Base + 10 pF Span, fast settle, V = 3.0 V

Output Data Rate [Hz]	FLOATING Fully compensated			GROUNDED Internally compensated		
	RMS Noise [aF]	Eff. Resolution 100 pF base [Bits]	Eff. Resolution 10 pF span [Bits]	RMS Noise [aF]	Eff. Resolution 100 pF base [Bits]	Eff. Resolution 10pF span [Bits]
5	71	20.4	17.1	106	19.8	16.5
10	91	20.1	16.7	133	19.5	16.2
25	185	19.0	15.7	226	18.8	15.4
100	321	18.2	14.9	350	18.1	14.8
250	543	17.5	14.2	480	17.7	14.3
1,000	1044	16.5	13.2	987	16.6	13.3
3,500	3320	14.9	11.6	1965	15.6	12.3
7,000	4226	14.5	11.2	3675	14.7	11.4

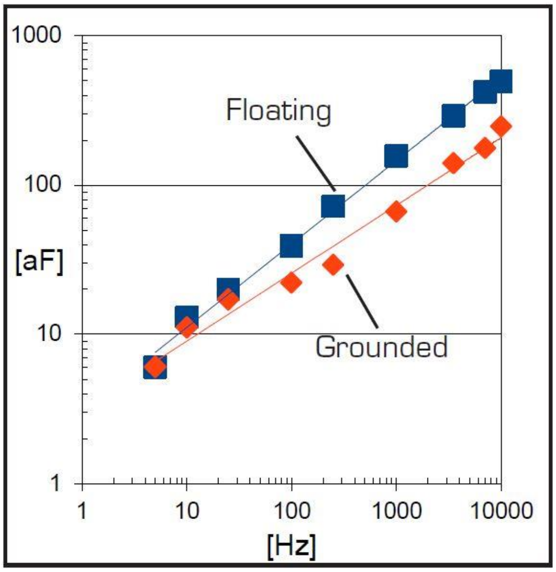


Figure 2-1 Typical Capacitive Noise vs. Output Data Rate, with 10 pF Base Capacitance, V = 3.0 V

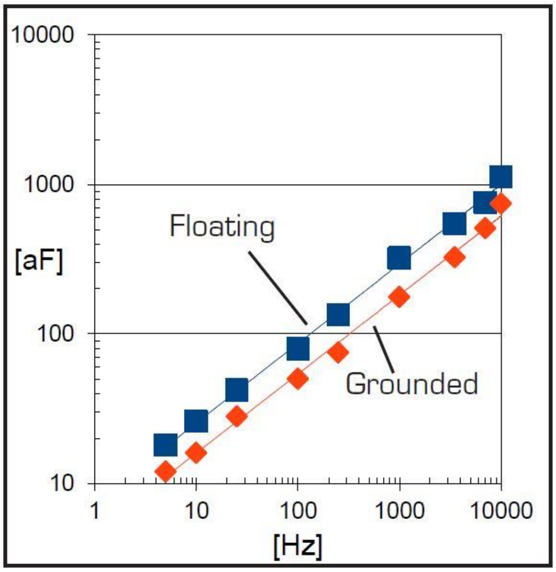


Figure 2-2 Typical Capacitive Noise vs. Output Data Rate, with 33 pF Base Capacitance, V = 3.0 V

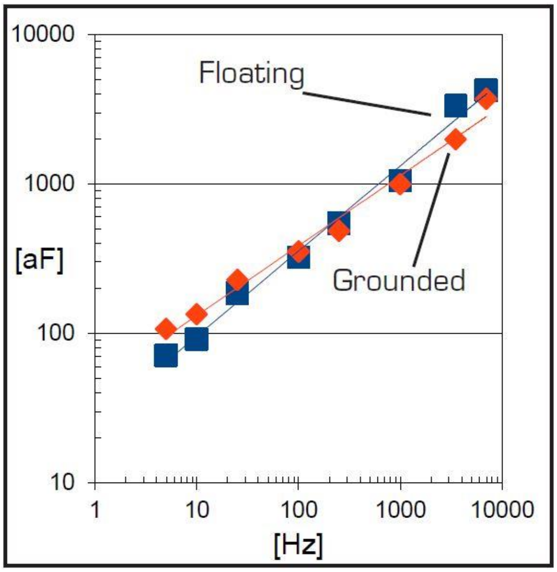


Figure 2-3 Typical Capacitive Noise vs. Output Data Rate, with 100 pF Base Capacitance, V = 3.0 V

2.2.2 RMS Noise vs. Supply Voltage

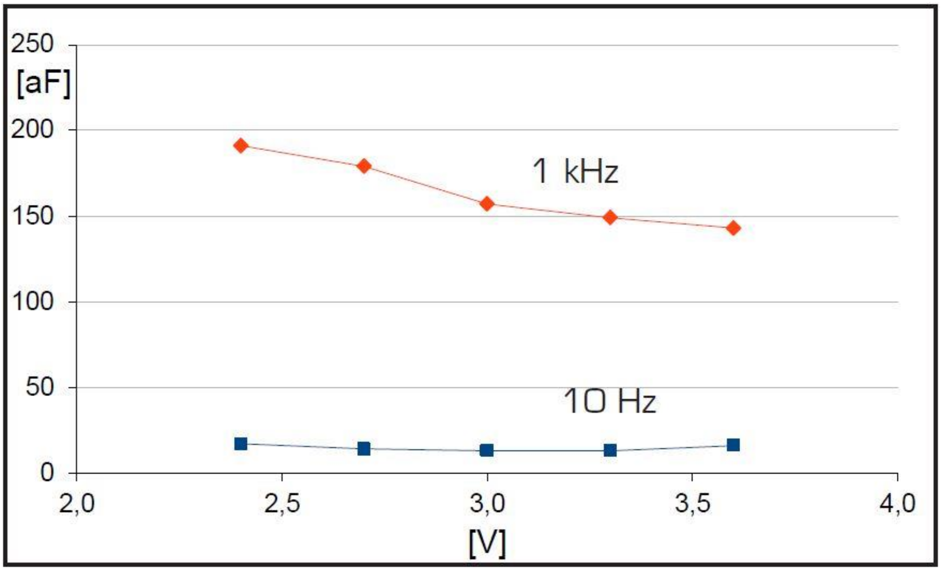


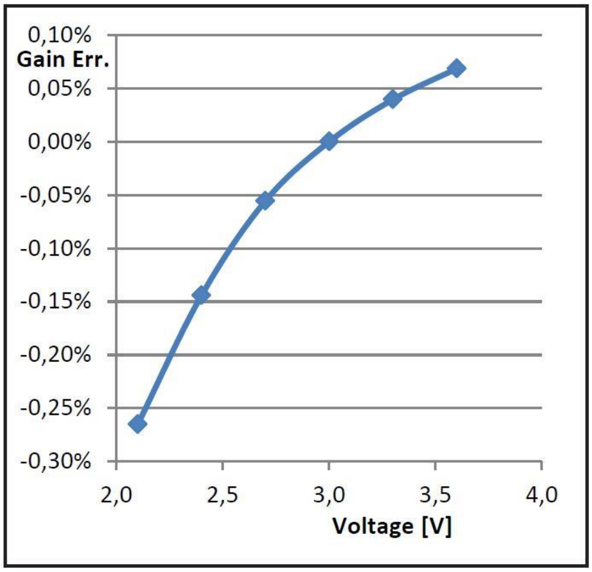
Figure 2-4 RMS Noise vs. Supply Voltage

RMS Noise expressed in aF as a function of VDD power supply voltage.

The upper curve is for 1 kHz output data rate, the lower curve for 10 Hz.

Data acquired like before with 10 pF ceramic COG capacitors connected "floating" in place of reference and sensor. The excitation capacitor was a 1 pF ceramics COG type.

2.2.3 Voltage-Dependent Offset and Gain Error (PSRR)



Data acquired like before with 100 pF ceramic COG capacitors connected "floating" in place of reference and sensor. The excitation capacitor was a 10 pF ceramics COG type.

The gain drift is the principal contribution to the error; offset drift is negligible. No dependency on update rate has been detected.

Figure 2-5 Gain Error in % vs. Supply Voltage (Power Supply Rejection Ratio)

At present, power-supply rejection ratio is poor, so the component needs well-filtered, stable supply voltages. Linear regulators will be indicated in most cases. The data presented here have been acquired in such conditions.

Any switching regulator in the supply line must be separated from the chip through a linear voltage regulator, combined with some purposefully designed RC filter. Any drift and noise in the supply line add error and noise to the output.

2.2.4 Temperature-Dependent Offset and Gain Error

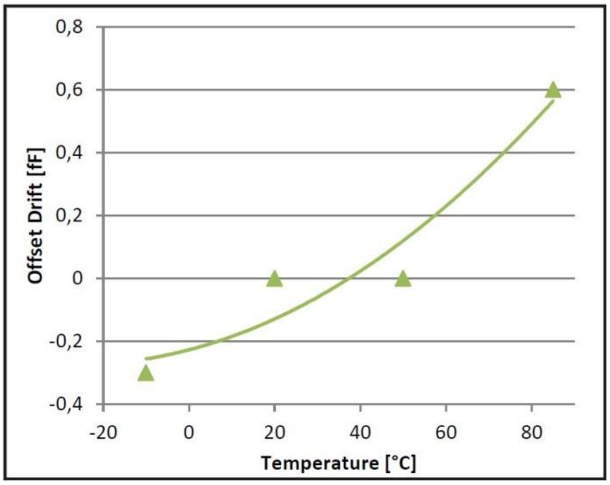


Figure 2-6 Offset Drift vs. Temperature

Offset drift as a function of temperature at 3.0V supply voltage VDD. 10 pF base capacitance, both sensor and reference, a COG ceramics capacitor each, connected “floating”.

Offset Drift:

3.0 V: 9.5 aF/K

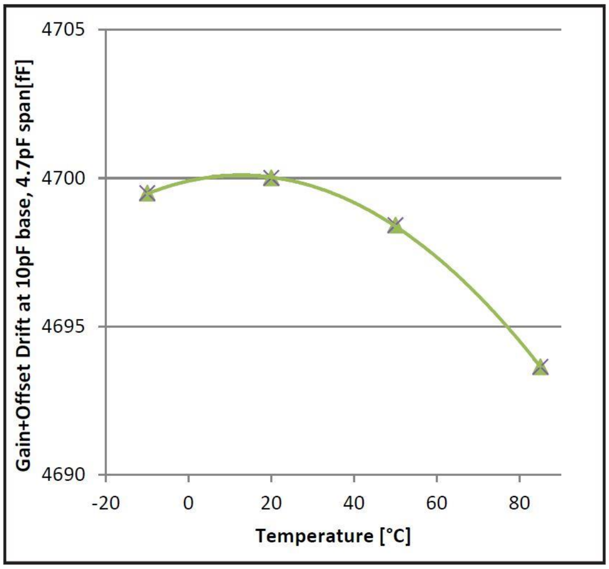


Figure 2-7 Gain Drift vs. Temperature

Gain drift as a function of temperature at 3.0V supply voltage VDD. 10 pF base capacitance, both sensor and reference, plus 4.7 pF span, with COG ceramics capacitors each, connected “floating”.

Offset Drift:

3.0 V: 13 ppm/K

2.3 Internal RC-Oscillator

The integrated RC-Oscillator can be set in the range between 10 kHz and 200 kHz, in which 50 kHz is the standard setting (see Register 1 description). The nominal frequency e.g. 50 kHz has a standard deviation of +/-20 % over parts. More than that, the internal oscillator is dependent on voltage and temperature.

For details of how to set RC oscillator by OLF_TUNE see register 1 description (Chapter 5).

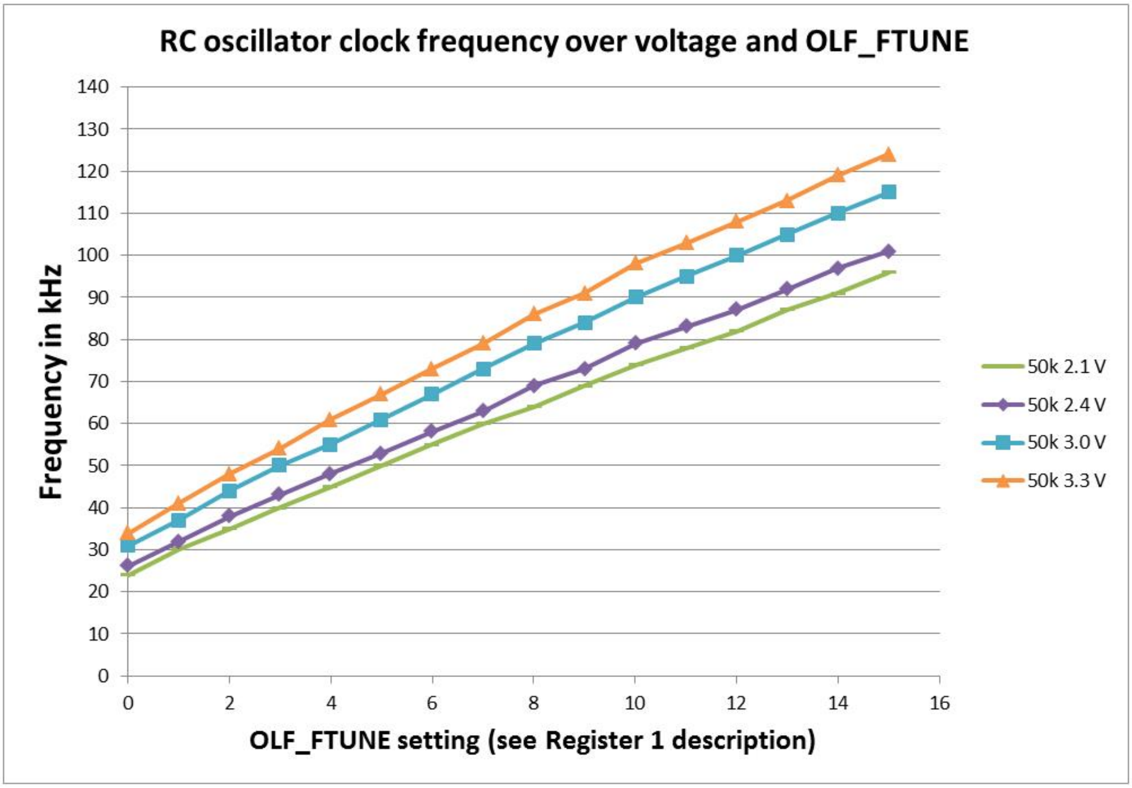


Figure 2-8: RC oscillator frequency dependence on voltage and OLF_FTUNE setting

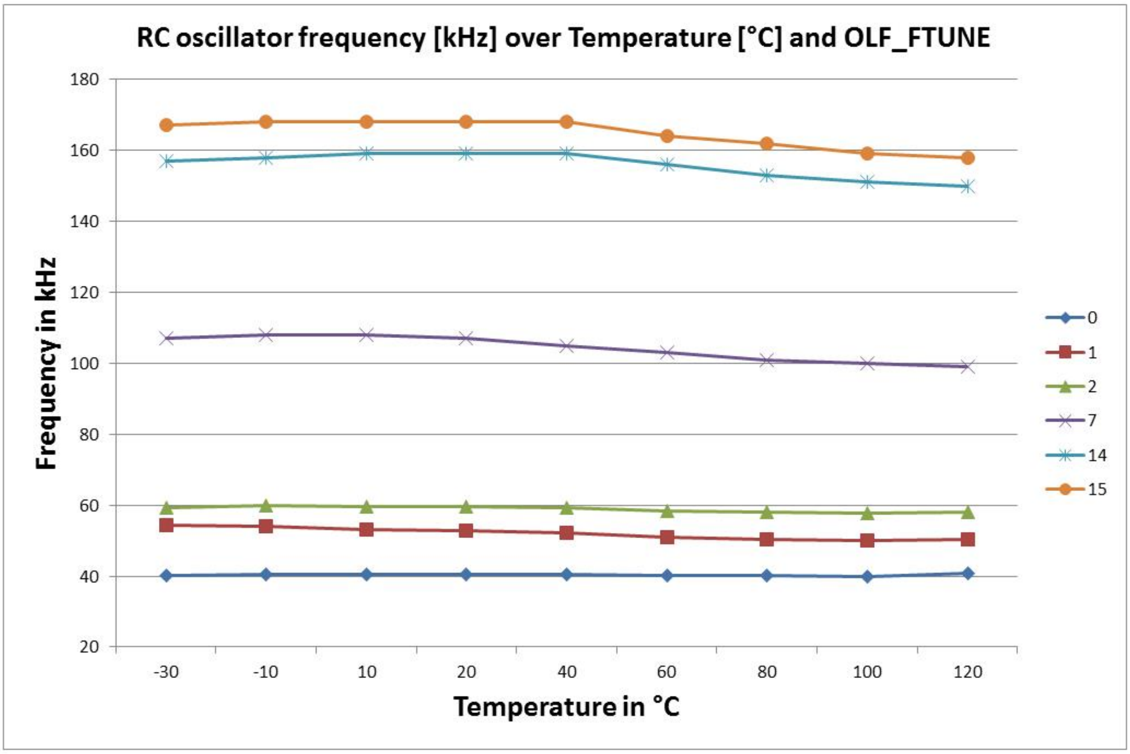


Figure 2-9: RC oscillator frequency dependence on temperature and OLF_FTUNE setting 0-15

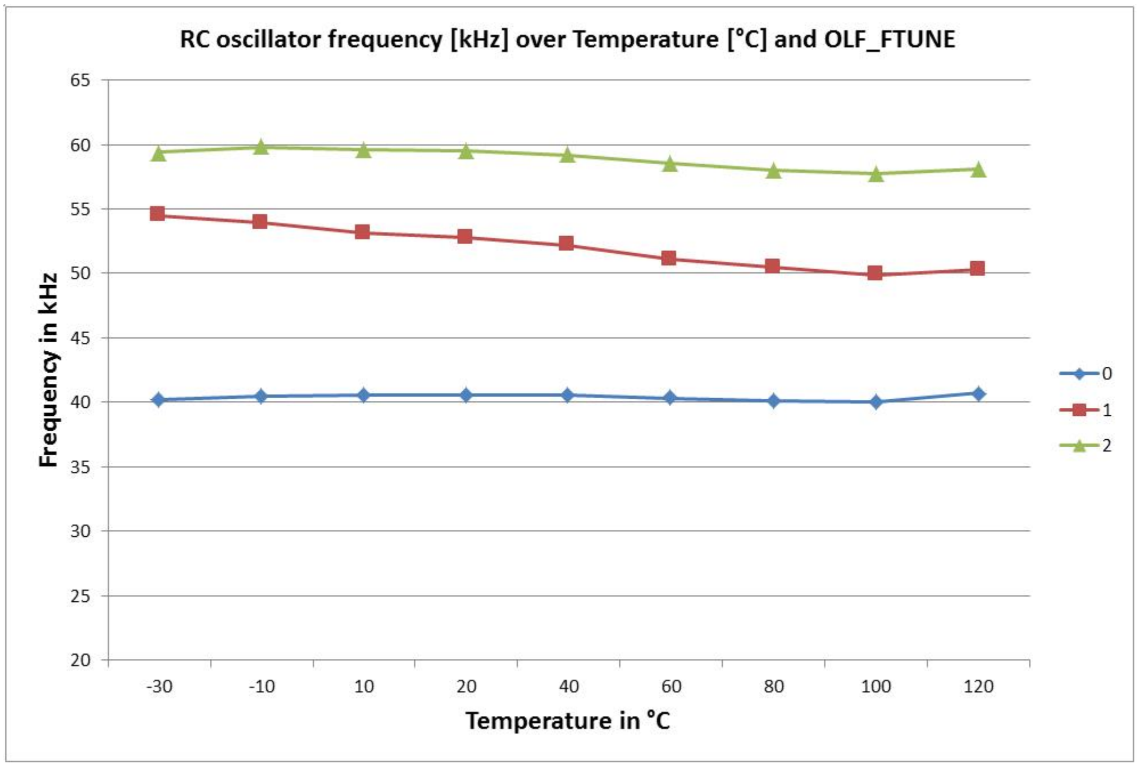


Figure 2-10: RC oscillator frequency dependence on temperature and OLF_FTUNE setting 0-2

2.4 RDC Precision

Thermoresistive Coefficients Tk at 20 °C

Material	Tk
Internal polysilicon reference	-1.1ppm/K
Internal aluminum thermistor	2830 ppm/K
External PT1000 sensor	3830 ppm/K

Resolution with internal Al/PolySi at 20 °C

Measurement Conditions	R2/Rref typ.	RMS noise R2/Rref	Typical RMS noise Temperature(*)
No averaging, 2 fake measurements	0.825	50 ppm	25 mK
16-fold averaging, 8 fake measurements	0.823	10 ppm	5 mK

(*) after linearization in post-processing software

Typical Error with internal Al-thermometer after linearization and conversion into temperature, assuming a linear relation between temperature and resistivity:

-20 °C < Temp. < 0 °C 290 mK

0 °C < Temp. < 80 °C 110 mK

2.5 Power Consumption

Table 2-5 Total Current I [µA] as a function of speed (SEQTIME) and resolution (C_AVRG) in Triggered Mode

SEQTIME (data rate [Hz])		I [µA]								
		C_AVRG (RMS resolution [Bits])								
		1	4	16	64	128	256	512	1024	2048
		(11.3)	(12.3)	(13.4)	(14.4)	(14.9)	(15.4)	(15.9)	(16.4)	(16.9)
13	(3.1)	4	4	4	5	10	10	55	80	150
12	(6.1)	4	5	7	10	20	35	80	150	
11	(12.2)	5	6	9	22	40	80	160		
10	(24.4)	6	8	15	44	82	160			
9	(48.8)	8	12	27	85	160				
8	(97.7)	12	20	49	163					
7	(195.0)	20	35	93						
6	(391.0)	36	65	178						
5	(781.0)	67	124							
4	(1560.0)	127	236							
3	(3120.0)	229								
2	(6250.0)	409								

Table 2-6 Total Current I [µA] as a function of speed (SEQTIME) and resolution (C_AVRG) in Continuous Mode (this mode yields highest possible speed/performance)

	C_AVRG (RMS resolution [Bits])								
	1	4	16	64	128	256	512	1024	2048
	(11.3)	(12.3)	(13.4)	(14.4)	(14.9)	(15.4)	(15.9)	(16.4)	(16.9)
I [µA]	515	275	204	185	182	181	180	180	179

Temperature measurement in addition to capacitive measurement will add between 2 and 10 µA approximately, depending on speed. Total consumption values below 30 µA may be obtained only when driving the on-chip 1.8 volts core supply generator in an energy-saving mode (see section 5, register 10); ultimate microamp savings with DSP slowed down (see section 5, register 8).

2.6 Package Information

2.6.1 Dice - Pad Layout

Die dimensions: 2.15 mm x 1.67 mm with pad pitch 120 µm, pad opening is 85 µm x 85 µm

Die thickness: 380 µm

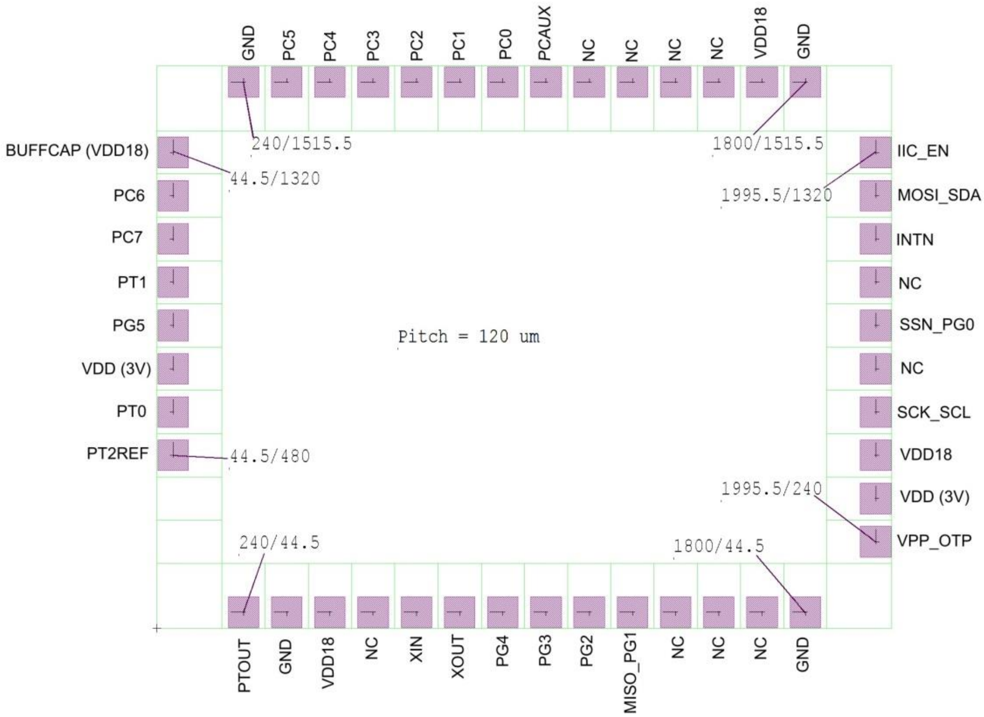


Figure 2-11: Pad Layout

2.6.2 QFN Packages

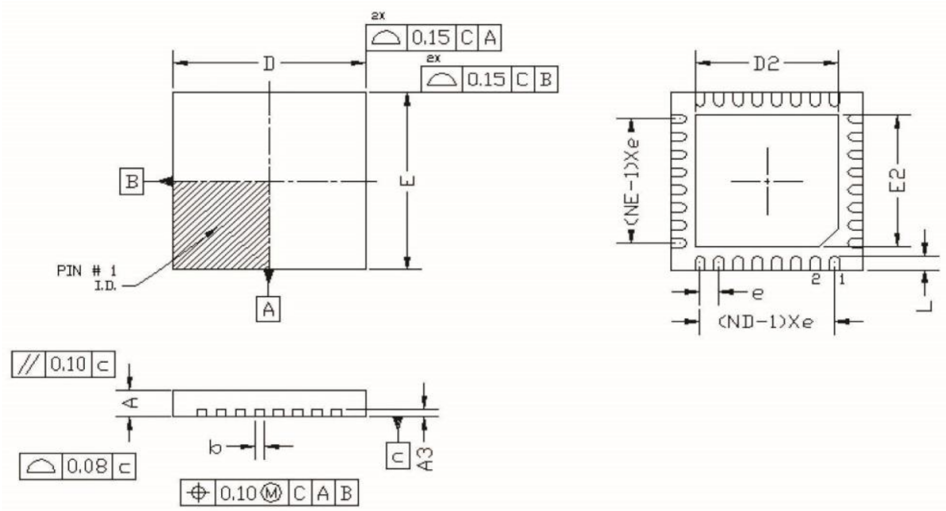


Figure 2-12: QFN package dimensions

Table 2-7: QFN Dimensions

		Dimensions in mm							
Device Name	Package	D, E	D2, E2	N	e	L	b	A	A3
PCap01-AD	QFN32	5.00	3.70	8	0.5	0.4	0.25	0.75/0.9	0.20
PCap01-AK	QFN24	4.00	2.70	6	0.5	0.35	0.25	0.75/0.9	0.20

Dimensioning and tolerances acc. to ASME Y14.5M-1994

2.6.3 Pin-Out QFN32 and QFN24 Versions

-AD: All pins are available

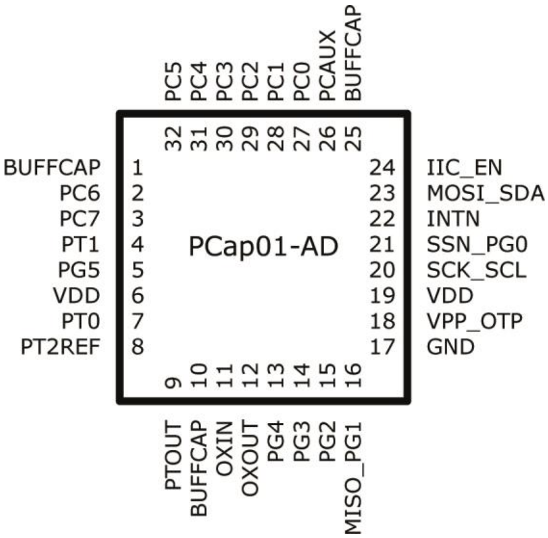


Figure 2-13

-AK: Reduced number of capacitor ports, no external oscillator

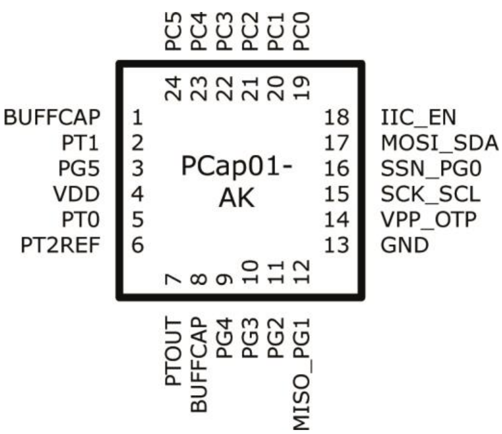


Figure 2-11

2.6.4 Pin/Pad Assignment

Pin	Description	Comment	Pin Number -AD	Pin Number -AK
BUFFCAP	Connect microfarad bypass capacitance and nanofarad bypass capacitance to GND. Bridge all BUFFCAP pins. Bypassing is mandatory!	Need to be connected in any case	1	1
			10	
			25	8
GND	Ground		17	13
IIC_EN	Put this to LOW or GND for use of SPI bus. Put it to HIGH or VDD otherwise.		24	18
INTN	Optional. Interrupt line, low active	Leave unconnected if not used	22	
MISO_PG1	Serial interface data line, Master In - Slave Out (SPI only, otherwise available as general-purpose port)		16	12
MOSI_SDA	Serial interface data line, Master Out - Slave In		23	17
OXIN	May be left open. Very exceptionally used for connecting a 4 to 20 MHz ceramics resonator or quartz.		11	
OXOUT			12	
PC0	"CDC" or capacitive measurement ports. Connect reference and sensors here, beginning with PCØ for the reference.	Leave unconnected if not used	27	19
PC1			28	20
PC2			29	21
PC3			30	22
PC4			31	23
PC5			32	24
PC6			2	
PC7			3	
PCAUX	May be used for external discharge resistor.		26	
PG2	General purpose I/O ports. PG4 and PG5 are output only, others are configurable input or output.		15	11
PG3			14	10
PG4			13	9
PG5			5	3

PT0	"RDC" or temperature measurement ports. Connect one side of the external resistive sensors here.		7	5
PT1			4	2
PT2REF	When there is an external resistive (temperature measurement) reference, connect it here, otherwise this is the place for a third resistive sensor.		8	6
PTOUT	For temperature measurement, connect the other side of the resistive sensors and a 33 nF ceramics capacitor here.		9	7
SCK_SCL	Serial interface clock line		20	15
SSN_PG0	SPI interface chip select line, low active. Alternatively general purpose I/O port.		21	16
VDD	VDD here, plus bypass capacitance to GND. Bypassing is mandatory!		6 19	4
VPP_OTP	Set to 6.5 V during OTP programming. Set back to GND rapidly after the end of the programming process. Keep pin grounded for normal device operation. Apply a 470 kOhm pull-down resistor to this pin.	Connect to GND	18	14
GND ground pad	The ground pad, bottom located, is internally connected to ground. Parallel external grounding is not necessary		-	-