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PCap04

Standard Board

PCAP04-EVA-KIT

ams Eval Kit Manual [v1-02] 2017-Oct-20 Page 1 Document Feedback

Content Guide

1	Introduction	. 3
2	Quick Start Guide	. 5
2.1	Install the Software	. 5
2.2	Install the Hardware:	. 5
2.3	Quick Start for Initial Measurements	. 6
3	Hardware Description	. 9
3.1	Connecting Capacitors and Resistors	. 9
3.2	Hardware Architecture	. 9
3.2.1	PCAP04 BOARD	. 9
3.2.2	Temperature Measurement	10
3.2.3	Pulse Code Generation	12
3.2.4	Motherboard	12
4	Software Description	13
4.1	Initialization	13
4.2	Graphical User Interface	13
4.2.1	Front Panel	13
4.2.2	Front Panel Menus	26
4.2.3	Special Windows	30
4.2.4	Linearize	37
4.2.5	Assembler	42
4.3	Scaling Results	42
4.4	Scaling PDM Output	44
5	Schematics, Layers and BOM	45
6	Ordering & Contact Information	49
7	Copyrights & Disclaimer	50
8	Revision Information	51



1 Introduction

The PCAP04-EVA-KIT evaluation system provides a complete system for generally evaluating the PCapØ4 IC. It is supplied with a main board, a plug-in board, a Windows based evaluation software, assembler software and the PICOPROG V3.0 programming device. The PCapØ4 evaluation board is connected to the PC's USB interface through the PICOPROG V3.0 programming device. The previous generation PICOPROG V2.0 programming device may also be used with the PCAP04-EVA-KIT.

Figure 1: Kit Content



Pos.	Item	Comment
1	PCapØ1-MB	Motherboard
2	PCapØ4-EVA-BOARD	Plug-in board based on PCapØ4 in QFN24 package
3	PICOPROG V3.0	Programmer and interface box
4	USB cable	Connects PICOPROG V3.0 to PC
5	High density DSUB15 cable	Connecting Evaluation board to programmer (optionally)
6	Wall power supply unit	9 V

The evaluation kit offers user-friendly operation of the PCapØ4 single-chip solution for capacitance measurement. This kit can be used to evaluate the capacitance measurement, temperature measurement and the pulse generation capabilities of the PCapØ4 chip. The kit also includes a CD-

ams Eval Kit Manual [v1-02] 2017-Oct-20



ROM containing software and data sheets. However, it is strongly recommended to use the latest data sheets and GUI software or get them on request.

2 Quick Start Guide

In this section, we described how to set up quickly the PCAP04-EVA-KIT and establish basic operation and make measurements.

2.1 Install the Software

It is crucial to install the software before connecting the evaluation kit to your computer. A default driver loading of your OS may interfere with correct installation.

- Download the latest zipped software installation package to the desired directory.
- Unzip the package to the desired directory.
- Open "setup.exe" from the unzipped directory.
- Follow the instructions on the screen.

2.2 Install the Hardware:

- Install the software before proceeding with this step!
- Connect your computer with the PICOPROG V3.0 using USB cable.
- Connect PICOPROG V3.0 and the evaluation kit motherboard using the DB15 interfaces
- Mount the plug-in board on the corresponding socket on the motherboard.
- Set the power supply unit to 7.5 V output.
- Connect the motherboard to power via the power supply unit.
 The green LED on the EVA kit motherboard should be on.





2.3 Quick Start for Initial Measurements

From the "Start" menu, go to "All Programs" and then to the "acam" directory. Double click the "PCap04 Frontpanel" icon to begin execution of the evaluation kit software. The following screen should appear:

Figure 3: Setup page

ams	PCap04	pole Ir	terface	Help									-	ı x
Setup	CDC From	ntend	CDC	RDC	PDI	M/PWN	DSP/	SP10	Misc	Exp	pert	C	m	
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	(onfigu	ration	is ready	to u	use wi	th Evalu	ation	system	m		Sta	rt Measur	ement
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- Pu - Pu - Co com	re capacita re resistan nsiders cor ipensation	nce ratio ratio nfigured mode	os 5	- Hum - Tem; - C Ser - Flo - Inter senso - PDM - PDM - Upda	idity perat ise: P ating ernal nal ti r and PULS PULS ite ra	in rh% oure in 200 & P 3 single I refere emper d refere E0 rh% E1 tem ate: 5 H	at RESO C at RES1 C1: nce sture ince perature z	- P - T - C - - - - - - - - - - - - - - - - - -	ressur emper Sense Floati Intern nterna nsor a DM PL DM PL pdate	e in % ature :: PCO 8 ng sing al refe I temp nd refe ILSE0 p LSE1 te rate 5	at RESO in °C at RES1 & PC1: gle srence erence erence ressure in % emperature 00Hz	P	nit Res Ru	eset et
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FR2	į.	0	n	one		5 ₿ 0	1	0	AO	0	0	0	0	0
FR3	8	0	n	one	•	5 ₿ 0	1	0	AO	0	0	0	0	0
FR4		0	n	one		5 ⊉ 0	1	0	AO	0	0	0	0	0
ED5		0	n	one	•	5 单 0	1	0	AO	0	0	0	0	0
1112					and the second se	Contraction of the second s	100 C							
FR6		0	n	one		5 0	1	0	AO	0	0	0	0	0

Click the "Verify Interface" Button to confirm communication with PICOPROG V3.0 is working:

Figure 4: Verify Message



The PCap04 plug-in board is pre-assembled with ceramic capacitors to emulate capacitive sensors. These capacitors, each 10 pF in value, are connected to the 6 ports PC0 to PC5.



To begin measurements using these preinstalled components, it is necessary to make the following adjustments on the "CDC Frontend" tab:

- 1. "Capacitive Measurement Scheme" section should be set to "Floating | Single".
- 2. All the capacitance ports should be turned on using the Cap. Port. Select buttons
- 3. The Stray Compensation setting should be set to "Both".

The resulting settings under the CDC tab should look like this:

Figure 5: CDC Frontend page at the start

	hday		Teele	Interfere	Liste										
116	Mer	mory	10015	Interface	Help			Tracas		122200	1				
Se	tup	CDCF	rontend	CDC	RDC	PDM/I	PWM	DSP/G	SPIO	Misc	Exp	ert	-0		
			Capacita	nce to D	igital (onver	sion F	ronten	nd						
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	C Refi exter Name C0/Cre C1/Cre C2/Cre C3/Cre	erenci rnal :f :f :f	e Select Resu 0 0 0 0	Inte 9 Its F n n n	pF	p.	fpp -27 -27 -27 -27 -27	Factor 10p 10p 10p	Offset 0 0 0 0	: AQ AQ AQ	Span 10p 10p 10p 10p	Final Result 0 0 0	Cc P1 Mean \$50 0 0 0	Rur ombined E Std Dev 0 0 0	nbit rror CA SNR (I 0 0 0
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	C Ref exter exter CO/Cre C2/Cre C2/Cre C3/Cre C3/Cre C3/Cre PT1/Re	erenci rnal ff if if if ef	e Select	lits F n n n n n n n	iliter one one one one one one		fpp -27 -27 -27 -27 -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p 10p 10p	Offset 0 0 0 0 0 0 0 0 0 0 0		Span 10p 10p 10p 10p 10p 10p	Final Result 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Cc PII Mean ∯50 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Rur ombined E Std Dev 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	nbit rror CA SNR [1 0 0 0 0 0 0 0

To begin measurements, on the right side of the window, click the following buttons in the order listed:

- 1. "Power On Reset"
- 2. "Write Complete"
- 3. "Start Measurement"

Measurements should now be running and your screen should resemble the following:

Figure 6: CDC Frontend page in use

	Ins PC	-apo4	Teele	Interfere	a Ilala										
Se	Capaci Groun	ttance	Tools irontend Capacitai : Measure : Single	Interface	E Help RDC Digital (cheme	PDP Conv Cap. 0 2 Port	M/PW ersic Port 1 0 0 0 1 2 3 Error	VM DSP/ on Fronte Select	GPIO	Misc itray (Interr	Exp Compe nal	nsation		Open Gra op Measurn Write Comp Vrite Comp ower On R	ph ement fig viete eset
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	C Refi exter Name C0/Cre C1/Cre C2/Cre C3/Cre	erence mal f f	e Select	Int 9. 1ts 1 805E / 4D70 / D60A / 060A	Filter Tone Tone Tone	P.		pp Factor 27 10p 27 10p 27 10p 27 10p 27 10p 27 10p	Offset 0 0 0 0	4 4 4 4 4 4 4	Span 10p 10p 10p	Final Result 10p 74,209p 22,8237p 23,0998p 0	Cc PI Mean ∯50 10p 74, 204p 22, 8228p 23, 0987p 0	Rur ombined E Std Dev 0 7,172f 3,324f 0	nbit rror SNR (tr 10,45 11,55 11,55 Tof
	C Refi exter Name C0/Cre C1/Cre C2/Cre C3/Cre C3/Cre	erence rnal f f f	e Select Resu 0800 3B5D 1242 127A 0000 0000	Int 9. 1ts 1 9. 1ts 1 1ts 1 1t	Filter filter tone tone tone tone			pp Factor 27 10p 27 10p 27 10p 27 10p 27 10p 27 10p 27 10p	Offset 0 0 0 0 0 0	4 4 4 4 4 4	Span 10p 10p 10p 10p	Final Result 10p 74,209p 22,8237p 23,0998p 0	Cc PI 10p 74,204p 22,8228p 23,0987p 0 0	Rur ombined E Std Dev 0 7,172f 3,324f 3,384f 0	nbit rror CA SNR (t Inf 10,45 11,55 11,55 Inf
	C Refn exter CO/Cre C2/Cre C3/Cre C5/Cre T1/2e	erence rnal f f f	e Select Resu 0800 3850 1242 127A 0000 0000 0000	Int 9. 1ts 1 005E 7 FFCC 7 4D70 7 0000 7 0000 7	Filter filter tone tone tone tone	P.		pp Factor 27 10p 27 10p 27 10p 27 10p 27 10p 27 10p 27 10p 25 1	Offset 0 0 0 0 0 0 0 0		Span 10p 10p 10p 10p 10p	Final Result 10p 74,209p 22,8237p 23,0998p 0 0 0	Cc PI 10p 74,204p 22,8228p 23,0987p 0 0 0	Rur ombined E Std Dev Ø 7,172f 3,324f 3,384f Ø Ø	SNR (b SNR (b Inf 10,45 11,55 11,55 Inf Inf

The C1 and C2 values should be continually updating but remain within a reasonably small standard deviation as shown.

At this point if the above steps have been successfully completed basic operation of the EVA kit should be achieved. The following sections provide a detailed description of the hardware and software for advanced operation.

3 Hardware Description

3.1 Connecting Capacitors and Resistors

This evaluation kit can be used for evaluating capacitance measurement by connecting capacitive sensors. Further, it can be used for evaluating temperature measurement by connecting external temperature sensitive resistors or for generating quasi analog voltage (pulse width/density modulated) that is dependent on the sensor connected to the system.

Depending on the purpose of evaluation, a modification has to be made to the same plug-in board. Following is a picture of the Mother board with the plug-in board.

Figure 7: The evaluation kit's motherboard and plug-in board

The following sections describe the modifications for each application in detail.

3.2 Hardware Architecture

3.2.1 PCAP04 BOARD

For the purpose of evaluating the capacitance measurement using PCapØ4, the plug-in board is pre-assembled with ceramic capacitors to emulate capacitive sensors. These capacitors, each 10 pF in value, are connected to the 6 ports PC0 to PC5. They are connected as single sensors in floating mode, i.e. each capacitor is connected between 2 ports, and hence there are 3 x 10 pF on-board capacitors. Please refer to section 3 of the PCapØ4 data sheet for more information on how to connect capacitors to the chip. In case using external reference, the capacitor connected between ports PC0 and PC1 is taken as the reference capacitor.



Figure 8: Details of the plug-in board (A=three C0G ceramic capacitors)



In the process of evaluation, when you are comfortable with interpreting the measurement results from the chip, these fixed capacitors can be replaced with the actual capacitive sensors of your application.

If you want to connect your capacitive sensors in grounded mode, then GND points are provided at the two ends of the board, where the sensor ground connections ought to be soldered.

The typical value of the capacitive sensors that can be connected to the evaluation kit lies in the range of 30 pF to 3.5 nF. The reference capacitor should be in the same order of magnitude as the sensor. Depending on the value of the sensor, the value of the internal resistor for performing the measurement has to be selected. For the pre-assembled 10 pF capacitors, an internal discharge resistor of 90 k Ω works well. See section 3 of the PCapØ4 data sheet on how to select the value of the internal discharge resistor.

3.2.2 Temperature Measurement

Temperature measurement or other resistive tasks may also be of interest for the user of this kit. The evaluation kit offers this possibility through the RDC (resistive-to-digital converter) ports. An onchip thermistor coupled with an on-chip temperature-stable reference resistor made of polysilicon is sufficient for observing the temperature measurement capability of the PCapØ4 chip.



Figure 9 Temperature sensor connection pads

Pos.	Item	Comment
A	Port PT1 for second external temperature sensor	not supported by the standard firmware
В	Port PT0 for external temperature sensor	
С	Port PT2 for external reference resistor	
D	10 nF COG	

However, there is a possibility to connect the reference resistor and the thermistor externally to the chip, too. In case of external resistors, the temperature-stable reference resistor ought to be connected at port PT2REF on the plug-in board. The board allows you to connect the external thermistor, e.g. a PT1000 sensor at port PT0 (or PT1, not supported yet by the standard firmware). In any case, for the temperature measurement, an external capacitor 10 nF C0G has to be connected to the chip; it is already pre-assembled on board.

3.2.3 Pulse Code Generation

Any of the capacitance or temperature measurement results from the PCapØ4 chip can be given out as a pulse width modulated or pulse density modulated signal. This output can be filtered to generate an analog output signal that can be used for further controlling.

These pulse width or pulse density codes can be generated at Ports PG0, PG1, PG2 or PG3 (in block A). Since ports PG0 and PG1 are used for the SPI Interface in the board, the hardware allows to get a valid pulse width/density modulated signal on PG2 or PG3. However, when I2C communication mode is used the pulsed signals can be optionally obtained on the ports PG0 and PG1.



Figure 10 General purpose interface ports PG0 to PG3 in block A

3.2.4 Motherboard

The motherboard connects to the PICOPROG V3.0 programmer. It serves the various power options. It can be powered via wall plug supply (B), the voltage being set from 1.8 V to 4.5 V by jumpers (C). Further, it supports a battery power option (D). The power options are switchable via jumper (E). Power present is indicated by a green LED.

There is a jumper 'Current' on the mother board (F). The current consumption of the PCapØ4 chip during operation can be directly measured from these jumper terminals.

All interface signals and general purpose I/O signals can be monitored by means of a separate jumper in block A.

4 Software Description

4.1 Initialization

Configuration files, Firmware, Settings and calibration data are subsumed in a project (.prj) file. When opening a project file then automatically the configuration and firmware data will be transferred to the chip and the chip is initialized.

Step 1: The first to do after starting the evaluation software is to read the device version from Chip by pressing the button or to select the supported PICOCAP device on the setup page. In the initial phase start with our standard firmware that calculates the capacitance ratios and resistance ratios. It automatically recognizes the operation mode and takes care of the set number of capacitors and the kind of connection. But it does no further processing.

Step 2: If you want to change from the default SPI to I2C interface, please select under Interface --> Bus --> I2C. The LED on the PICOPROG V3.0 programmer should now turn red. When the LED does not glow at all, then it indicates that the interface is faulty.

Step 3: By pressing the 'Standard'-button, the standard project file will be open.

You also may load your own project file.

Step 4: Open Graph window and press 'Start Measurement'.

4.2 Graphical User Interface

Next, the main front panel comes up. Overall, the graphical user interface offers various windows for on-line configuration, for parameter and calibration data setting, and of course for the graphical and numerical display of the measurement data. The various windows will be explained in this chapter.

4.2.1 Front Panel

Open Graph	Open a window for graphic representation of measurement data
Start Measurement	Start or stop a running measurement
Write Config.	Transfer once more, the present settings in the evaluation software to the chip (in case of doubt)
Write Complete	Transfer the complete firmware, calibration data and configuration to the chip
Power On Reset	After Power up reset, 'Write Config.' may be necessary.
Init Reset	With an init reset, the chip is re-initialized with respect to its frontend and processor.

This is the main window. On the right side, the front panel shows six general buttons:

4.2.1.1 Setup Page

] ar ile	ms PCap04 Memory	Tools Inte	erface He	lp									X
Set	up CDC F	rontend	CDC RD(PD	M/PWM	DSP/G	iPIO	Misc	Exp	pert	0	m	
				Sele PC	ect Devi ap04v1	ce	Re Versi	ad Di on fro	evice om Chi	q	Sta	Open Gra	ph
		Configura	ations rea	dy to	use with	i Evalua	ition S	ystei	n				
	Sta	ndard		H	lumidity				Pres	sure		Write Con	fig
	-		8 <u> </u>									ower On R	eset
	Pure capac Pure resist Considers o compensatio	itance ratios ance ratios configured on mode	s - H - Te - C - In - In - PC - In - In - PC - PC - PC - V	unidity mperation ense: loatin nterna ternal t sor and M PULS odate ra Verif	in rh% ar ture in °C PCO & PCI g single I referen- temperat d referen SEO rh% SE1 tempe ate: 5 Hz	t RESO at RES1 : ce ure ce erature	- Pri - Te - C (- F - 1 - In - PC - PC - Up	essur emper Sense Ioatii ntern terna isor a OM PU OM PU Odate	e in % ature :: PCO & ng sing al refe I temp nd refe LSE0 p LSE1 te rate 5	at RESO in °C at RES1 PC1: gle rence erence erence rence rence ressure in % emperature 00Hz	, a PI	Init Rese Rur Smbined E	
‡ P	lame	Results	Filter		fpp	Factor	Offset	3	Span	Final Result	Mean \$ 50	Std Dev	SNR (bi
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. 0	:1/Cref	3B5DEA	4B none	-	5 -27	10p	0	AO	10p	74,2086p	74,2064p	6,71f	10,54
0	2/Cref	124188	16 none		5 -27	10p	0	AO	10p	22,82p	22,8232p	3,616f	11,43
0	3/Cref	127A20	FD none		5 -27	10p	0	AO	10p	23,0963p	23,0993p	3,582f	11,45
6	:4/Cre <mark>f</mark>	000000	30 none		5 27	10p	0	AO	10p	0	0	0	Inf
0	5/Cref	000000	30 none	-	5 -27	10p	0	40	10p	0	0	0	Inf
	T1/Ref	000000	30 none		5 -25	1	0	AO	1	0	0	0	Inf
F		100000000000000000000000000000000000000	1011	Carton I	T	1.1.1	124	1000	17	1 The second second second	1000		

Figure 11 Setup page

Options on 'Setup' page:

Select Device	Select the PICOCAP device which you use. <pcap04v0> means silicon version "Z" <pcap04v1> means release silicon version "v1"</pcap04v1></pcap04v0>
Read Device Version from Chip	Reads the device version from chip
Standard	Opens the <selected device="">_standard.prj project file with configuration and standard firmware.</selected>
Humidity	Opens the <i><selected device="">_</selected></i> humidity.prj project file with configuration and linearization firmware.
Pressure	Opens the <i><selected device="">_</selected></i> pressure.prj project file with configuration and linearization firmware.

Verify Interface	When everything is in order, then pressing this button will indicate the release
	version number of the software and of the PICOPROG V3.0 Firmware. It also
	confirms with 'Memory read/write: OK' if a supported PICOCAP device is present.

The lower part of the window is used for real-time numerical display of the measurement results. In principal it shows the content of the read registers. The content itself depends on the firmware. Figure 1-16 shows the content as it is given with the standard firmware. The first six rows show the capacitance ratios, the last two rows show the temperature result (resistance ratio or linearized temperature).

The tab has 12 columns of information, defining labels, data format, resolution specification (white background) and results (grey background). The information in the white fields increase convenience of reading and is stored in the project files (*.prj). All number may get a character to indicate the well-known prefixes for denoting the factor in thousands ('p', 'f', 'a', 'k'...).

Name	Label for the register content, depends on the firmware.
Results	Raw hex data display of the result register content. The column before shows the width. The button column after shows whether the result is signed or unsigned.
Filter	Selection of various software filters like Sinc (rolling average) and Median (non-linear filter).
fpp	This column shows the size of the fractional part of the fixed point number and the necessary shift. Depends on the firmware.
Factor	The factor is a scaling factor that allows to scale the result according to the reference capacitor. Factor = '1' gives back the initial capacitance ratio in column 'Final Result'.
Offset	Offset to be added or subtracted in the evaluation software.
Auto Offset	By pressing [AO], the software re-calculates the 'Offset', setting back the 'Final Result' to 0
Span	Number that defines the maximum span of the sensor. Is relevant only for the calculation of the resolution in column SNR [bit].
Final Result	Display of the final result, scaled by 'Factor' and the 'Offset' added.
Mean	Display of the mean value. The sample size can be selected.
Std.Dev	Standard deviation of the 'Final Result'.
SNR [bit]	Signal-to-Noise ratio in bit, calculated as 'Span'/ 'Std.Dev.'

4.2.1.2 CDC Frontend Page

2.														
ile	Memo	ry Tools	Interfa	ce Help			-		_					
Set	tup CC)C Frontend	CDC	RDC	PDM/	WM	DSP/G	PIO I	Misc	Exp	ert		m	
		Capacit	ance to	Digital (Conver	sion F	ronten	d						
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1	Capacita	nce Measu	rement S	Scheme	Cap. Po	rt Sele	ect	St	ray (Compe	nsation		Open Graj	on
	Grounde	d Single	-	0	000	000		1	nterr	nal	• 1	Sto	p Measure	ement
					012	2 3 4	5							
					999								Write Con	fig
					Port Err	or						W	/rite Comp	lete
						51						P	ower On Re	eset
	Dischar	ge Resistar	ice Port (03 Disc	harge Re	esista	nce Port	45 CI	narge	e Resis	tance		Init Rese	ut i
	90k	1		90k		F	- 1	1	Ok				init itere	
	C Refere	nce Select	In 9	iternal Ca	p.									
	C Refere	nce Select	ln 9	itemai Ca	p.								Rur Imbined Er	
t	C Refere externa	nce Select	in 9 ults	Filter	p.	fpp	Factor	Offset		Span	Final Result	Co PII Mean ‡150	Rur embined Er	
	C Refere externa Name 20/Cref	ence Select	ults 0005E	Filter	p.	fpp	Factor 10p	Offset 0	AO	Span 10p	Final Result 10p	Co PII Mean \$50 10p	Run embined Er	nbit Control of the second sec
	C Refere externa Name D0/Cref C1/Cref	ence Select	ults 0005E DFFCC	Filter none none	p.	fpp -27 -27	Factor 10p 10p	Offset 0 0	AO	Span 10p 10p	Final Result 10p 74,209p	Co PII Mean \$ 50 10p 74,204p	Run embined Er Std Dev Ø 7,172f	sNR [t Inf 10,45
	C Refere externa Name CO/Cref C1/Cref C2/Cref	Res	ults 0005E DFFCC 24D70	Filter none none	p.	fpp -27 -27 -27	Factor 10p 10p	Offset 0 0 0	40 40	Span 10p 10p 10p	Final Result 10p 74,209p 22,8237p	Co PI Mean (50 10p 74,204p 22,8228p	Run Imbined Er Std Dev 0 7,172f 3,324f	SNR [t 10,45 11,55
	C Refere externa Name C0/Cref C1/Cref C2/Cref C3/Cref	Res 8080 385 124 127	ults 0005E DFFCC 24D70 AD60A	Filter none none none	p.	fpp -27 -27 -27 -27	Factor 10p 10p 10p	Offset 0 0 0 0	40 40 40	Span 10p 10p 10p 10p	Final Result 10p 74,209p 22,8237p 23,0998p	Ca PII Mean∯50 10p 74,204p 22,8228p 23,0987p	Rur embined Er Std Dev 0 7,172f 3,324f 3,384f	bit rror SNR [t 10,45 11,55 11,55
	C Refere externa Name C0/Cref C1/Cref C3/Cref C3/Cref	Res 885 885 124 127 886	ults 0005E 24D70 AD60A 00000	Filter none none none none	p.	fpp -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p	Offset 0 0 0 0 0	40 40 40 40	Span 10p 10p 10p 10p 10p	Final Result 10p 74,209p 22,8237p 23,0998p 0	Cc Mean ∰50 10p 74,204p 22,8228p 23,0987p 0	Rur embined Er Std Dev 0 7,172f 3,324f 3,384f 0	Inf Inf Inf Inf Inf Inf Inf
	C Refere externa Name C0/Cref C1/Cref C3/Cref C3/Cref C3/Cref	Res 8 080 385 124 127 000 000	ults 0005E 0FFCC 24D70 AD60A 00000 00000	Filter none none none none	P.	fpp -27 -27 -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p 10p 10p	Offset 0 0 0 0 0 0 0 0	40 40 40 40 40 40	Span 10p 10p 10p 10p 10p 10p	Final Result 10p 74,209p 22,8237p 23,0998p 0 0	Cc Mean \$50 10p 74,204p 22,8228p 23,0987p 0 0	Rur embined Er Std Dev 0 7,172f 3,324f 3,384f 0 0	Inf Inf Inf Inf Inf Inf
	C Refere externa Name C0/Cref C1/Cref C3/Cref C3/Cref 25/Cref P11/Ref	Res Res 080 385 124 127 000 000 000	ults 0005E DFFCC 24D70 AD60A 00000 00000 00000	Filter none none none none none none	p. 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	fpp -27 -27 -27 -27 -27 -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p 10p 10p 1	Offset 0 0 0 0 0 0 0 0 0 0	40 40 40 40 40	Span 10p 10p 10p 10p 10p 10p	Final Result 10p 74,209p 22,8237p 23,0998p 0 0 0 0	Cc Mean \$50 10p 74,204p 22,8228p 23,0987p 0 0 0 0	Rur embined Er Std Dev 0 7,172f 3,324f 3,384f 0 0 0	SNR [t Inf 10,45 11,55 11,55 Inf Inf Inf

Figure 12 CDC Frontend page



Options on 'CDC Frontend page:

Capacitance Measurement Scheme	Grounded Single – Single capacitive sensor connected between a port and ground.
	Grounded Differential – Differential capacitive sensor connected between 2 ports with the middle tap of the sensor connected to ground.
	Floating Single – Single capacitive sensor connected between 2 ports.
	Floating Differential – Differential capacitive sensor connected between 2 ports with the middle tap of the sensor connected to another 2 ports.
Cap. Port Select	Select which capacitive ports have to be measured (Ports 0-5), i.e. at which ports the sensors have been connected in hardware.
Stray Compensation	None – No compensation
	Internal – One additional measurement performed through only the chip- internal stray capacitance with respect to ground.
	External – One additional measurement per port pair, performed through a parallel connection of the capacitance at the two ports with respect to ground.
	Both – Both internal and external compensation together.
Discharge Resistance Port 03	Selects the value of the internal resistance (180k, 90k, 30k, 10k) for measurements on port PC0 to PC3 through which the discharge cycles during measurement are to be performed. This value has to be selected in accordance with the capacitance value of the sensor.
Discharge Resistance Port 45	Selects the value of the internal resistance (180k, 90k, 30k, 10k) for measurements on port PC4 to PC5 through which the discharge cycles during measurement are to be performed. This value has to be selected in accordance with the capacitance value of the sensor.
Charge Resistance	Choice of one out of 4 on-chip charging resistors (180k, 10k) for the CDC. Permitting to limit the charging current and avoiding transients.
C Reference Select	Switching between external and internal reference capacitance.
Internal Cap	Selection of internal reference capacitance value. (031pF)

4.2.1.3 CDC Page

	ams PCap	04			17								X
File	e Memo	ory Tools Interfa	ice Help										
Se	etup C	DC Frontend CDC	RDC	PDM/P	WM	DSP/0	SPIO	Misc	Exp	pert	0	m	
		Capacitance to	Digital Co	nvers	ion S	Setting	s						
C	ycle Cont	rol									6		
	Prech	arge Time	Fullcharge 1	ime		Disch	arge Tin	ne				Open Gra	ph
		0 🚔 s × 3FF	20u	\$ x C			20u 🌲	s ×C			Sta	rt Measur	ement
		• •	-		-	4				C FAKE		Write Con	fig
1	/00	_	1			×				0		/rite Comp	lete
						1				C AVRG			ecet
			15/653	20		1				(Sample Size)		OWEIONA	eset
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	ov							\geq					
	Outle C	lock Select					1	ime					
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	50,0101	- 1 com romen									6		
C	onversior	Control											
	Can Tr	inner Select		SVT. Triz	iner.l	Din							
	Timer	Triggered		DED IN	10		Co	onver	sion Ti	me 80,0ms		Drug	
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	Conver	sion Time					N	Aeasu	uring R	ate 12,5Hz	Co	mbined E	rror 🔘
	2000	A. T								inter (
											H		JAF
ŧ	Name	Results	Filter		fpp	Factor	Offset		Span	Final Result	Mean 🗍 50	Std Dev	SNR (bit
)	CO/Cref	0800005E	none .		-27	10p	0	AO	10p	10p	10p	0	Inf
1	C1/Cref	3B5DEA4B	none .	. 5	-27	10p	0	40	10p	74,2086p	74,2064p	6,71f	10,54
2	C2/Cref	12418816	none 💽	5	-27	10p	0	AO	10p	22,82p	22,8232p	3,616f	11,43
3	C3/Cref	127A20FD	none .	5	-27	10p	0	40	10p	23,0963p	23,0993p	3,582f	11,45
4	C4/Cref	00000000	none .	5	-27	10p	0	AO	10p	0	0	0	Inf
5	C5/Cref	00000000	none .	5	-27	10p	0	AC	10p	0	0	0	Inf
6	PT1/Ref	00000000	none .	- 5 A	-25	1	0	AO	1	0	0	0	Inf
7	Alu/Ref	01DD2CBE	Median 5		-25	1	0	AO	1	931,982m	931,937m	30,36u	15,01

Figure 13 CDC page

Options on 'CDC page:

Cycle Control

Precharge Time	Time to charge via resistor for current limitation, can be set in multiples of the cycle clock
Fullcharge Time	Time for final charge without current limitation, can be set in multiples of the cycle clock
Discharge Time	Time to discharge the capacitor, can be set in multiples of the cycle clock
C_FAKE	Number of fake measurements per measurement cycle. Performing fake measurements may help in reducing noise.



C_AVRG	Enables averaging the measurement results over multiple measurement cycles. Setting to 1 \rightarrow No averaging, Setting to any number N, will result in averaging over N measurement cycles for generating one measurement result. (08191)
Cycle Clock Select	50,0kHz Low Power – Single capacitive sensor connected between a port and ground.
	500kHz High Speed/4 – Differential capacitive sensor connected between 2 ports with the middle tap of the sensor connected to ground.
	2,00MHz High Speed – Single capacitive sensor connected between 2 ports.
Conversion Duration	Displays the entire conversion duration per cycles for averaging and fake measurements.
C_TRIG_SEL	Selects the source that triggers the start of a capacitance measurement
	Continuous – Continuous measurement, self-triggering. Recommended when no temperature measurement is made in parallel.
	Read Triggered – Triggered by read out
	Timer Triggered – Depending on the setting the 'Conversion Time'. Generally recommended setting \rightarrow less prone to error conditions.
	Timer Triggered (Stretched) – Depending on the setting the CONV_TIME. The parameter is used as sequence period.
	Pin triggered – Triggered by external Pin, selectable from option ext.Trigger-Pin
	Opcode Triggered Off – Started by SPI Command 0x8C
	Continuous (exp.) – (not recommended)
Ext. Trigger-Pin	Used to select the pin to be used as the source of trigger for the capacitance measurement.
	NOTE: In the delivered EVA board, the pins DSP_IN0 and DSP_IN1 are part of the SPI communication interface, hence only DSP_IN2 and DSP_IN3 selections are relevant.

Conversion Control

CONV_TIME	Sets the conversion time in multiples of twice the period of the low-frequency clock
Conversion Time	Displays the entire conversion time per measurement.
Measuring rate	Displays the frequency at which capacitive measurement data is transferred from the DSP to the interface (SPI or I2C).

4.2.1.4 RDC Page



Figure 14 RDC page

Options on 'RDC' page:

Temp.Sensor0	To select a thermistor connected to port PT0/REF for temperature measurement. This could be e.g. an external PT1000.
Temp.Sensor1	To select a thermistor connected to port PT1 for temperature measurement.
Temp.Sensor2	To select either the internal aluminum (ALU) thermistor for temperature measurement.
Reference	To select either the internal Poly-Si thermistor or an external reference resistor at port PT0/REF for temperature measurement.

Cycle Control

Precharge Time	Displays the precharge time. It depends on R_OLF_DIV.
Fullcharge Time	Displays the fullcharge time It depends on R_OLF_DIV.
Discharge Time	Set the discharge time. It depends on R_OLF_DIV.
R_AVRG	Set averaging for temperature measurement.
R_FAKE	Set number of fake measurements per temperature measurement cycle.
Conversion Duration	Displays the entire conversion duration per cycles for averaging and fake measurements.

Conversion Control

Temp. Trigger Select	Selects the source that triggers the start of a temperature measurement
	Off : Default setting when no temperature measurement is wanted. In this case, a temperature measurement can still be started by SPI Command 0x8E.
	OLF_CLK: Triggered by Low-frequency oscillator.
	Pin-Triggered : Triggered by external Pin, selectable from option ext.Trigger-Pin
	CDC asynchronous : Depending on the setting in the 'T_TRIG_PREDIV' counter on the RDC page. The DSP is triggered by the RDC end of conversion. If RDC rate is less than CDC rate the DSP is triggered directly from the CDC for inactive RDC conversions.
	CDC synchronous : Depending on the setting in the 'T_TRIG_PREDIV' counter on the RDC page. The DSP is triggered by the RDC end of conversion. Assuming that RDC rate is less than the CDC rate, the inactive RDC conversions are replaced by a delay.
R_TRIG_PREDIV	For CDC and OLF options the RDC measure rate can be reduced by setting a divider.
Conversion Time	Displays the entire conversion time per measurement.
Measuring Rate	Displays the frequency at which capacitive measurement data is transferred from the DSP to the interface (SPI or I2C).
Ext. Trigger-Pin	Used to select the pin to be used as the source of trigger for the capacitance measurement.
	NOTE: In the evaluation board, the pins DSP_IN0 and DSP_IN1 are part of the SPI communication interface, hence only DSP_IN2 and DSP_IN3 selections can be used.

4.2.1.5 PDM / PWM Page

	ams PCap	104												×
File	e Memo	ry Tools Ir	nterface	Help										
S	etup Cl	DC Frontend	CDC	RDC	PDM/P	WМ	DSP/G	SPIO	Misc	Exp	pert		m	
	Pulse Int	terface 0			Pul	se Int	t <mark>erf</mark> ace 1							
	CI	ock Select					Clock Se	elect					Open Graj	oh
	0	HF / 1	▼ 5				OHF / 1	-	•	5		Sta	rt Measure	ement
	Re	esolution					Resolut	ion					Write Con	fig
	14	4 bits	• 2				10 bits	8	•	0			Vrite Comp	lete
	Pu	lise Interface	Select				Pulse Ir	nterface	Sele	ct		P	ower On R	eset
	P	DM	• 1				PDM		-	1			Init Rese	t
		Toggle Enable	e				Togg	le Enab	le					
	Pu	ulse Select					Pulse S	elect						
	C	1/Cref	• 1				Alu/Re	f	-	7				
													Run	bit 🥘
												Cc	Run ombined Er	bit 🧶 ror 🌒
													Run ombined Er	ibit) ror)
+	Name	Result	s F	ilter		fpp	Factor	Offset		Span	Final Result	Co PI	Run ombined Er	
#	Name C0/Cref	Result	s F 05E nd	ilter		fpp -27	Factor 10p	Offset 0	04	Span 10p	Final Result 10p	Co PI Mean $\frac{2}{30}$ 10p	Rur ombined Er C C C Std Dev	bit
# 0	Name C0/Cref C1/Cref	Result 08000 385DE	s F Ø5E no A4B no	ilter one [fpp -27 -27	Factor 10p 10p	Offset 0 0	40	Span 10p 10p	Final Result 10p 74,2086p	Cc PI Mean \$ [50 10p 74, 2064p	Rur ombined Er Std Dev 0 6,71f	bit ror CAF SNR (bi Inf 10,54
# 0 1 2	Name CO/Cref C1/Cref C2/Cref	Result 08000 385DE 12418	s F 05E nd A4B nd 816 nd	ilter one [one [fpp -27 -27 -27	Factor 10p 10p	Offset 0 0 0	40	Span 10p 10p	Final Result 10p 74,2086p 22,82p	Cc PI Mean ∯50 10p 74, 2064p 22, 8232p	Run ombined Er Std Dev Ø 6,71f 3,616f	bit ror CAF SNR (bi Inf 10,54 11,43
# 0 1 2 3	Name C0/Cref C1/Cref C2/Cref C3/Cref	Result 08000 385DE 12418 127A2	s F 05E nd A4B nd 816 nd 0FD nd	ilter one [one [one [one [fpp -27 -27 -27 -27	Factor 10p 10p 10p	Offset 0 0 0 0	40 40 40 40	Span 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p	Cc PI Mean ∯50 10p 74, 2064p 22, 8232p 23, 0993p	Rur ombined Er Std Dev 0 6,71f 3,616f 3,582f	bit ror CAF SNR (b) Inf 10,54 11,43 11,45
# 0 1 2 3 4	Name C0/Cref C1/Cref C2/Cref C3/Cref C4/Cref	Result 08000 3B5DE 12418 127A2 00000	s F 05E nd 816 nd 0FD nd 000 nd	ilter one [one [one [one [one [fpp -27 -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p	Offset 0 0 0 0 0	40 40 40	Span 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p 0	Cc PI Mean ∰50 10p 74, 2064p 22, 8232p 23, 0993p 0	Rur ombined Er Std Dev 0 6,71f 3,616f 3,582f 0	bit ror CAF SNR (b Inf 10,54 11,43 11,45 Inf
# 0 1 2 3 4 5	Name C0/Cref C1/Cref C2/Cref C3/Cref C4/Cref C5/Cref	Result 08000 3B5DE 12418 127A2 00000 00000	s F 05E ni A4B ni 816 ni 0FD ni 000 ni 000 ni	ilter one [one [one [one [one [one [fpp -27 -27 -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p 10p	Offset 0 0 0 0 0 0 0 0	40 40 40 40 40 40 40 40 40 40 40 40 40 4	Span 10p 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p 0 0	Cc PI Mean ∯50 10p 74,2064p 22,8232p 23,0993p 0 0 0	Rur ombined Er Std Dev 0 6,71f 3,616f 3,582f 0 0	bit ror CAF SNR (bi Inf 10,54 11,43 11,45 Inf Inf
# 0 1 2 3 4 5 6	Name C0/Cref C1/Cref C2/Cref C3/Cref C4/Cref C5/Cref PT1/Ref	Result 08000 385DE 12418 127A2 00000 00000 00000	:s F 05E n A4B n 816 n 0FD n 000 n 000 n	ilter one [one [one [one [one [one [one [fpp -27 -27 -27 -27 -27 -27 -27 -25	Factor 10p 10p 10p 10p 10p 10p	Offset 0 0 0 0 0 0 0 0 0 0	4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	Span 10p 10p 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p 0 0 0	Cc PI Mean ∯50 10p 74,2064p 22,8232p 23,0993p 0 0 0 0	Run ombined En Std Dev 0 6,71f 3,616f 3,582f 0 0 0	bit ror CAF SNR (bi Inf 10,54 11,43 11,45 Inf Inf Inf Inf

Figure 15 PDM/PWM page

Options on 'PDM / PWM' Page:

Clock Select	Selects the clock frequency to be used for the PWM/PDM generation.
Resolution	Resolution of the output in bits. This resolution also determines the pulsed output range.
Pulse Interface Select	Select the pulse interface – Pulse Width Modulated Output (PWM) or Pulse Density Modulated (PDM) Output. Of the two, the PDM is the recommended interface.
	With PWM option, 100 kHz clock and 10-bit resolution the resulting PWM output frequency = $(100 \text{ kHz} / 1024) \sim 100 \text{ Hz}.$



Toggle Enable	activates toggle flip flop at Pulse Interface Output, especially for PDM to create 1:1 duty factor
Pulse Select	Select the measurement result which has to be given out as pulsed output – any of the capacitance or temperature measurement results.

4.2.1.6 DSP/GPIO Page

1	ams PCap04												×
Fil	e Memory T	ools Interfa	ce Help	-									
S	etup CDC From	ntend CDC	RDC	PDN	I/PWM	DSP/G	iPIO I	Misc	Exp	pert.	Q	m	
	DSP_SPEED Slow DSP_START OSP_START OSP_START CDC_TRIG_EN CDC_TRIG_EN	_EN			P_FF_IN	ONPIN	DS	P_M	OFLO_E	EN	Sta	Open Gra rt Measure Write Con Irite Comp ower On R Init Rese	ph ement fig lete eset et
0	apio												
	PG_DIR_IN PG_PU				PG0xP0	32 se0 > PG 33 se1 > PG	2 3	[PG4	_INTN_EN _INTN_EN	» اح	Rur ombined E	nbit ● rror ● ? ∆₽
#	Name	Results	Filter		fpp	Factor	Offset		Span	Final Result	Mean 🛔 50	Std Dev	SNR [bit]
0	C0/Cref	0800005E	none	- 5	-27	10p	0	AO	10p	10p	100	0	Inf
1	C1/Cref	3B5DEA4B	none	¥ 5	-27	10p	0	40	10p	74,2086p	74,2064p	6,71f	10,54
2	C2/Cref	12418816	none	• 5	-27	10p	0	AO	10p	22,82p	22,8232p	3,616f	11,43
3	C3/Cref	127A20FD	none	• 5	-27	10p	0	AO	10p	23,0963p	23,0993p	3,582f	11,45
4	C4/Cref	00000000	none	. 5	-27	10p	0	AO	10p	0	0	0	Inf
5	C5/Cref	00000000	none	- 5	-27	10p	0	40	10p	0	0	0	Inf
6	PT1/Ref	00000000	none	• 5	-25	1	0	AO	1	0	0	0	Inf
7	Alu/Ref	01DD2CBE	Median 5	• 5	-25	1	0	40	1	931,982m	931,937m	30,36u	15,01

Figure 16 DSP/GPIO page



Options on 'DSP/GPIO' Page:

DSP

DSP_SPEED	Select the DSP Speed. Choose between Fastest, Fast, Slow and Slowest.
DSP_FF_IN	Pin mask for latching flip-flop activation (PG0 to PG3)
DSP_MOFLO_EN	Activates anti-bouncing filter in PG0 and PG1 lines
DSP_STARTONPIN	Not supported by standard firmware The DSP can be started externally by a signal on a pin; these buttons select the pin that has to be sensed for detecting the start signal.
DSP_START_EN	Mask for activating various trigger sources for starting the DSP

GPIO

PG_DIR_IN	To configure the ports PG0-PG3 as input (otherwise output)						
PG_UP	To enable the internal pull up on the ports PG0-PG3						
PG0_X_PG2	Possible only when the selected interface for communication is IIC. Interchange PortG0 with PortG2. This is useful when the Pulsed output is needed on Port PG0 instead of PG2.						
PG1_X_PG3	Possible only when the selected interface for communication is IIC. Interchange PortG1 with PortG3. This is useful when the Pulsed output is needed on Port PG1 instead of PG3.						
PG4_INTN_EN	Map the Interrupt output from chip, INTN to Port PG4. This setting is useful for 24 pin QFN package, because the dedicated INTN pin is absent in this version.						
PG5_INTN_EN	Map the Interrupt output from chip, INTN to Port PG5. This setting is useful for 24 pin QFN package, because the dedicated INTN pin is absent in this version.						

4.2.1.7 Misc. Page

	anis reapos												
Fil	e Memory 1	Fools Interfa	ce Help										
S	etup CDC Fro	ontend CDC	RDC	PDM/	PWM	DSP/C	SPIO 1	Aisc	Exp	pert	d	m	
L	F Clock				HF (Clock							
			TUNE			OX_RUN	4					Open Gra	ph
	200kHz	11				Perman	nent		-	1	Sta	rt Measure	ement
						■ox_d	iis UTOSTOI	P_DI:	s 🗖	OX_STOP OX_DIV4	Pr	Write Con Irite Comp ower On Ri Init Rese	fig lete eset
0	Guarding												
	Guarding Po	ort Select	CGTIM	ELVED	0								
	0 1 2 3 4 C_G_OP_RUI pulsed	N	4 [] [] C_G_C	DP_EXT	uns)		7 C_G_OI 2,0 pF C_G_OI x 1,00	►_AT ►_VU ►	7 TN 3		Cc	Rur mbined Er	ıbit 🥥 rror 🔵
ŧ	0 1 2 3 4 C_G_OP_RUI pulsed	A 5 N		DP_EXT	for	Fartor	7 C_G_01 2,0 pF C_G_01 x 1,00	▼_AT ▼_VU ▼	7 TN 3 0	Final Decuit	Co PI	Rur ombined Er	
# 0	0 1 2 3 4 C_G_OP_RUI pulsed	A 5 N Results	G_G_C G_G_C Filter	DP_EXT	fpp	Factor	7 C_G_OI 2,0 pF C_G_OI x 1,00 Offset	AT P_AT P_VU VU VU T	7 TN 3 0 Span	Final Result	Cc PI Mean \$50	Rur ombined Er	ibit) rror) CAP
# 0 1	0 1 2 3 4 C_G_OP_RUI pulsed Name C0/Cref	Results 080005E 3BSDEAAP	Filter	DP_EXT	fpp -27	Factor 10p	7 C_G_OI 2,0 pF C_G_OI x 1,00 Offset 0		7 TN 3 0 Span 10p	Final Result 10p	Cc PII Mean ∯50 10p 74, 2064≂	Rur ombined Er C D (Std Dev 0 6 71 f	ibit
# 0 1 2	0 1 2 3 4 C_G_OP_RUI pulsed Name C0/Cref C1/Cref C2/Cref	Results 0800005E 3B5DEA4B	Filter	DP_EXT	fpp -27 -27	Factor 10p 10p	7 C_G_01 2,0 pF C_G_01 x 1,00 Offset 0 0	A	7 TN 3 0 5pan 10p 10p	Final Result 10p 74,2086p 22,82n	Cc PII Mean \$50 10p 74,2064p 22,8232p	Run ombined Er Std Dev 0 6,71f 3,616f	ibit
# 0 1 2 3	Name CO/Cref C1/Cref C2/Cref C3/Cref	Results 0800005E 3B5DEA4B 12418816 127420ED	Filter none none none		fpp -27 -27 -27 -27	Factor 10p 10p 10p	7 C_G_01 2,0 pF C_G_01 x 1,00 Offset 0 0 0 0		7 TN 3 0 0 Span 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23.0963p	Cc PII Mean #50 10p 74,2064p 22,8232p 23,0993n	Run ombined Er Std Dev 0 6,71f 3,616f 3,582f	Ibit) rror) CAP SNR (bit) Inf 10,54 11,43 11,45
# 0 1 2 3 4	Name C2/Cref C2/Cref C2/Cref C3/Cref C4/Cref	Results 0800005E 3B5DEA4B 12418816 127A20FD 00000000	Filter none none none none	PP_EXT	fpp -27 -27 -27 -27 -27 -27	Factor 10p 10p 10p 10p	7 C_G_01 2,0 pF C_G_01 x 1,00 Offset 0 0 0 0 0 0		7 TN 3 0 0 5pan 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p 0	Cc PI Mean ∯50 10p 74,2064p 22,8232p 23,0993p 0	Run ombined Er Std Dev 0 6,71f 3,616f 3,582f 0	Ibit rror CAP SNR (bit) Inf 10,54 11,43 11,45 Inf
# 0 1 2 3 4 5	Name C_C_CP_RUI pulsed Name C0/Cref C1/Cref C2/Cref C3/Cref C3/Cref C3/Cref C3/Cref	Results 0800005E 3B5DEA4B 12418816 127A20FD 00000000 00000000	Filter none none none none none	DP_EXT	fpp -27 -27 -27 -27 -27 -24 -24	Factor 10p 10p 10p 10p 10p	7 C_G_01 2,0 pF C_G_01 × 1,00 0 0 0 0 0 0 0 0 0 0 0 0		7 TN 3 0 0 10p 10p 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p 0 0	Cc PI Mean ∯50 10p 74,2064p 22,8232p 23,0993p 0 0	Run ombined Er Std Dev 0 6,71f 3,616f 3,582f 0 0	Ibit rror CAP SNR (bit) Inf 10,54 11,43 11,45 Inf Inf Inf
# 0 1 2 3 4 5 6	Name CO/Cref C1/Cref C2/Cref C3/Cref C3/Cref C3/Cref C3/Cref C5/Cref PT1/Ref	Results 0800005E 3B5DEA4B 12418816 127A20FD 00000000 00000000 00000000	Filter none none none none none none	DP_EXT	fpp -27 -27 -27 -27 -27 -27 -24 -24 -24 -24	Factor 10p 10p 10p 10p 10p	7 C_G_01 2,0 pF C_G_01 x 1,00 0 0 0 0 0 0 0 0 0 0 0 0		7 TN 3 0 0 5pan 10p 10p 10p 10p 10p 10p	Final Result 10p 74,2086p 22,82p 23,0963p 0 0 0	Cc PI Mean ‡50 10p 74,2064p 22,8232p 23,0993p 0 0 0 0	Run ombined Er Std Dev 0 6,71f 3,616f 3,582f 0 0	Ibit rror CAP SNR (bit) Inf 10,54 11,43 11,45 Inf Inf Inf Inf Inf

Figure 17 Misc. page

Options on 'Misc.' Page:

LF Clock

OLF_CTUNE	Coarse-tune the low frequency clock. (10kHz, 50kHz, 100kHz, 200kHz)
OLF_FTUNE	Fine-tune the low frequency clock. (015)

HF Clock

OX_RUN	Controls the permanency or the latency of the OX generator. Latency means an
	oscillator settling time before a measurement starts.