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TELEDYNE LECROY
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QPHY-DDR2
DDR2 Serial Data
Operator's Manual

Revision A – December, 2014

Relating to the Following Release Versions:

- **Software Option Rev. 5.9**
- **DDR2 Script Rev. 1.0**
- **Style Sheet Rev. 1.2**

700 Chestnut Ridge Road
Chestnut Ridge, NY, 10977-6499
Tel: (845) 578-6020, Fax: (845) 578 5985
teledynelecroy.com

922536 Rev A
December, 2014

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INTRODUCTION TO QPHY-DDR2

QPHY-DDR2 is an automated test package performing all of the real time oscilloscope tests for Double Data Rate in accordance with JEDEC Standard No. 79-2E. The software can be run on the LeCroy SDA/DDA/WavePro 740Zi and 760Zi and all SDA/DDA/WaveMaster 8Zi oscilloscopes.

Required equipment

- SDA/DDA/WavePro 740/760Zi or SDA/DDA/WaveMaster 8Zi oscilloscope
- Four D620 Probes with WL-Plink Prolink probe body
- Alternatively, D610 probes may be used if the voltage swing of the signal is within +/- 2.5Vp-p.
- TF-DSQ Probe Deskew and Calibration Fixture (not needed if using a Zi oscilloscope)

SIGNALS MEASURED

The compliance test requires probing the following signals (# is the negative polarity of the differential signal):

CK, CK# Input

Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output (read) data is referenced to the crossings of CK and CK# (both directions of crossing).

DQ Input/Output

Data Input/Output: Bi-directional data bus.

DQS, DQS# Input/Output

Data Strobe: output with read data, input with write data. This signal is in phase with read data and 90 degrees out of phase with write data. The data strobes DQS may be used in single ended mode or paired with optional complementary signal DQS# to provide differential pair signaling to the system during both reads and writes.

ADD/CTRL

In addition to the Clock, Data and Strobe signals, address and control signals can also be measured. Bank Address (BA0 – BA2), Chip Select (CS), Command Inputs (RAS, CAS and WE), Clock Enable (CKE) and On Die Termination (ODT) can all be specified as the signal under test.

BASIC FUNCTIONALITY

The functionality is extracted from JEDEC Standard No. 79-2E section 3.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command.

Prior to normal operation, the DDR2 SDRAM must be initialized.

Burst Read

The Burst Read command is initiated by having CS# and CAS# LOW while holding RAS# and WE# HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner.

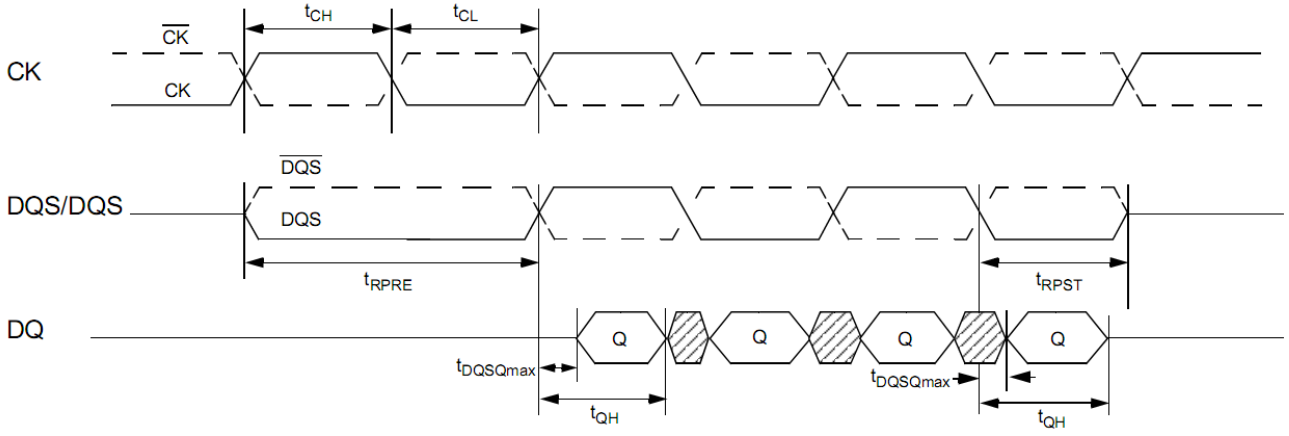


Figure 1. Data output (read) timing [JESD79-2E figure 32]

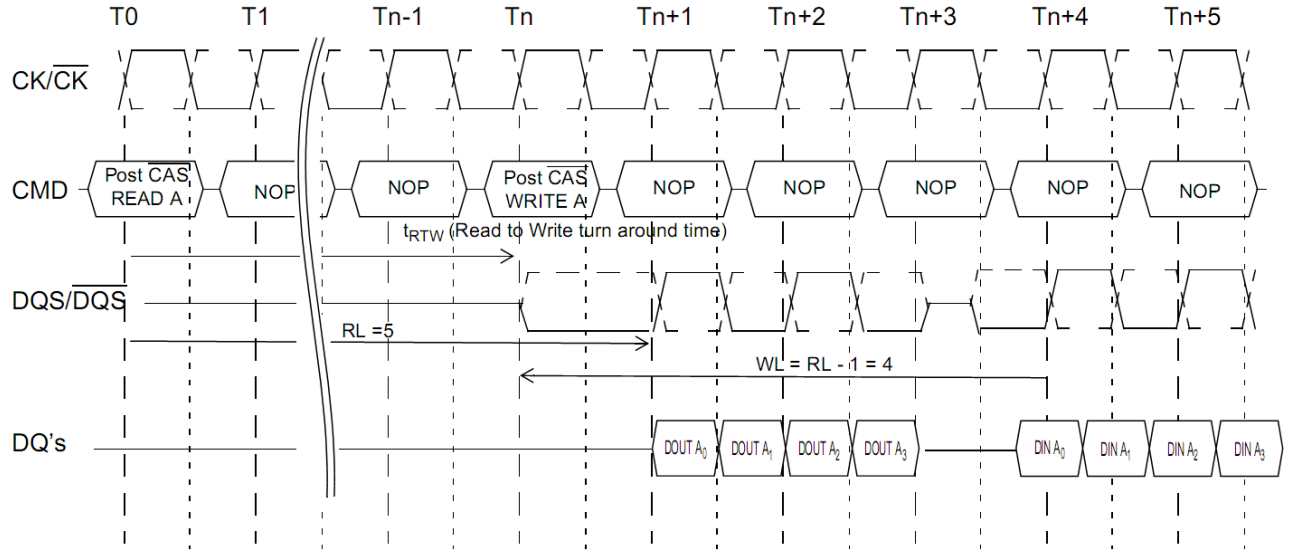


Figure 2. Burst read followed by burst write [JESD79-2E figure 35]

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Burst Write

The Burst Write command is initiated by having CS#, CAS# and WE# LOW while holding RAS# HIGH at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) nominally half clock prior to the [first rising edge]. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst.

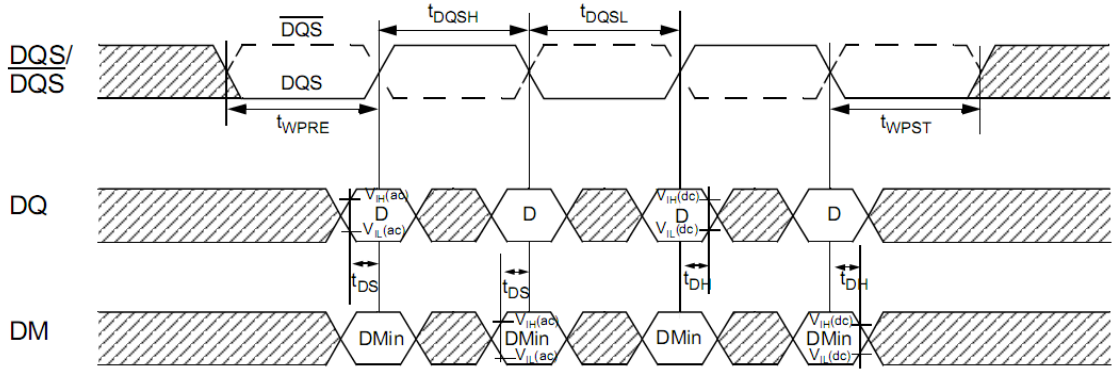


Figure 3. Data input (write) timing [JESD79-2E figure 38]

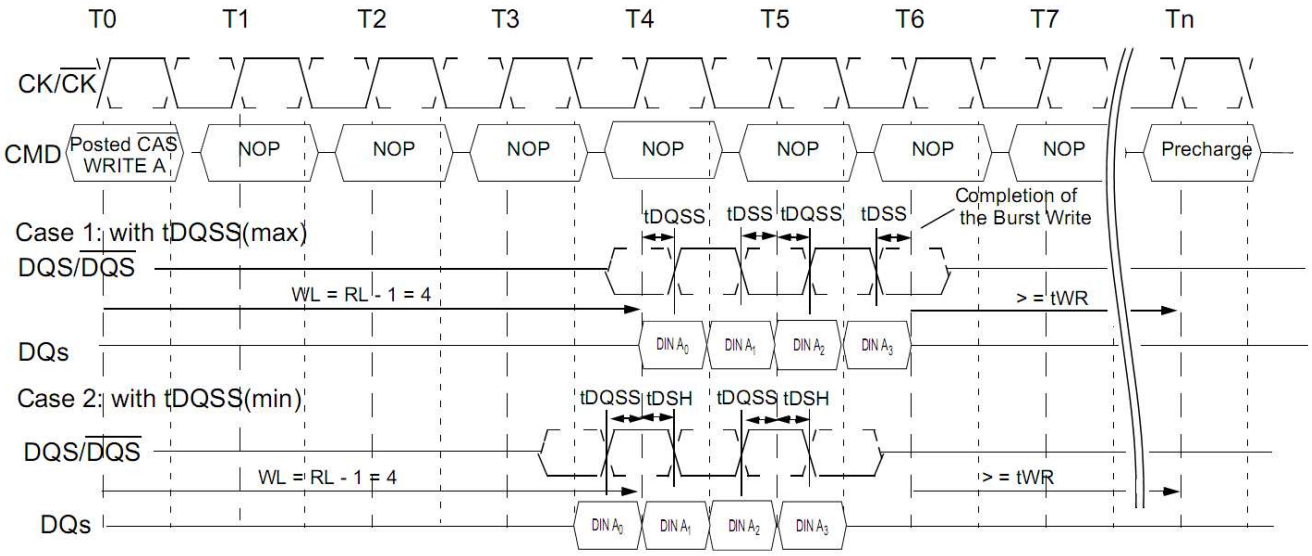
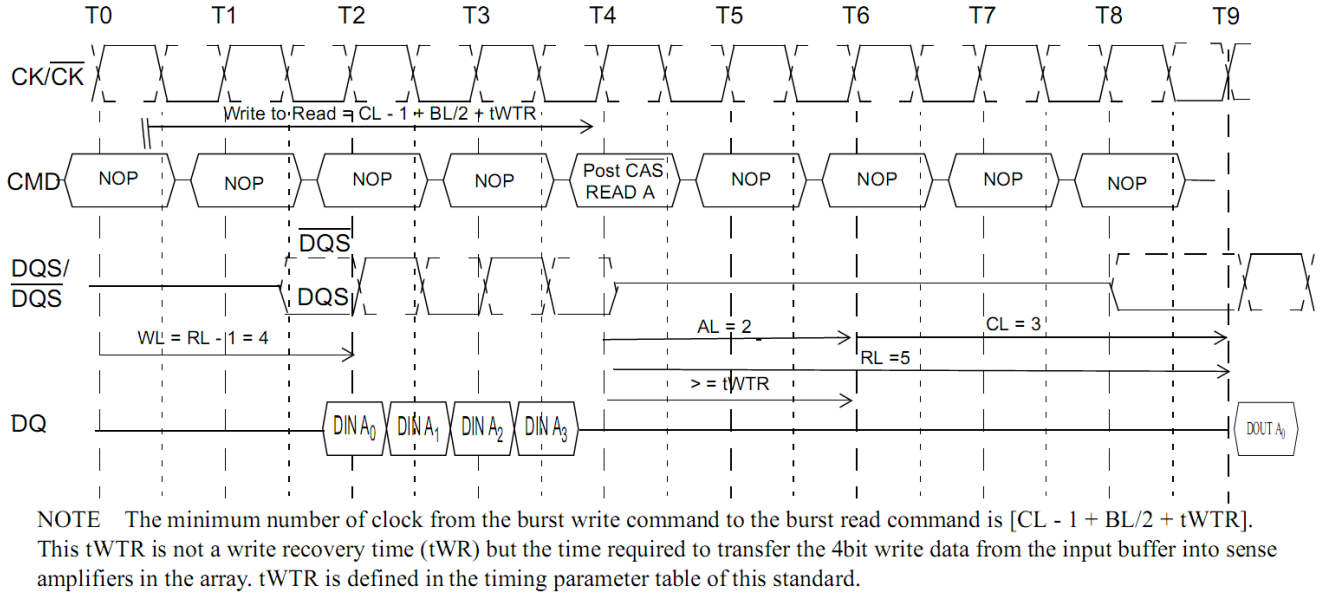


Figure 4. Burst write operation [JESD79-2E figure 39]



NOTE The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in the timing parameter table of this standard.

Figure 5. Burst write followed by burst read [JESD79-2E figure 41]

USING QUALIPHY DDR2

QualiPHY DDR2 guides the user, step-by-step, through each of the source tests described in JEDEC Standard No. 79-2E. To do this, the user must setup a test session.

Users choose test configurations to run. There are several pre-loaded test configurations including:

- **1) Clock tests DDR2-667 (1 Probe)**
- **2) CKdiff-DQse-DQSdiff 667 Write Burst (3 probes)**
- **3) CKdiff-DQse-DQSdiff 667 Read Burst (3 probes)**
- **4) Eye Diagram (3 Probes Debug)**
- **5) All tests that require 4 Probes**
- **D1) Demo of All Clock tests**
- **D2) Demo of Eye Diagram (Debug)**
- **D3) Demo of All tests**
- **D4) Demo of All Ck-diff-DQSdiff-DQse tests**

The pre-loaded configurations provide quick and easy ways to begin compliance testing. You can create your own custom configurations (see the **Customizing QualiPHY** topic for details).

The variables are pre-loaded with the standard settings for compliance testing; however, the user may choose to create their own configuration with the variables set as desired.

QUALIPHY COMPLIANCE TEST PLATFORM

QualiPHY is Teledyne LeCroy's compliance test framework which leads the user through the compliance tests. QualiPHY displays connection diagrams to ensure tests run properly, automates the oscilloscope setup, and generates complete, detailed reports.

The QualiPHY software application automates the test and report generation.

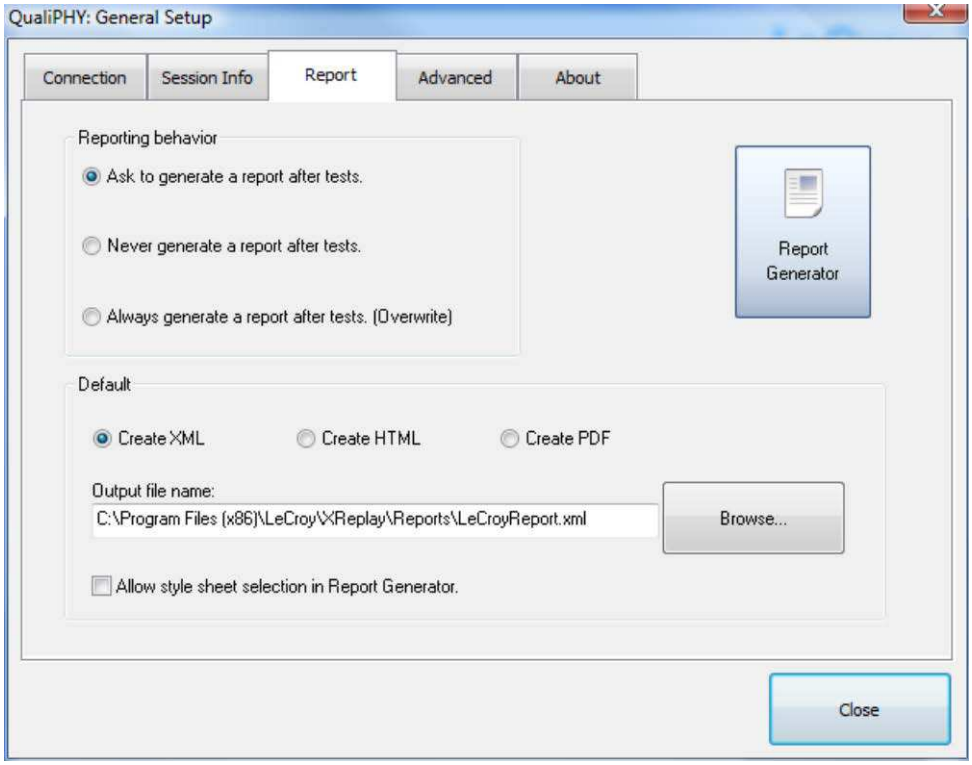


Figure 6. Report menu in QualiPHY General Setup

LeCroy

DDR2 Test Report

Overall result: Pass

DUT:	Demo
Comment:	Example
Time of test:	02/28/2009 02:59:51
Operator:	LeCroy
Temperature	25° C
Configuration in use:	Demo of All tests
Limits in use:	DDR2-667
Standard in use:	DDR2
Oscilloscope Name:	geneva-nb201 Model: WP760Zi
Oscilloscope Serial #:	GENEVA-NB201
Computer:	GENEVA-NB201
Oscilloscope firmware version:	0.5.9.0 (Build 122911)
QualiPHY core version:	0.5.8.0 (Build 122474)
QualiPHY script version:	0.1.3.235
Stylesheet version:	1.2.0.2

Summary Table

[Hide Table]

Pass	Test	Measurement	Current Value	Test Criteria
	Clock	Clock Speed Grade	668.863 MHz	Informational Only
	Clock	tCK(avg), rise	2.991 ns	Informational Only
	Clock	tCK(avg), fall	2.991 ns	Informational Only
✓	Clock	tCK(abs), rise, min	2.934 ns	2.875 ns <= n <= 3.125 ns
✓	Clock	tCK(abs), rise, max	3.031 ns	2.875 ns <= n <= 3.125 ns
✓	Clock	tCK(abs), fall, min	2.932 ns	2.875 ns <= n <= 3.125 ns
✓	Clock	tCK(abs), fall, max	3.040 ns	2.875 ns <= n <= 3.125 ns
✓	Clock	tCH(avg)	505.4 mtCK(avg)	480.0 mtCK(avg) <= n <= 520.0 mtCK(avg)
✓	Clock	tCL(avg)	494.5 mtCK(avg)	480.0 mtCK(avg) <= n <= 520.0 mtCK(avg)
✓	Clock	tCH(abs), min	1.462 ns	1.315 ns <= n <= 1.685 ns
✓	Clock	tCH(abs), max	1.556 ns	1.315 ns <= n <= 1.685 ns
✓	Clock	tCL(abs), min	1.427 ns	1.315 ns <= n <= 1.685 ns
✓	Clock	tCL(abs), max	1.517 ns	1.315 ns <= n <= 1.685 ns
✓	Clock	tJIT(duty), min	-52 ps	-125 ps <= n <= 125 ps
✓	Clock	tJIT(duty), max	45 ps	-125 ps <= n <= 125 ps
✓	Clock	tJIT(per)rise, min	-57 ps	-125 ps <= n <= 125 ps

QualiPHY

✓	Timing	tAC Min	29 ps	>= -450 ps
✓	Timing	tDS(base) min	567 ps	>= 100 ps
ℹ	Clock	Clock Speed Grade	668.868 MHz	Informational Only
✓	Timing	tDS1(base) min	486 ps	>= -25 ps

Details

PROBE SETUP: CKdiff-DQse-DQSdiff

Clock Tests

[Up]

Measurement:	***Clock Speed Grade***
Limit Name:	InfoOnlyMHz
Current Value:	668.863 MHz
Test Criteria:	Informational Only
Timestamp:	02/28/2009 02:59:04
Description:	Check that Clock has the expected frequency

Clock Frequency
Timestamp: 02/28/2009 02:59:05

[Up]

Pass

Measurement:	***tJIT(per)rise, min***
Limit Name:	tJIT(per)_limit
Current Value:	-57 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:11
Description:	Clock Period Jitter, rising edge, min

[Up]

Pass

Measurement:	***tJIT(per)rise, max***
Limit Name:	tJIT(per)_limit
Current Value:	41 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:11
Description:	Clock Period Jitter, rising edge, max

Test Timing - tDS(base) min: DQ10 VIH/VIL(ac) to DQS1 VREF
Timestamp: 02/28/2009 03:02:35

[Up]

Pass

Measurement:	***tJIT(per)fall, min***
Limit Name:	tJIT(per)_limit
Current Value:	-59 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:11
Description:	Clock Period Jitter, falling edge, min

[Up]

Pass

Measurement:	***tJIT(per)fall, max***
Limit Name:	tJIT(per)_limit
Current Value:	59 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:12
Description:	Clock Period Jitter, falling edge, max

[Up]

Pass

Measurement:	***tJIT(cc)rise***
Limit Name:	tJIT(cc)_limit_abs
Current Value:	84 ps
Test Criteria:	<= 250 ps
Timestamp:	02/28/2009 02:59:12
Description:	Cycle to Cycle Period Jitter, rising edge

[Up]

Pass

Measurement:	***tJIT(cc)fall***
Limit Name:	tJIT(cc)_limit_abs
Current Value:	102 ps
Test Criteria:	<= 250 ps
Timestamp:	02/28/2009 02:59:12
Description:	Cycle to Cycle Period Jitter, falling edge

[Up]

Measurement:	***Number of Clock Cycles***
Limit Name:	InfoOnly
Current Value:	200
Test Criteria:	Informational Only
Timestamp:	02/28/2009 02:59:12
Description:	200 clock cycles are required for compliance test

[Up]

Pass

Measurement:	***tDS1(base) min***
Limit Name:	tDS1(base)_min
Current Value:	486 ps
Test Criteria:	>= -25 ps
Timestamp:	02/28/2009 03:02:54
Description:	DQ and DM Input Setup Time

Test Timing - tDS1(base) min: DQ10 VIH/VIL(ac) to DQS1p VIH/VIL(dc) and DQS1n VIH/VIL(dc)
Timestamp: 02/28/2009 03:02:55

Figure 7. The Test Report includes a summary table with links to the detailed test results

Oscilloscope Option Key Installation

An option key must be purchased to enable the QPHY-DDR2 option. Call Teledyne LeCroy Customer Support to place an order and receive the code.

Enter the key and enable the purchased option as follows:

1. From the oscilloscope menu select **Utilities → Utilities Setup**
2. Select the **Options** tab and click the **Add Key** button.
3. Enter the **Key Code** using the on-screen keyboard.
4. Restart the oscilloscope to activate the option after installation.

Typical (Recommended) Configuration

QualiPHY software can be executed from the oscilloscope or a host computer. The first step is to install QualiPHY.

Teledyne LeCroy recommends running QualiPHY on an oscilloscope equipped with Dual Monitor Display capability (Option DMD-1 for oscilloscopes where this is not standard). This allows the waveform and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

By default, the oscilloscope appears as a local host when QualiPHY is executed in the oscilloscope. Follow the steps under **Oscilloscope Selection** (as follows) and check that the IP address is 127.0.0.1.

Remote (Network) Configuration

It is also possible to install and run QualiPHY on a host computer, controlling the oscilloscope with a Network/LAN Connection.

The oscilloscope must already be configured, and an IP address (fixed or network-assigned) must already be established.

Oscilloscope Selection

Set up the oscilloscope using QualiPHY over a LAN (Local Area Network) by doing the following:

1. Make sure the host computer is connected to the same LAN as the oscilloscope. If unsure, contact your system administrator.
2. From the oscilloscope menu, select **Utilities → Utilities Setup**
3. Select the **Remote** tab.
4. Verify the oscilloscope has an IP address and the control is set to TCP/IP.
5. Run QualiPHY in the host computer and click the **General Setup** button.
6. Select the **Connection** tab.
7. Enter the IP address from step 4 (previous).
8. Click the **Close** button.

QualiPHY is now ready to control the oscilloscope.

QualiPHY tests the oscilloscope connection after clicking the **Start** button. The system prompts you if there is a connection problem. QualiPHY's **Scope Selector** function can also be used to verify the connection.

Accessing the QPHY-DDR2 Software using QualiPHY

This topic provides a basic overview of QualiPHY's capabilities.

Access the QPHY-DDR2 software using the following steps:

1. Wait for the oscilloscope to start and have its main application running.
2. Launch QualiPHY from the **Analysis** menu if installed on the oscilloscope or from the desktop icon if installed on a host computer.
3. From the QualiPHY main window (as follows), select **Standard**, then **DDR2** from the pop-up menu (if not already selected). If you check the **Pause on Failure** box (circled) QualiPHY prompts to retry the test in the case of a failure.

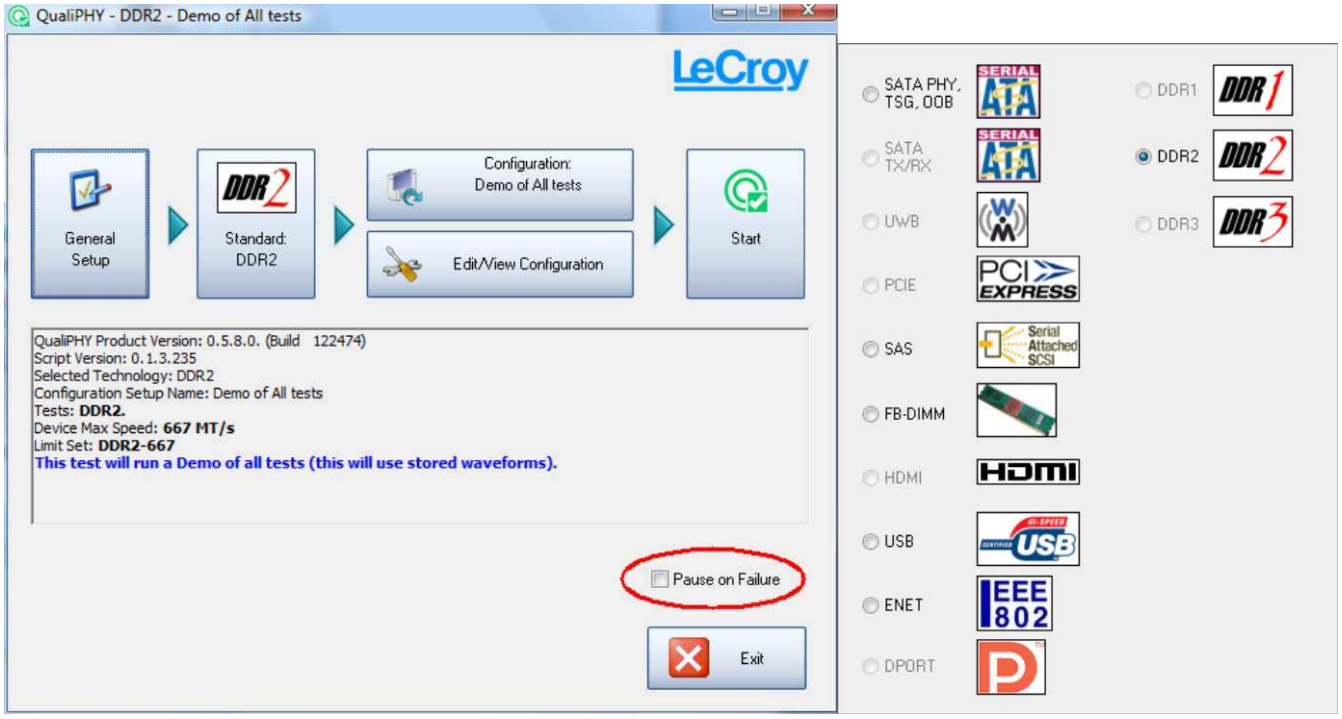


Figure 8. QualiPHY main menu and compliance test Standard selection menu

4. Click the **Configuration** button in the QualiPHY main menu:

5. Select a configuration from the pop-up menu:

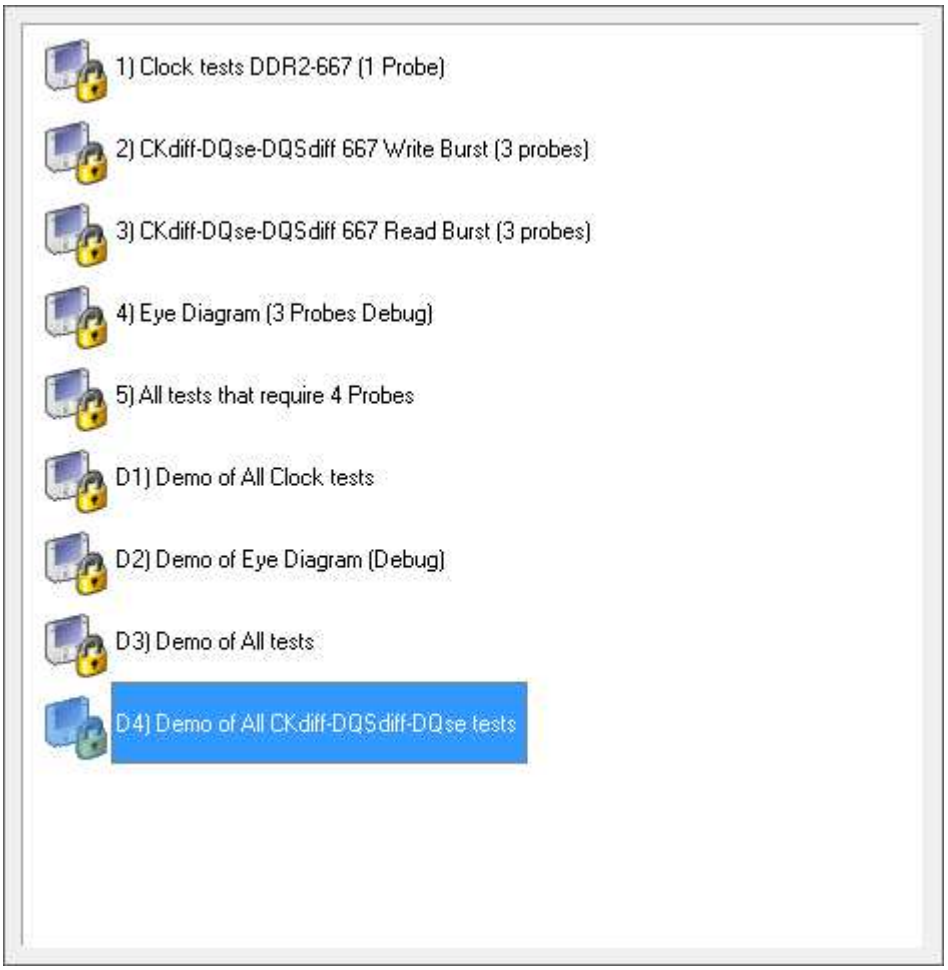


Figure 9. QualiPHY configuration selection menu

6. Click **Start**.

7. Follow the pop-up window prompts.

Customizing QualiPHY

The predefined configurations in the **Configuration** screen cannot be modified. However, you can create your own test configurations by copying one of the standard test configurations and making modifications. A description of the test is also shown in the description field when selected.

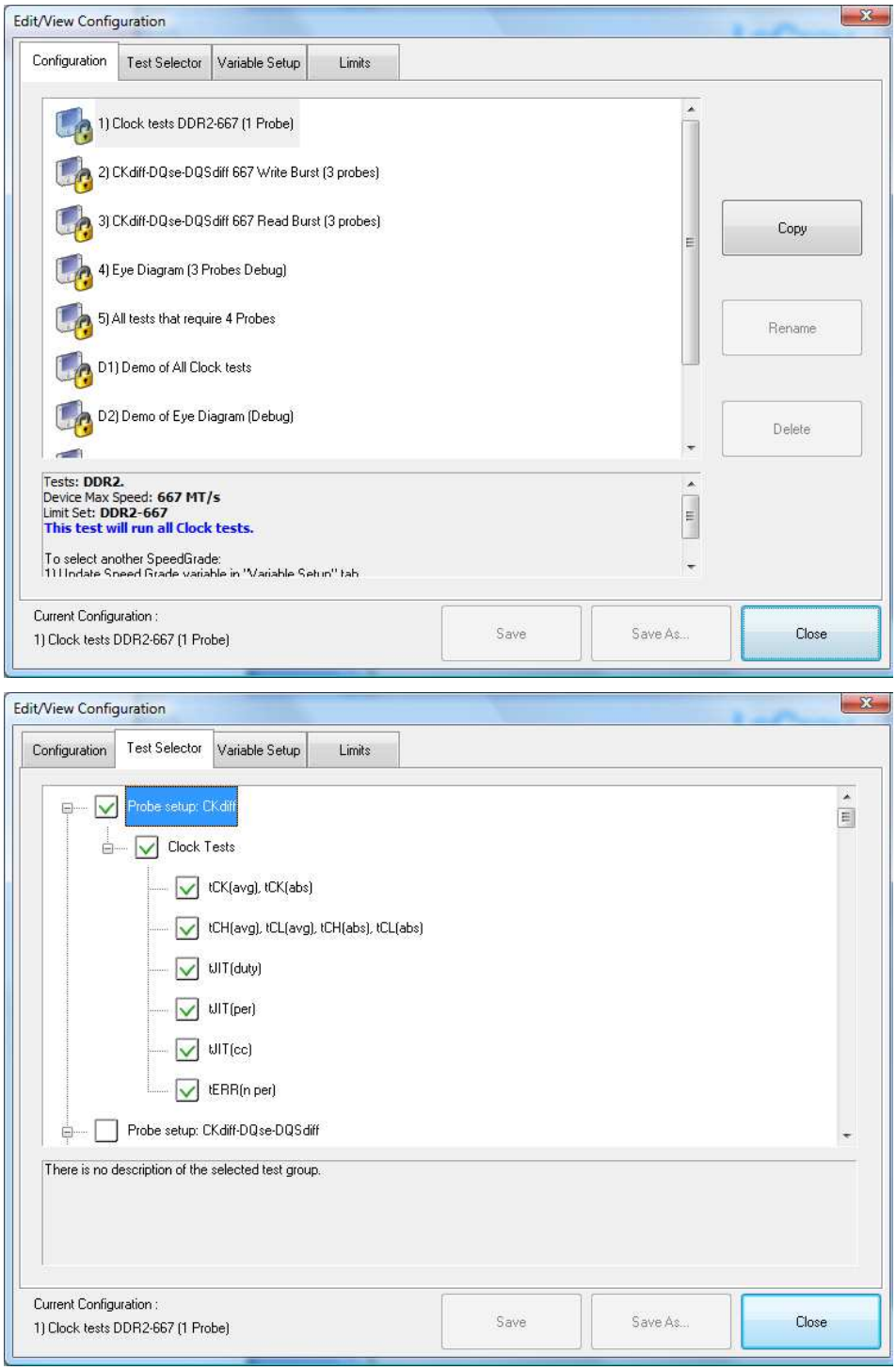


Figure 10. QualiPHY test item selection menu

Once a custom configuration is defined, script variables and the test limits can be changed by using the **Variable Setup** and **Limits Manager** from the **Edit/View Configuration** window.

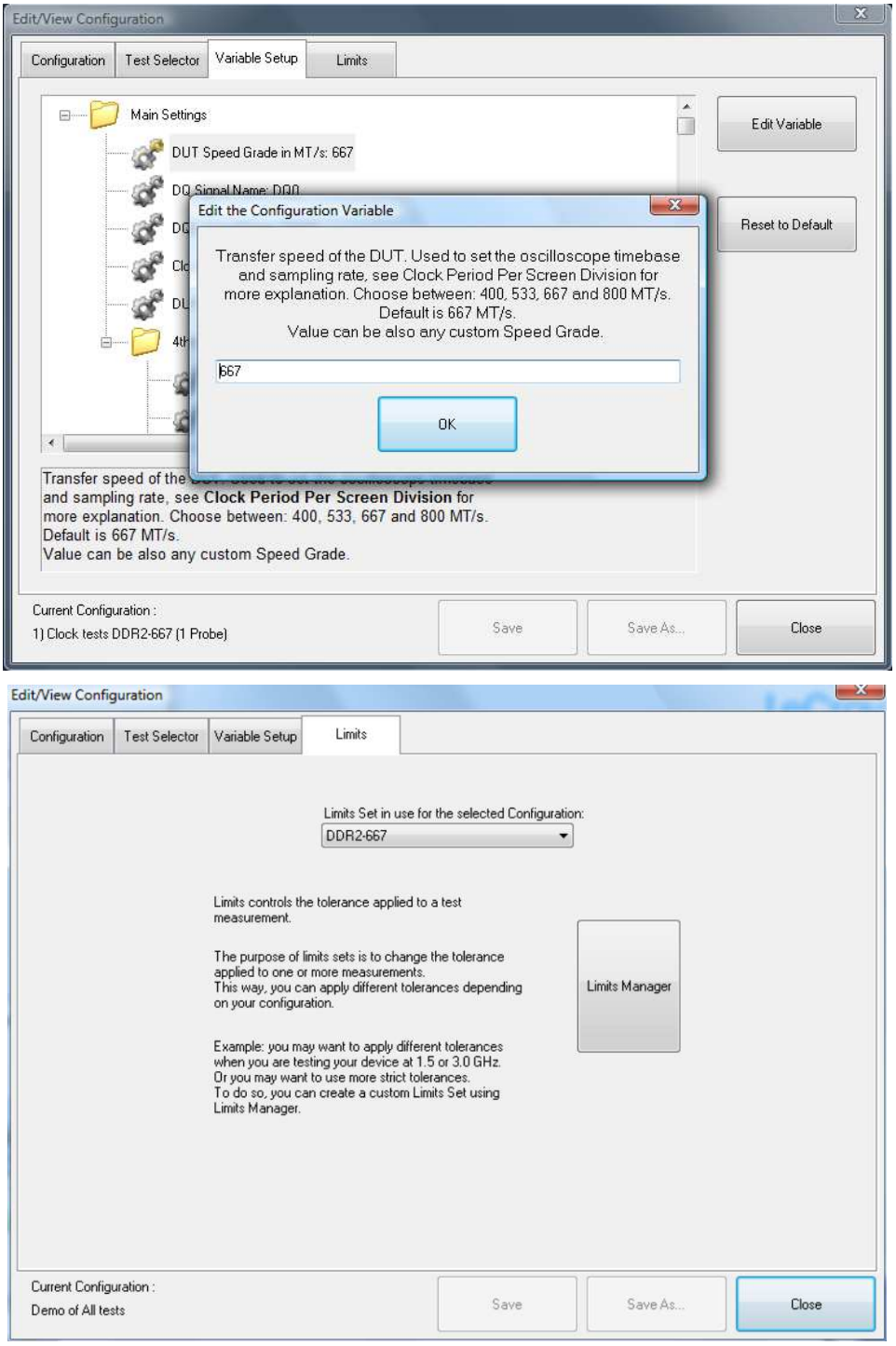


Figure 11. Variable Setup and Limits Manager windows

QPHY-DDR2 Operation

After pressing **Start** in the QualiPHY menu, the software instructs how to set up the test using pop-up connection diagrams and dialog boxes.

Figure 12. Start button

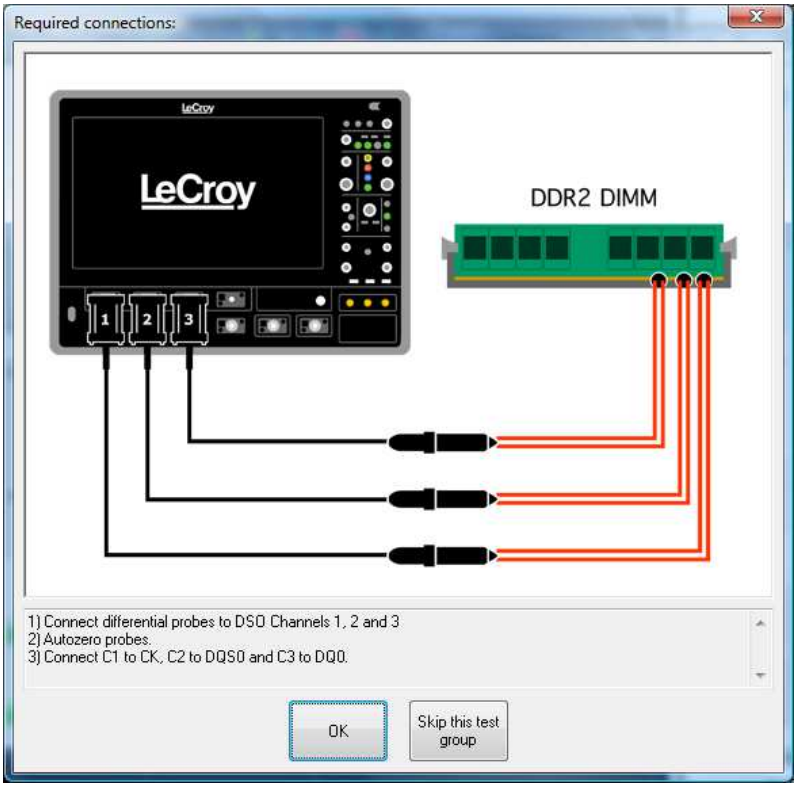


Figure 13. Example of pop-up connection diagram and dialog box

DDR2 MEASUREMENT PREPARATION

Before starting any test or data acquisition, the oscilloscope must be warmed for at least 20 minutes. Calibration is automatic under software control and no manual calibration is required. The procedure should be run again if the temperature of the oscilloscope changes by more than a few degrees.

Differential Probe Deskew Procedure using TF-DSQ

Note: Another procedure can be used for Zi oscilloscopes, refer to the next section for details.

Follow the procedure described in the TF-DSQ Probe Deskew and Calibration Fixture manual. Deskew all four channels with their respective probe, using external trigger (AUX IN) as reference signal.

You can get more information on TF-DSQ using the oscilloscope Help menu and searching for Probe Calibration. There is also a section on Deskew Theory of Operation.

Differential Probe Deskew Procedure on Zi oscilloscopes using PCF200

Use the PCF200 Characterization Fixture provided as standard accessory with WaveLink series probes. The fixture determines the effect of probe input loading on the circuit under test and the probe response to the signal being measured, using the AT, ST, Dx10, and Dx20 modules with SI, or SP, or QC (QC for WL-Plink only) interconnect leads.

Probe calibration is accomplished with the PCF200 fixture by following the basic steps in the following flowchart. It is recommended that you read the instructions presented here in their entirety to familiarize yourself with the advanced features of the PCF200 fixture.

Connecting probes to the circuit under test can be a difficult procedure. With this in mind, Teledyne LeCroy's system is designed in a manner that allows you to set up the probe calibration fixture, calibrate each individual probe once, connect your probes to the circuit, and disconnects the fixture. Once your probes are in the circuit, there is no need to revisit the fixture until the next calibration interval.

You should familiarize yourself with the following topics:

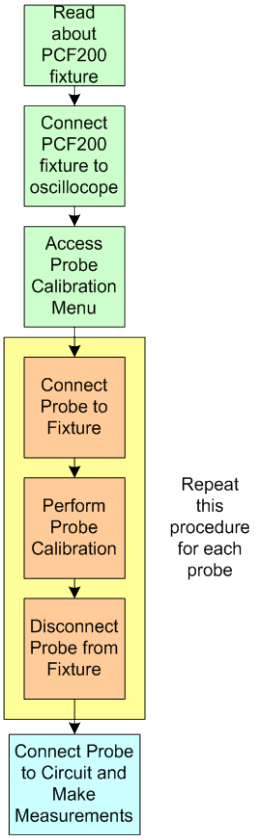
-

PCF200 Fixture Overview

- **Probe Connection to PCF200**
- **Probe Calibration Menu**
- **D620 Probe Calibration**

Advanced mode is available:

- **Advanced Mode Probe Calibration Menu**
- **Advanced Probe Calibration**



Connecting probes to the circuit under test can be a difficult procedure. With this in mind, Teledyne LeCroy's system is designed in a manner that allows you to set up the probe calibration fixture, calibrate each individual probe once, connect your probes to the circuit, and disconnect the fixture. Once your probes are in the circuit, there is no need to revisit the fixture until the next calibration interval.

You should familiarize yourself with the following topics:

- **PCF200 Fixture** Overview
- **Probe Connection to PCF200**
- **Probe Calibration Menu**
- **D620 Probe Calibration**

Advanced mode is available:

- **Advanced Mode Probe Calibration Menu**
- **Advanced Probe Calibration**

PCF200 Fixture Overview

Major components of the PCF200 fixture are shown in the following figure:

- SMA male connector Fast Edge input.
- SMA female connector output to AUX IN for 50-ohm termination.
- Clip for connection of Solder-In probes.
- 2-pins header for connection of Square-Pin probes.

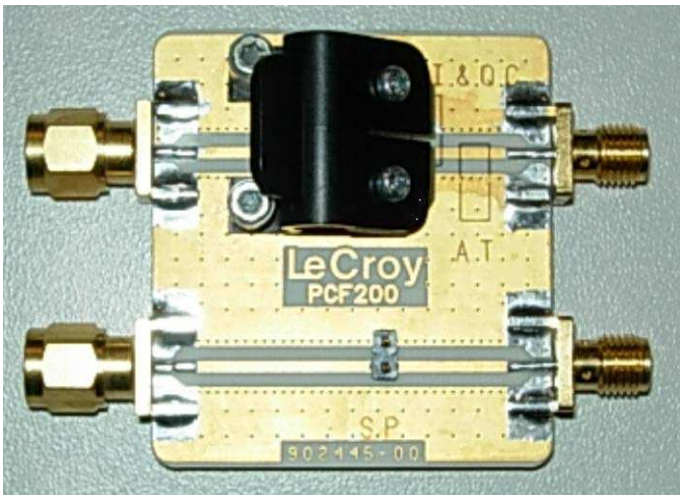


Figure 14. PCF200 Deskew Fixture

A SMA male to BNC male 50-ohm cable is required to perform the calibration.

System assembly is accomplished in the following steps:

1. Connect the BNC end of the 50 Ohm cable to the oscilloscope AUX IN.
2. Connect the SMA end of the 50 Ohm cable to the SMA female connector on the PCF200 fixture.
3. Connect the PCF200 SMA male connector to the oscilloscope Fast Edge SMA output.

The SMA connections should be torqued with an RF torque wrench and must be properly tightened.

Probe Connection to PCF200

The PCF200 provides multiple probe connectors for various kinds of probes. There are 2 circuits depending on the type of probes to calibrate:

- The upper circuit is for Solder-In (SI) and Quick-Connect (QC) probes. This circuit can also be used for AT probes using the designated area to apply the probe tips.
- The lower circuit is for Square-Pin (SP) probes.

Probes are connected electrically in a single-ended arrangement: the positive (+) side of the probe must be connected to the signal trace, while the negative (-) side is connected to the ground plane.

Figure 15. Differential probe properly connected to the fixture (Solder-In configuration)

Probe Calibration Menu

The probe calibration menu can be accessed from the Vertical drop-down menu or from the channel dialog:

Figure 16. Accessing the probe calibration menu

Figure 17. Basic Probes Calibration menu

The information in the probe calibration menu is organized such that each row represents the information for a given channel, and each column represents the calibration information or control for that channel. For each channel, the information and control provided includes:

- The channel number in the colored button icon and the probe type that is installed.
- A **Full Calibration** button, which starts the calibration. Use only with TF-DSQ. DO NOT use with PCF200.
- DC correction information including both gain and offset correction.
- The skew correction.
- A **Clear** button.

Probe

This area shows the type of probe connected to the channel. All other information shown in a given row is associated with that probe.

Full Calibration Button

This button causes the oscilloscope to automatically perform a full DC and deskew calibration. See details of DC Calibration Theory of Operation and Deskew Theory of Operation in TF-DSQ Operation Manual. Use only with TF-DSQ. DO NOT use with PCF200.

Gain & Offset

These fields show the gain and offset applied to the probe. If the probe measures a voltage of V, the new, calibrated voltage is:

$$V_{calibrated} = V \cdot Gain + Offset$$

Note that the offset is in Volts, and the gain is unitless.

The probe DC calibration information can be entered either manually or as the result of an automatic calibration. In the case of automatic calibration, it can be part of the full calibration or it can be a standalone DC calibration executed in advanced mode. When the DC calibration information is a result of an automatic calibration utilizing the TF-DSQ fixture, the information shown is the gain and offset utilized for the currently configured channel sensitivity (volt/division setting; see details of DC Calibration Theory of Operation in the TF-DSQ Operator's Manual on the Teledyne LeCroy website for details). In this case, when the channel sensitivity is altered these values change. **When the DC calibration information is entered manually, it clears any automatic results and replaces them globally with the newly entered values. This means that if new gain and offset numbers are entered manually, these values apply across all sensitivity oscilloscope settings.**

The gain is limited to between 0.8 and 1.2, but the offset is not limited.

Note: It is important to note that some passive probes, and any user-designed probes, do not provide proper probe identification information to the oscilloscope. In these cases, the oscilloscope may not be able to determine the proper attenuation values and you should make sure that the proper attenuation is entered from the channel's **Vertical** setup dialog. Furthermore, the gain entered should be the gain *correction* applied to the system with the correctly entered attenuation.

If used with PCF200, enter values manually.

Skew

This field shows the measured skew between the probe in the specified channel and the reference channel. This can be entered manually or as the result of an automatic calibration. In the case of automatic calibration, it can be the result of a portion of the full calibration or it can be the result of a standalone deskew calibration. Even after the deskew has been performed automatically, the deskew correction can be adjusted manually.

Clear

All probe calibrations can be cleared by pressing this button corresponding to a specific probe.

Calibration Source

This field specifies the signal source used for DC calibrations. When using the PCF200 fixture, specify AUX OUT as the calibration source (even if the PCF200 is connected to Fast Edge output). This signal is not used for deskew.

Calibration Skew Reference

These values specify the channel or external input where the skew reference is supplied. The skew reference is the absolute time reference to which all deskew measurements are made. When the PCF200 fixture is used, select the EXT input.

Recall Calibration

Whenever a probe calibration is applied, the oscilloscope saves the information in a file on the disk. If the oscilloscope must be rebooted for any reason, the probe calibration information is always cleared, but can be manually recalled by pressing this button.

Advanced Mode Checkbox

When the **Advanced Mode** checkbox is unchecked, you have access to the basic probe calibration menu. The basic probe calibration menu shows you only what is absolutely needed to perform a simple calibration of the probes. In other words, it shows you the calibration information and provides the capability to calibrate the probe with a single button press, clear the calibration information, and manually reload the calibration information following an oscilloscope reboot. When the advanced mode button is checked, you have access to the advanced mode probe calibration menu.

This checkbox must be checked for deskew calibration using PCF200.

Advanced Mode Probe Calibration Menu

The advanced mode is entered by checking the advanced mode box in the basic probe calibration menu.

Figure 18. Advanced Mode Probe Calibration menu

Checking this box allows:

- Calibration of gain/offset only
- Calibration of deskew only
- Access to the advanced menu (shown as a tab behind the "Probes Cal" dialog)

Gain/Offset Only

Pressing this button performs only the DC calibration of the probe on the specified channel. See details of DC Calibration Theory of Operation in TF-DSQ Operation Manual. DO NOT use with PCF200 connected to Fast Edge output.

Deskew Only

Pressing this button performs only the deskew calibration of the probe on the specified channel. See details of Deskew Theory of Operation in TF-DSQ Operation Manual.

This is the button to use with PCF200 connected to Fast Edge output.

The Advanced Menu

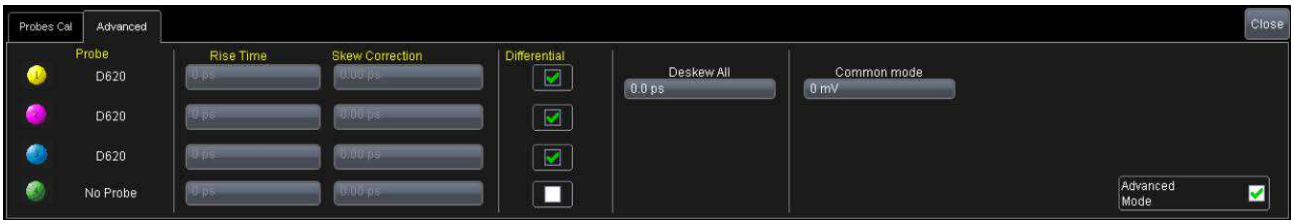


Figure 19. Probes Calibration menu Advanced tab

The Advanced Menu contains information and functionality useful to the advanced user of the PCF200 fixture. These include:

- Rise Time Skew Correction
- Differential(or Single-Ended) probe selection
- Deskew All (or common deskew capability)
- Common mode voltage settings for DC calibration

Rise Time Skew Correction

This field shows the signal risetime and the corresponding skew correction based on the signal risetime.

When probes are deskewed, the risetime measurement of the edge used for deskewing is displayed in the **Rise Time** field corresponding to the probe and probe channel, and an additional skew correction of zero is applied.

The measured risetime of the signals encountered can be entered into the **Rise Time** field, and the oscilloscope automatically calculates and applies a new skew correction value to be utilized in addition to the deskew amount calculated during the deskew calibration procedure. With this use, a finer deskew calibration is performed because the risetimes of the signals measured are now taken into account. Refer to the Deskew Risetime Adjustment Theory of Operation in the TF-DSQ Operator's Manual on the Teledyne LeCroy website for details.