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PCF2113x

LCD controllers/drivers

Rev. 04 — 4 March 2008 Product data sheet

1. General description

The PCF2113x is a low-power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 lines of 12 characters or 1 line of 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113x interfaces to most microcontrollers via a 4-bit or 8-bit bus or via the 2-wire I^2C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters.

The letter 'x' in PCF2113x characterizes the built-in character set. Various character sets can be manufactured on request.

2. Features

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user-defined symbols
- Icon mode for e.g. additional segment display section: reduced current consumption while displaying icons only
- Icon blink function
- Very low current consumption (20 μA to 200 μA):
  - Icon mode: < 25 μA
  - Power-down mode: < 2 μA
- On-chip:
  - Configurable 4, 3 or 2 voltage multiplier, generating LCD supply voltage V_{LCD}, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V_{LCD}: –0.16 %/K to –0.24 %/K (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters of 5 × 8 dots
- Character generator RAM: 16 characters of 5 × 8 dots; 3 characters used to drive 120 icons, 6 characters used if icon blink feature is used in application
- 4-bit or 8-bit parallel bus and 2-wire I^2C-bus interface
- 18 row and 60 column outputs

- Multiplex rates (MUX) 1:18 (for normal operation), 1:9 (for single-line operation) and 1:2 (for Icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range $V_{DD1} - V_{SS1}$ = 1.8 V to 5.5 V (chip may be driven with two battery cells)
- V_{LCD} generator supply voltage range $V_{DD2} - V_{SS2}$ = 2.2 V to 4.0 V
- Display supply voltage range $V_{LCD} - V_{SS2}$ = 2.2 V to 6.5 V
- Direct mode to save current consumption for Icon mode and MUX 1:9 (depending on V_{DD2} and LCD liquid properties)
- CMOS compatible
- **Remark:** Icon mode is a way to save current. When only icons are displayed (i.e. only the lower two rows are active), a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

3. Applications

- Telecom equipment
- Point-of-sale terminals
- Portable instruments

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2113AU/10/F4	-	chip on flexible film carrier	-
PCF2113DU/F4	-	chip in tray	-
PCF2113DH/4	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
PCF2113DU/2/F4	-	chip with bumps in tray	-
PCF2113EU/2/F4	-	chip with bumps in tray	-
PCF2113WU/2/F4	-	chip with bumps in tray	-

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF2113DH/4	PCF2113DH

6. Block diagram

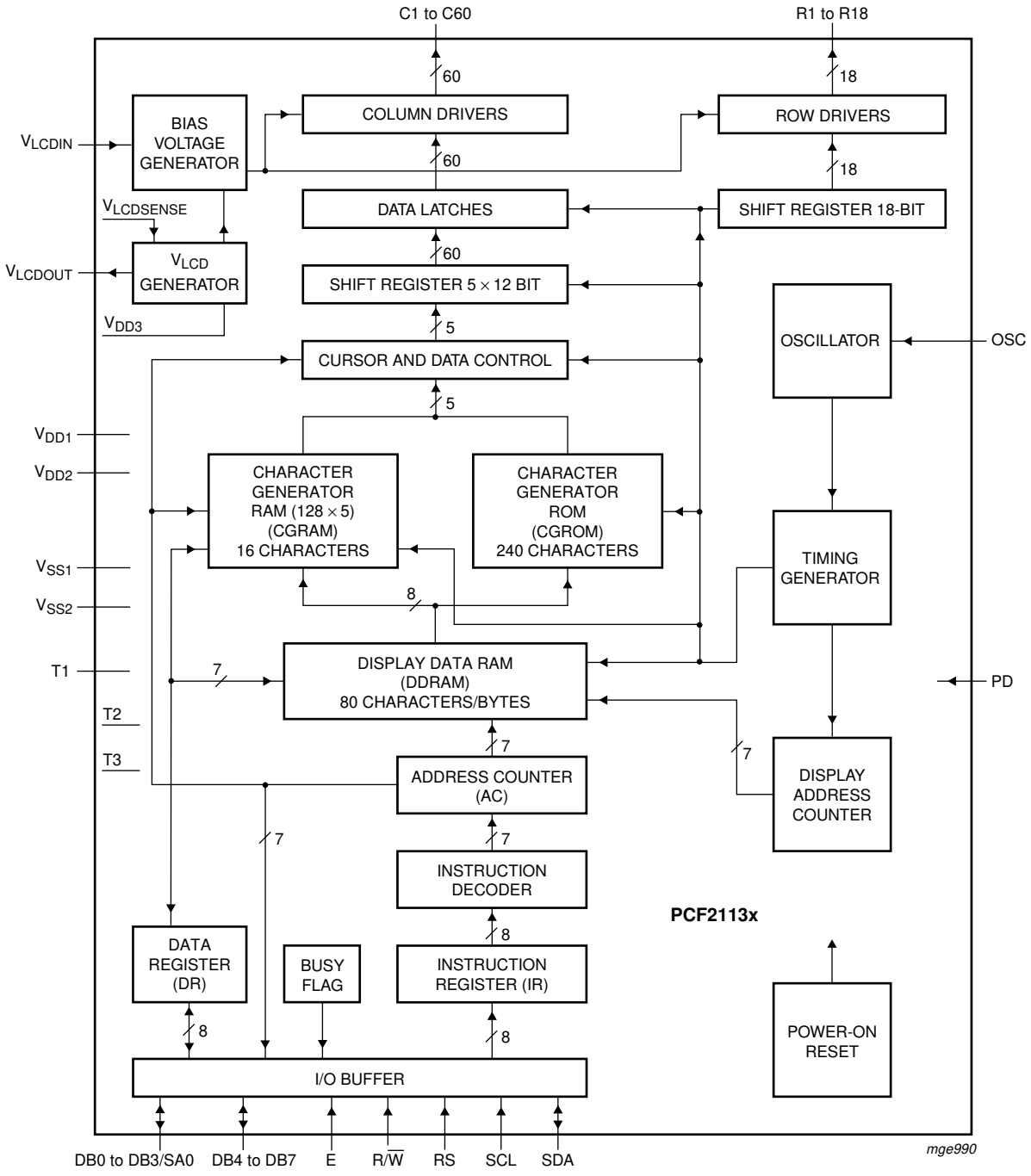


Fig 1. Block diagram of PCF2113x

7. Pinning information

7.1 Pinning

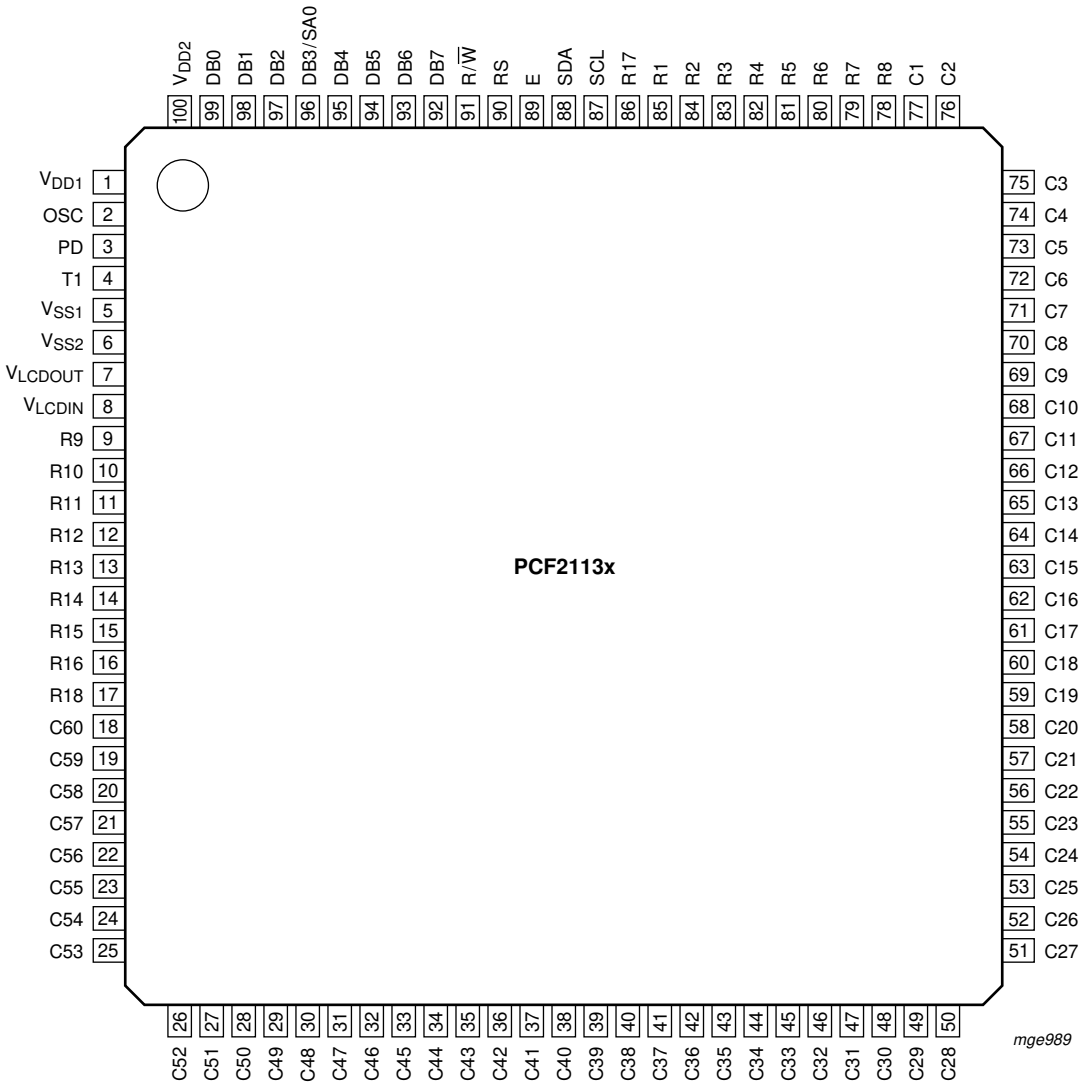


Fig 2. Pin configuration for PCF2113DH (LQFP100)

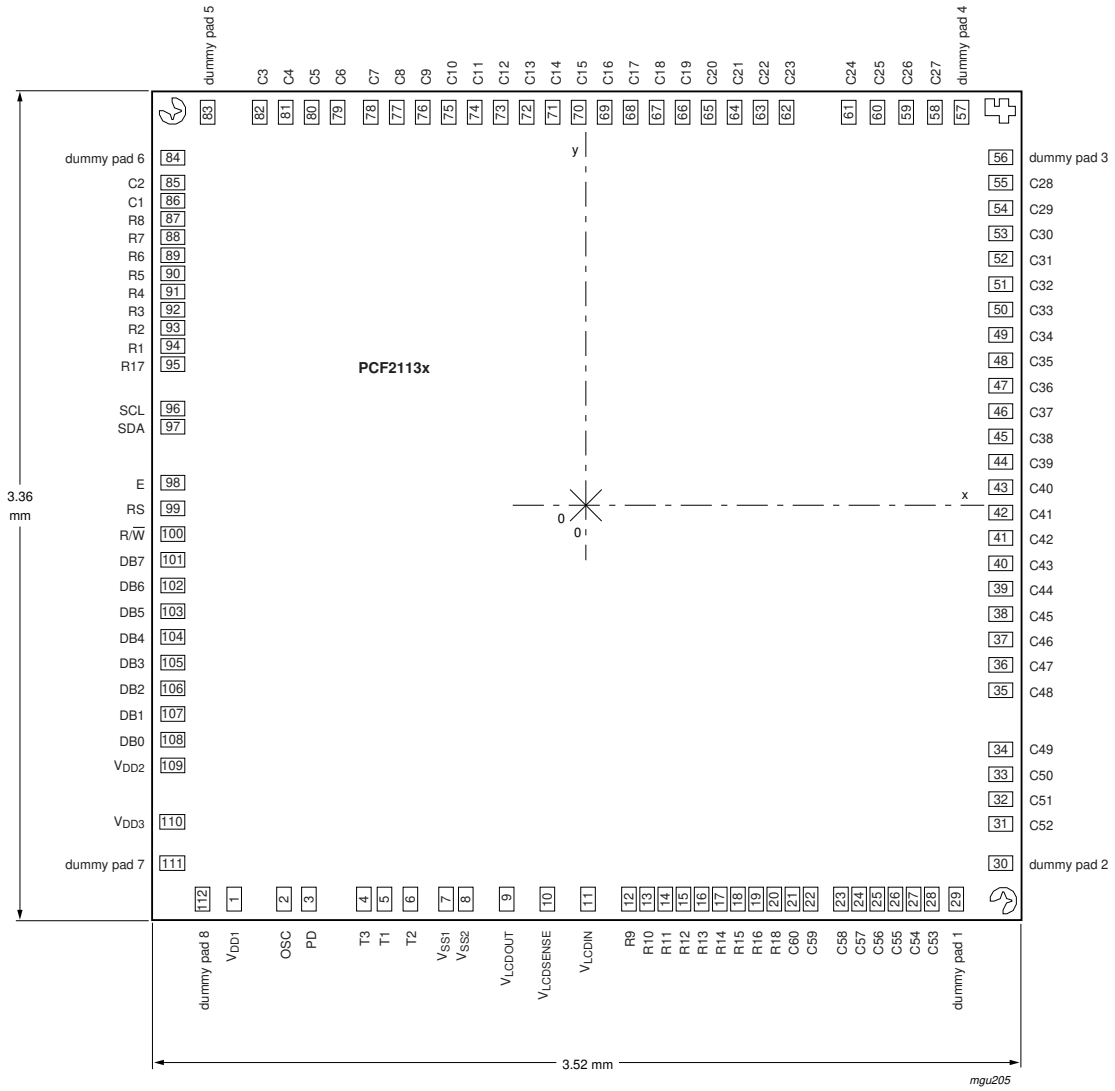


Fig 3. Bonding pad locations for PCF2113xU (bottom view)

Table 3. Pin (LQFP100 package) or pad allocation table

Pin	Pad	Symbol	Pin	Pad	Symbol
1	1	V_{DD1}	-	84	dummy pad
2	2	OSC	76	85	C2
3	3	PD	77	86	C1
-	4	T3	78 to 85	87 to 94	R8 to R1
4	5	T1	86	95	R17
-	6	T2	87	96	SCL
5	7	V_{SS1}	88	97	SDA
6	8	V_{SS2}	89	98	E
7	9	V_{LCDOUT}	90	99	RS
-	10	$V_{LCDSENSE}$	91	100	R/$\overline{W}$

Table 3. Pin (LQFP100 package) or pad allocation table *...continued*

Pin	Pad	Symbol	Pin	Pad	Symbol
8	11	V_{LCDIN}	92	101	DB7
9 to 16	12 to 19	R9 to R16	93	102	DB6
17	20	R18	94	103	DB5
18 to 25	21 to 28	C60 to C53	95	104	DB4
-	29	dummy pad	96	105	DB3/SA0
-	30	dummy pad	97	106	DB2
26 to 50	31 to 55	C52 to C28	98	107	DB1
-	56	dummy pad	99	108	DB0
-	57	dummy pad	100	109	V_{DD2}
51 to 75	58 to 82	C27 to C3	-	110	V_{DD3}
-	83	dummy pad	-	-	-

Table 4. Bonding pad dimensions

Pad	Size		Unit
Type	galvanic pure Au		
Bump dimensions	$(50 \pm 6) \times (90 \pm 6) \times (17.5 \pm 5)$		µm
Height difference in one die	< 2		µm
Convex deformation	< 5		µm
Pad size (aluminium)	62×100		µm
Passivation opening	36×76		µm
Pad pitch	–635.0		µm
Wafer thickness (excluding bumps)	380 ± 25		µm
	Fab 1 [1]	**Fab 2** [2]	
Die size X	3.52	3.47	mm
Die size Y	3.36	3.31	mm

[1] Fab 1 identification starts with nnnnnn, where n represents a number between 0 and 9 (8 inch wafer).

[2] Fab 2 identification starts with AXnnnn, where X represents a letter or a number and n represents a number between 0 and 9 (6 inch wafer).

Table 5. Pin and bonding pad description

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (µm)	Y (µm)	Description	
V_{DD1}	1	P	1	–1345	–1550	supply voltage 1 for all except V_{LCD} generator	
OSC	2	I	2	–1155	–1550	oscillator and external clock input	[1]
PD	3	I	3	–1055	–1550	power-down select input; for normal operation PD is LOW	
T3	-	I	4	–845	–1550	test pad; open circuit and not user accessible	
T1	4	I	5	–765	–1550	test pin; must be connected to V_{SS1}	
T2	-	I	6	–665	–1550	test pad; must be connected to V_{SS1}	
V_{SS1}	5	P	7	–525	–1550	ground 1 for all except V_{LCD} generator	

Table 5. Pin and bonding pad description *...continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (μm)	Y (μm)	Description
V_{SS2}	6	P	8	−455	−1550	ground 2 for V_{LCD} generator
V_{LCDOUT}	7	O	9	−295	−1550	V_{LCD} output if V_{LCD} is generated internally [2]
$V_{LCDSENSE}$	-	I	10	−145	−1550	input (V_{LCD}) for voltage multiplier regulation [2][3]
V_{LCDIN}	8	I	11	15	−1550	input for generation of LCD bias levels [2]
R9	9	O	12	175	−1550	LCD row driver output
R10	10	O	13	245	−1550	LCD row driver output
R11	11	O	14	315	−1550	LCD row driver output
R12	12	O	15	385	−1550	LCD row driver output
R13	13	O	16	455	−1550	LCD row driver output
R14	14	O	17	525	−1550	LCD row driver output
R15	15	O	18	595	−1550	LCD row driver output
R16	16	O	19	665	−1550	LCD row driver output
R18	17	O	20	735	−1550	LCD row driver output
C60	18	O	21	805	−1550	LCD column driver output
C59	19	O	22	875	−1550	LCD column driver output
C58	20	O	23	995	−1550	LCD column driver output
C57	21	O	24	1065	−1550	LCD column driver output
C56	22	O	25	1135	−1550	LCD column driver output
C55	23	O	26	1205	−1550	LCD column driver output
C54	24	O	27	1275	−1550	LCD column driver output
C53	25	O	28	1345	−1550	LCD column driver output
dummy pad 1	-	-	29	1435	−1550	-
dummy pad 2	-	-	30	1630	−1395	-
C52	26	O	31	1630	−1255	LCD column driver output
C51	27	O	32	1630	−1155	LCD column driver output
C50	28	O	33	1630	−1055	LCD column driver output
C49	29	O	34	1630	−955	LCD column driver output
C48	30	O	35	1630	−735	LCD column driver output
C47	31	O	36	1630	−635	LCD column driver output
C46	32	O	37	1630	−535	LCD column driver output
C45	33	O	38	1630	−435	LCD column driver output
C44	34	O	39	1630	−335	LCD column driver output
C43	35	O	40	1630	−235	LCD column driver output
C42	36	O	41	1630	−135	LCD column driver output
C41	37	O	42	1630	−35	LCD column driver output
C40	38	O	43	1630	65	LCD column driver output
C39	39	O	44	1630	165	LCD column driver output
C38	40	O	45	1630	265	LCD column driver output
C37	41	O	46	1630	365	LCD column driver output

Table 5. Pin and bonding pad description *...continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (μm)	Y (μm)	Description
C36	42	O	47	1630	465	LCD column driver output
C35	43	O	48	1630	565	LCD column driver output
C34	44	O	49	1630	665	LCD column driver output
C33	45	O	50	1630	765	LCD column driver output
C32	46	O	51	1630	865	LCD column driver output
C31	47	O	52	1630	965	LCD column driver output
C30	48	O	53	1630	1065	LCD column driver output
C29	49	O	54	1630	1165	LCD column driver output
C28	50	O	55	1630	1265	LCD column driver output
dummy pad 3	-	-	56	1630	1335	-
dummy pad 4	-	-	57	1435	1550	-
C27	51	O	58	1335	1550	LCD column driver output
C26	52	O	59	1225	1550	LCD column driver output
C25	53	O	60	1115	1550	LCD column driver output
C24	54	O	61	1005	1550	LCD column driver output
C23	55	O	62	765	1550	LCD column driver output
C22	56	O	63	665	1550	LCD column driver output
C21	57	O	64	565	1550	LCD column driver output
C20	58	O	65	465	1550	LCD column driver output
C19	59	O	66	365	1550	LCD column driver output
C18	60	O	67	265	1550	LCD column driver output
C17	61	O	68	165	1550	LCD column driver output
C16	62	O	69	65	1550	LCD column driver output
C15	63	O	70	−35	1550	LCD column driver output
C14	64	O	71	−135	1550	LCD column driver output
C13	65	O	72	−235	1550	LCD column driver output
C12	66	O	73	−335	1550	LCD column driver output
C11	67	O	74	−435	1550	LCD column driver output
C10	68	O	75	−535	1550	LCD column driver output
C9	69	O	76	−635	1550	LCD column driver output
C8	70	O	77	−735	1550	LCD column driver output
C7	71	O	78	−835	1550	LCD column driver output
C6	72	O	79	−965	1550	LCD column driver output
C5	73	O	80	−1065	1550	LCD column driver output
C4	74	O	81	−1165	1550	LCD column driver output
C3	75	O	82	−1265	1550	LCD column driver output
dummy pad 5	-	-	83	−1465	1550	-
dummy pad 6	-	-	84	−1630	1355	-
C2	76	O	85	−1630	1255	LCD column driver output

Table 5. Pin and bonding pad description *...continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (μm)	Y (μm)	Description	
C1	77	O	86	−1630	1185	LCD column driver output	
R8	78	O	87	−1630	1115	LCD row driver output	
R7	79	O	88	−1630	1045	LCD row driver output	
R6	80	O	89	−1630	975	LCD row driver output	
R5	81	O	90	−1630	905	LCD row driver output	
R4	82	O	91	−1630	835	LCD row driver output	
R3	83	O	92	−1630	765	LCD row driver output	
R2	84	O	93	−1630	695	LCD row driver output	
R1	85	O	94	−1630	625	LCD row driver output	
R17	86	O	95	−1630	555	LCD row driver output	
SCL	87	I	96	−1630	375	I^2C-bus serial clock input	[4]
SDA	88	I/O	97	−1630	305	I^2C-bus serial data input/output	[4]
E	89	I	98	−1630	85	data bus clock input	[4]
RS	90	I	99	−1630	−15	register select input	
R/$\overline{W}$	91	I	100	−1630	−115	read or write input	
DB7	92	I/O	101	−1630	−215	8-bit bidirectional bus bit 7	[5]
DB6	93	I/O	102	−1630	−315	8-bit bidirectional bus bit 6	
DB5	94	I/O	103	−1630	−415	8-bit bidirectional bus bit 5	
DB4	95	I/O	104	−1630	−515	8-bit bidirectional bus bit 4	
DB3/SA0	96	I/O	105	−1630	−615	8-bit bidirectional bus bit 3 or I^2C-bus address input	[4][5]
DB2	97	I/O	106	−1630	−715	8-bit bidirectional bus bit 2	
DB1	98	I/O	107	−1630	−815	8-bit bidirectional bus bit 1	
DB0	99	I/O	108	−1630	−915	8-bit bidirectional bus bit 0	
V_{DD2}	100	P	109	−1630	−1015	supply voltage 2 for V_{LCD} generator	[6]
V_{DD3}	-	P	110	−1630	−1235	supply voltage 3 for V_{LCD} generator	[3][6]
dummy pad 7	-	-	111	−1630	−1395	-	
dummy pad 8	-	-	112	−1465	−1550	-	

[1] When the on-chip oscillator is used this pad must be connected to V_{DD1}.

[2] When V_{LCD} is generated internally, pins V_{LCDIN}, V_{LCDOUT} and $V_{LCDSENSE}$ must be connected together. When an external V_{LCD} is supplied, this should be done via V_{LCDIN}. In this case only pins V_{LCDOUT} and $V_{LCDSENSE}$ must be connected together.

[3] In the LQFP100 version this signal is connected internally and is not accessible.

[4] When the I^2C-bus is used, the parallel interface pin E must be LOW. In the I^2C-bus read mode pins DB7 to DB0 must be connected to V_{DD1} or left open-circuit.

When the parallel bus is used, the pins SCL and SDA must be connected to pin V_{SS1} or pin V_{DD1}; they must not be left open-circuit.

When the 4-bit interface is used without reading out from the PCF2113x (bit R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be connected to V_{SS1} or V_{DD1} instead of leaving them open-circuit.

[5] DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the four higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit except for I^2C-bus operations (see Table note 4).

[6] V_{DD2} and V_{DD3} must always be equal.

8. Functional description

8.1 LCD supply voltage generator

The LCD supply voltage (V_{LCD}) may be generated on-chip. The V_{LCD} generator is controlled by two internal 6-bit registers: VA and VB. Section 10.10.1 shows how to program these registers. The nominal LCD operating voltage at room temperature is given by the relationship:

$V_{oper(nom)}$ = (integer value of register × 0.08 V) + 1.82 V

With a programmed value from 1 to 63, $V_{oper(nom)}$ = 1.90 V to 6.86 V at T_{amb} = 27 °C.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} tolerance and temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and therefore are not allowed.

Value 0 for VA and VB switches off the generator (i.e. VA = 0 in Character mode, VB = 0 in Icon mode).

Usually register VA is programmed with the voltage for Character mode and register VB with the voltage for Icon mode.

When V_{LCD} is generated on-chip, the V_{LCD} pins must be decoupled to V_{SS} with a suitable capacitor.

The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the V_{LCD} generator and the Direct mode are switched off, an external voltage may be supplied at pins V_{LCDIN} and V_{LCDOUT} (which are connected together). V_{LCDIN} and V_{LCDOUT} may be higher or lower than V_{DD2}.

During Direct mode (program DM bit) the internal V_{LCD} generator is turned off and the V_{LCDOUT} output voltage is directly connected to V_{DD2}. This reduces the current consumption during Icon mode and MUX 1:9 (depending on V_{DD2} and LCD liquid properties).

The V_{LCD} generator ensures that, as long as V_{DD} is in the valid range (2.2 V to 4 V), the required peak operating voltage of 6.5 V can be generated at any time.

8.2 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. Using a 5-level bias scheme for 1:18 maximum rate allows V_{LCD} < 5 V for most LCD liquids. The intermediate bias levels for the different multiplex rates are shown in Table 6. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 6. Bias levels as a function of multiplex rate

Multiplex rate	Number of levels	Bias voltages[1]					
		V_1	V_2	V_3	V_4	V_5	V_6
1:18	5	V_{LCD}	$^3/_4$	$^1/_2$	$^1/_2$	$^1/_4$	V_{SS}
1:9	5	V_{LCD}	$^3/_4$	$^1/_2$	$^1/_2$	$^1/_4$	V_{SS}
1:2	4	V_{LCD}	$^2/_3$	$^2/_3$	$^1/_3$	$^1/_3$	V_{SS}

[1] The values in the table are given relative to $V_{LCD} - V_{SS}$, e.g. $^3/_4$ means $\{^3/_4 \times (V_{LCD} - V_{SS})\} + V_{SS}$.

8.3 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD1}.

8.4 External clock

If an external clock is to be used, this input is at the OSC pin. The resulting display frame frequency is given by: $f_{fr(LCD)} = \frac{f_{osc}}{3072}$

Only in the Power-down mode is the clock allowed to be stopped (pin OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

8.5 Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 oscillator cycles to be executed.

8.6 Registers

The PCF2113x has two 8-bit registers: an Instruction Register (IR) and a Data Register (DR). The Register Select (RS) signal determines which register will be accessed. The instruction register stores instruction codes such as ‘display clear’, ‘cursor shift’, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to but not read from by the system controller.

The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the ‘read data’ instruction.

8.7 Busy flag

The busy flag indicates the internal status of the PCF2113x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pin DB7 when bit RS = 0 and bit R/$\overline{W}$ = 1. Instructions must only be written after checking that the busy flag is at logic 0 or waiting for the required number of cycles.

8.8 Address counter

The Address Counter (AC) assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands ‘set DDRAM address’ and ‘set CGRAM address’. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter contents are output to the bus (DB6 to DB0) when bit RS = 0 and bit R/$\overline{W}$ = 1.

8.9 Display data RAM

The Display Data RAM (DDRAM) stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Figure 4. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00h in line 1 are displayed. Figure 5 and Figure 6 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM, wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together. The address ranges and wrap-around operations for the various modes are shown in Table 7.

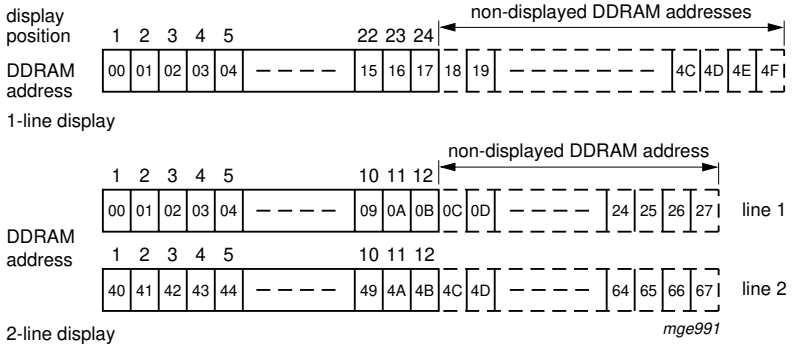


Fig 4. DDRAM to display mapping: no shift

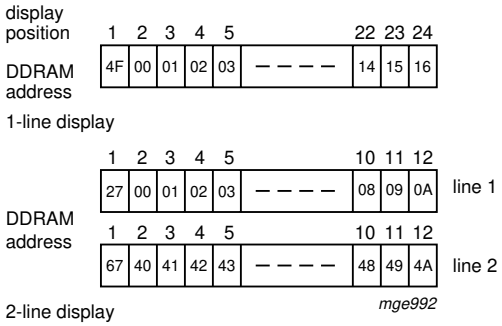


Fig 5. DDRAM to display mapping: right shift

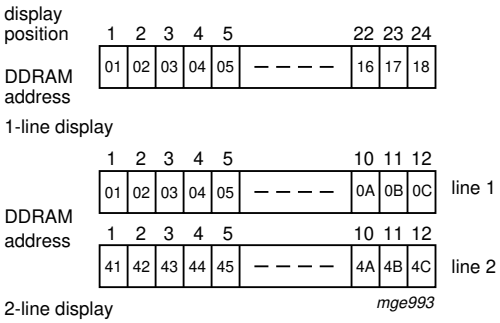


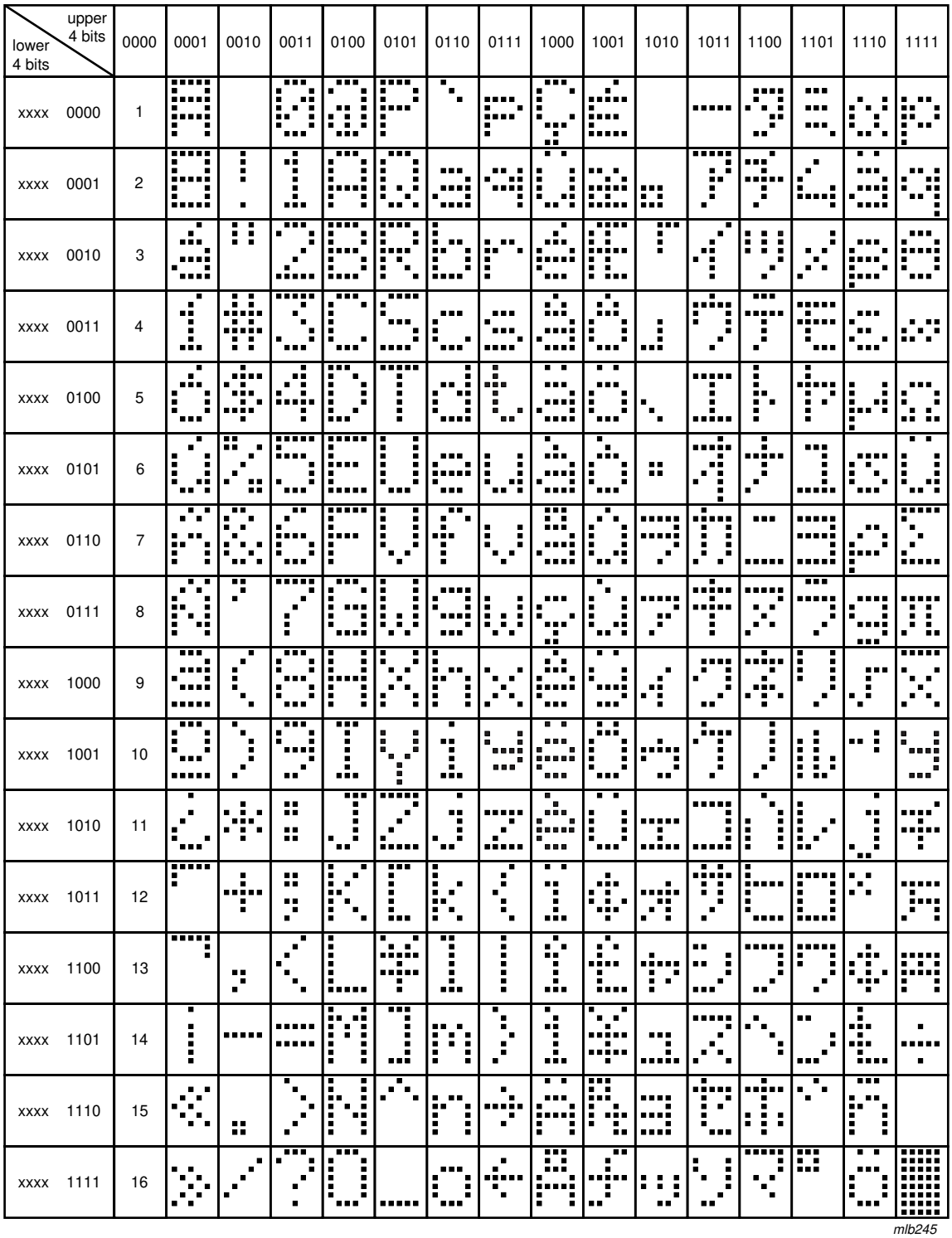
Fig 6. DDRAM to display mapping: left shift

Table 7. Address space and wrap-around operation

Mode	1 × 24	2 × 12	1 × 12
Address space	00h to 4Fh	00h to 27h; 40h to 67h	00h to 27h
Read/write wrap-around (moves to next line)	4Fh to 00h	27h to 40h; 67h to 00h	27h to 00h
Display shift wrap-around (stays within line)	4Fh to 00h	27h to 00h; 67h to 40h	27h to 00h

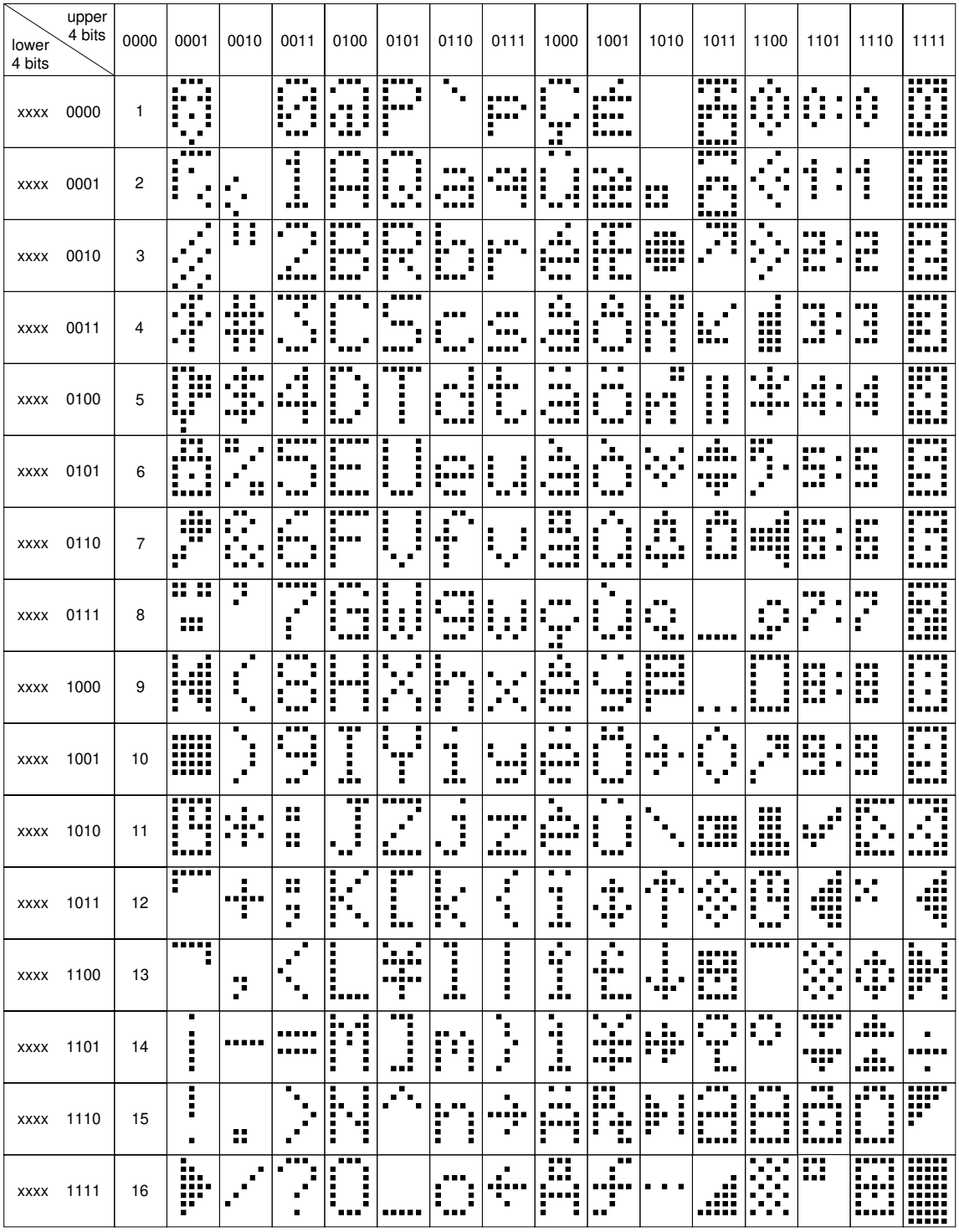
8.10 Character generator ROM

The Character Generator ROM (CGROM) generates 240 character patterns in a 5 × 8 dot format from 8-bit character codes. Figure 7, Figure 8, Figure 9 and Figure 10 show the character sets that are currently implemented.



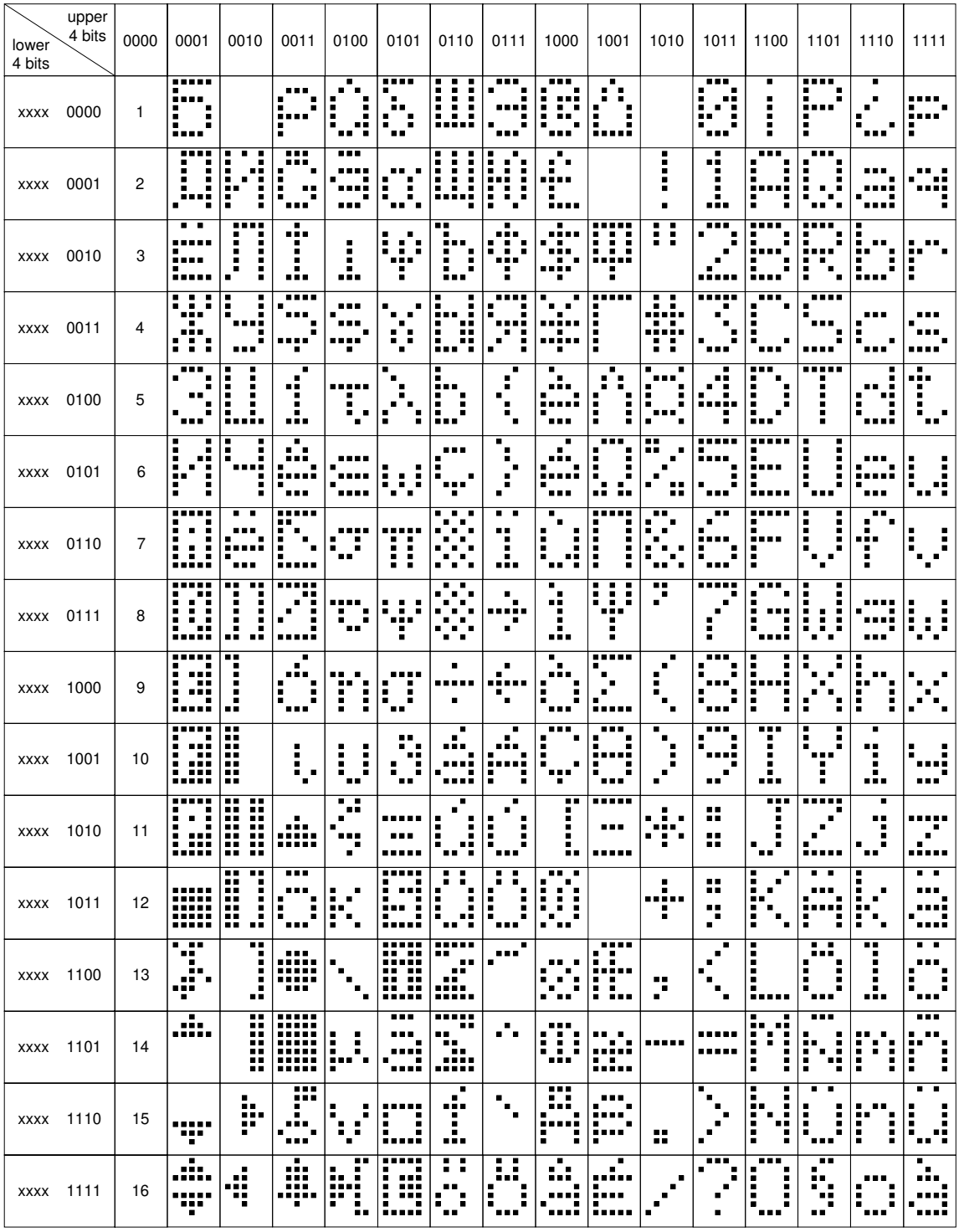
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 7. Character set ‘A’ in CGROM



The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

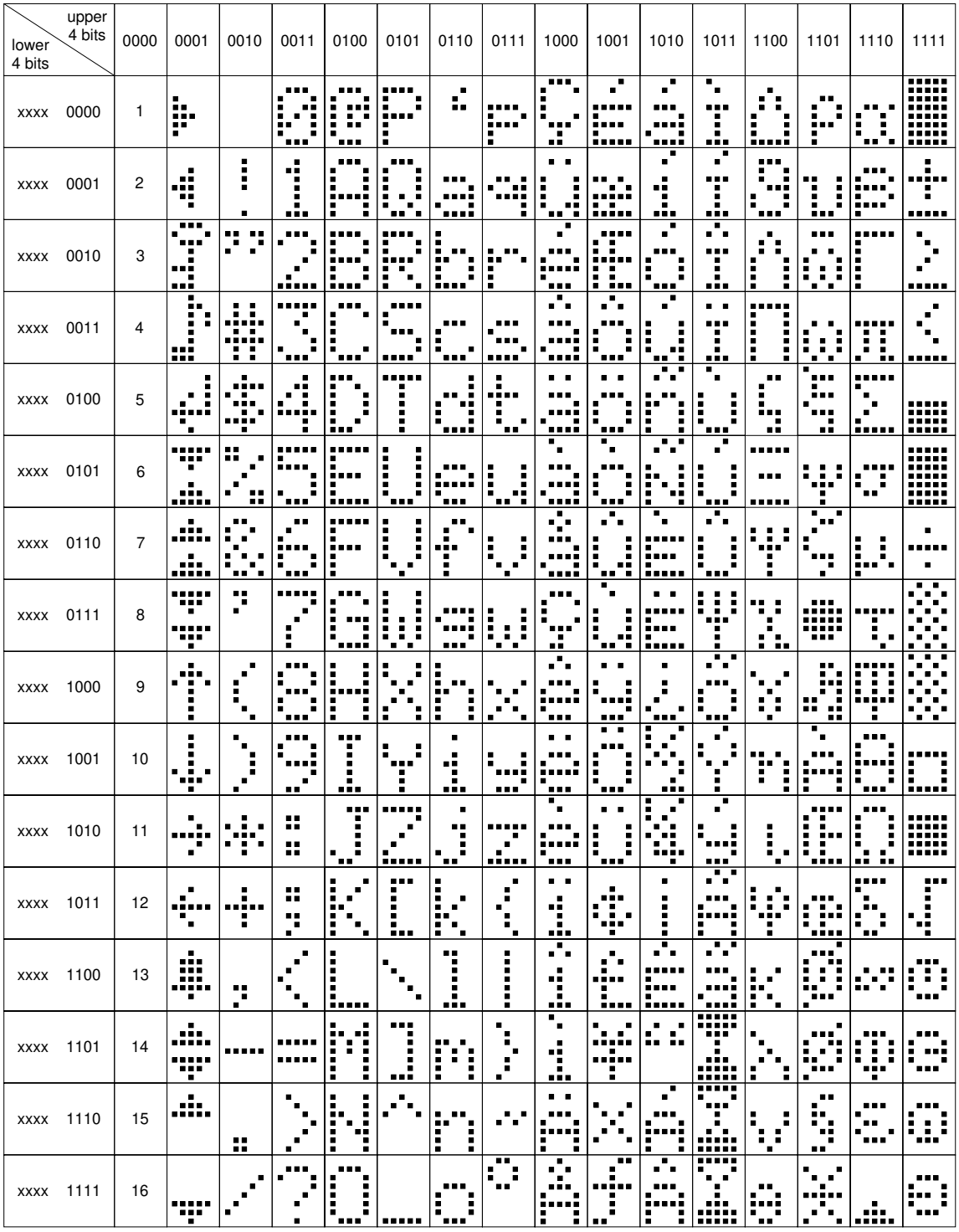
Fig 8. Character set ‘D’ in CGROM



mgd689

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 9. Character set ‘E’ in CGROM



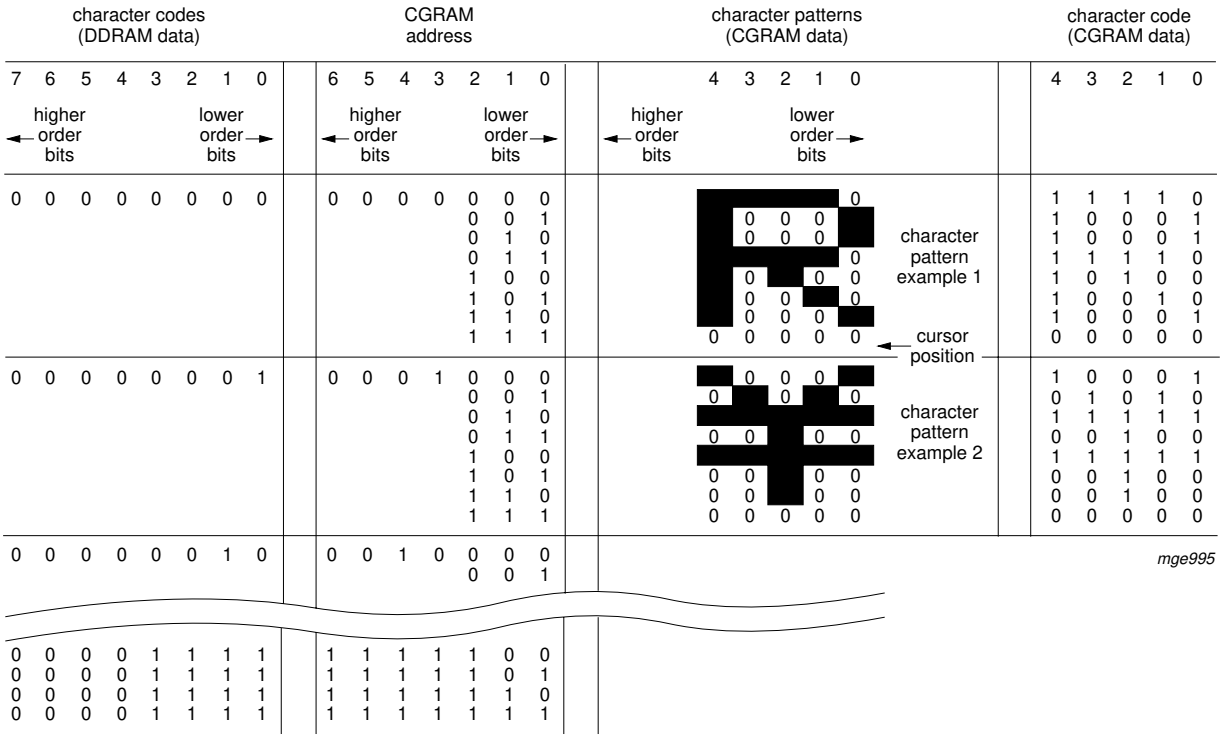
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 10. Character set 'W' in CGROM

8.11 Character generator RAM

Up to 16 user-defined characters may be stored in the Character Generator RAM (CGRAM). Some CGRAM characters (see Figure 18 and Figure 19) are also used to drive icons (6 if icons blink and both icon rows are used in the application; 3 if no blink but both icon rows are used in the application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Figure 7, Figure 8, Figure 9 and Figure 10).

Figure 11 shows the addressing principle for the CGRAM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logic OR with the cursor. Data in the 8th position appears in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in this figure.

CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' command. Bit 6 can be set using the 'set DDRAM address' command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag' and 'address counter' command.

Fig 11. Relationship between CGRAM addresses, data and display patterns

8.12 Cursor control circuit

The cursor control circuit generates the cursor underline and/or cursor blink as shown in Figure 12 at the DDRAM address contained in the address counter.

When the address counter contains the CGRAM address the cursor will be inhibited.

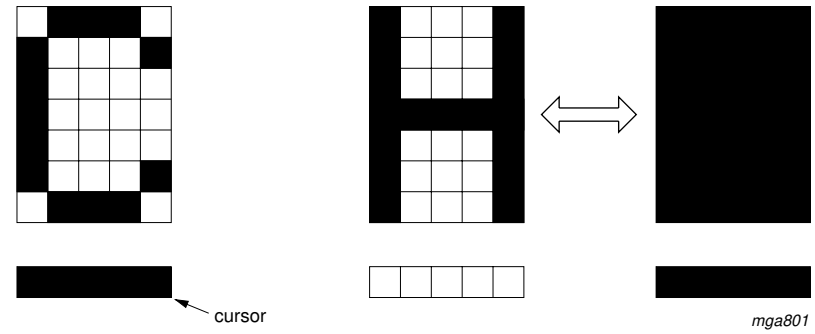
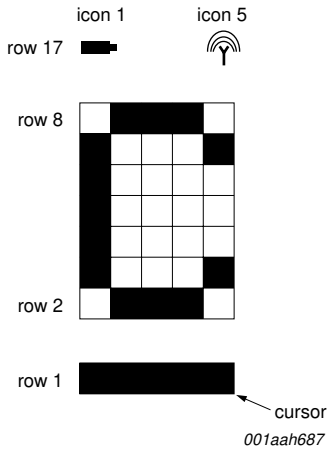


Fig 12. Cursor and blink display examples



Bit Q = 1

Fig 13. Example of a display with icons

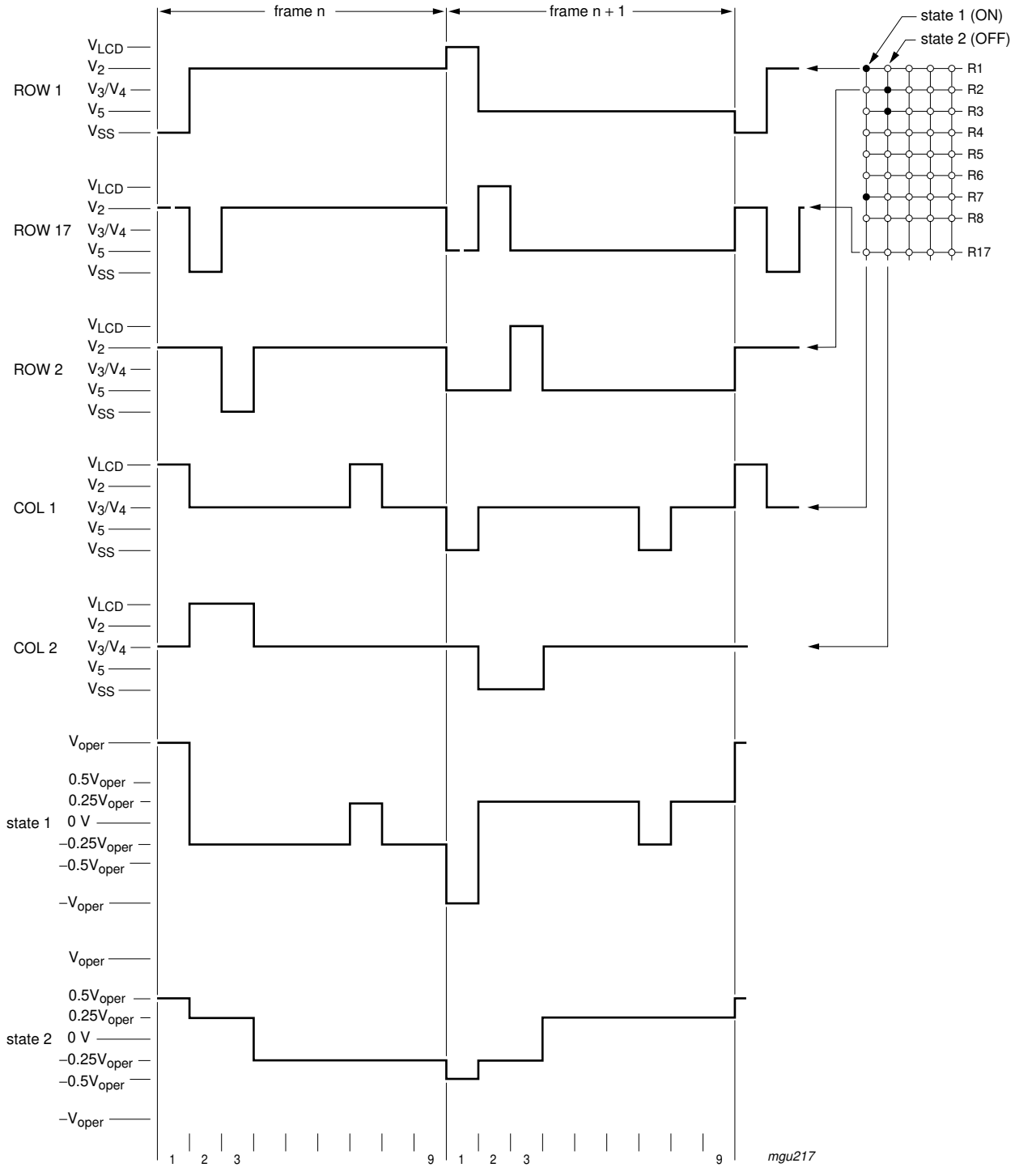
8.13 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.14 LCD row and column drivers

The PCF2113x contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figure 14, Figure 15, Figure 16 and Figure 17 show typical waveforms. Unused outputs should be left unconnected.



R9 to R16 and R18 to be left open

Fig 14. MUX 1:9 LCD waveforms; Character mode

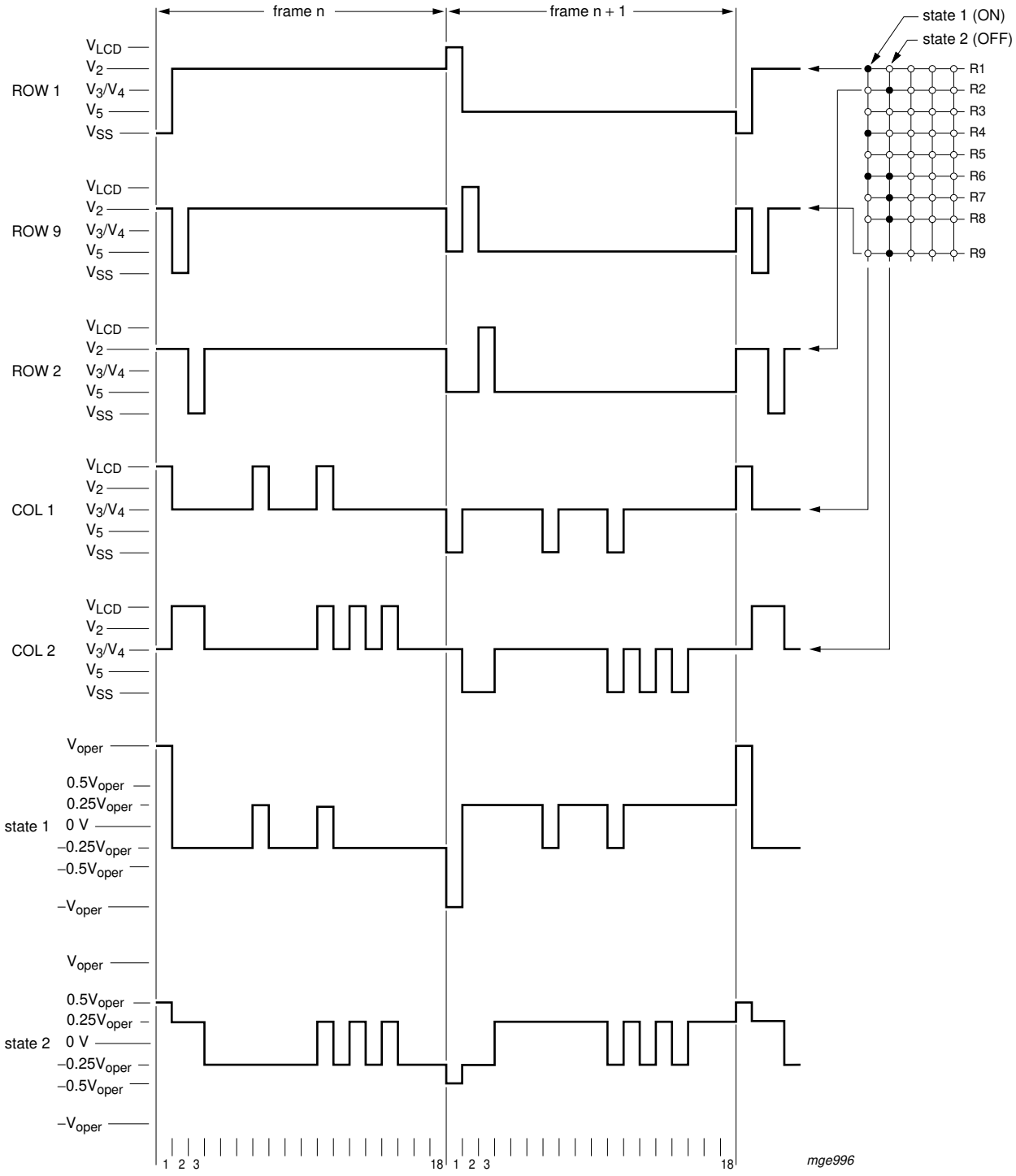


Fig 15. MUX 1:18 LCD waveforms; Character mode

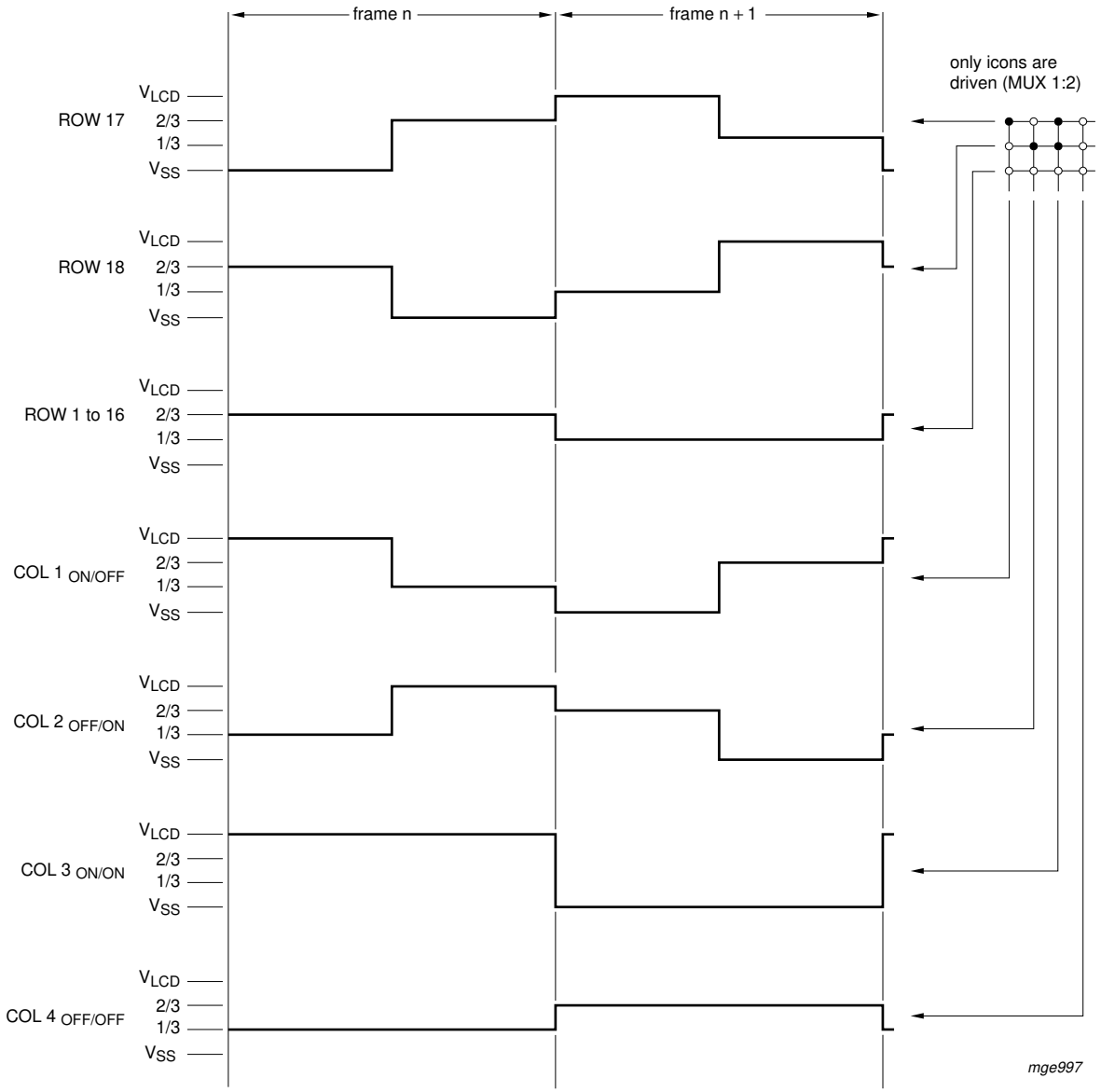
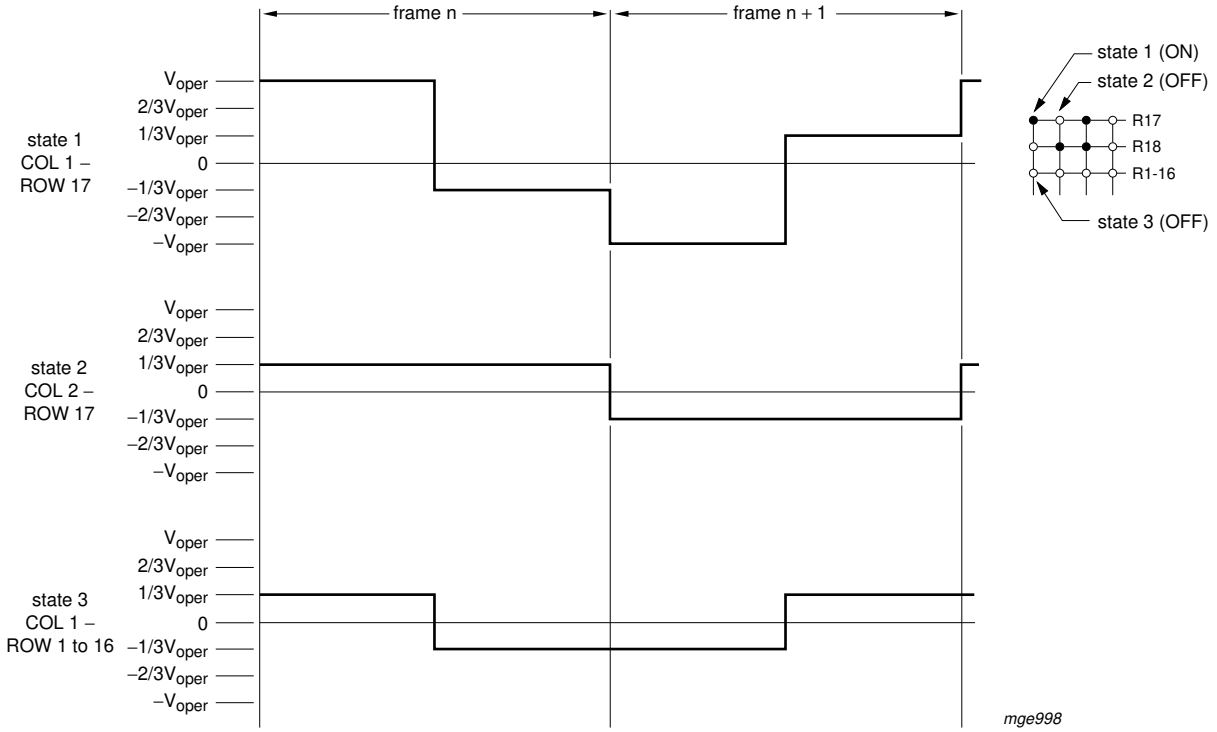


Fig 16. MUX 1:2 LCD waveforms; Icon mode (a)



$V_{on(RMS)} = 0.745V_{oper}$

$V_{off(RMS)} = 0.333V_{oper}$

$$D = \frac{V_{on}}{V_{off}} = 2.23$$

Fig 17. MUX 1:2 LCD waveforms; Icon mode (b)

8.15 Power-down mode

The chip can be put into Power-down mode by applying an external HIGH level to the PD pin. In Power-down mode all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}).

During power-down, information in the RAMs and the chip state are preserved. Instruction execution during power-down is possible when pin OSC is externally clocked.

8.16 Reset function

The PCF2113x automatically initializes (resets) when power is turned on. The chip executes a reset sequence, including a ‘clear display’, requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 8.

Table 8. State after reset

Step	Function	Control bit state	Conditions
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
		SL = 0	MUX 1:18 mode
5	default address pointer to DDRAM	the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends	the busy state lasts 2 ms; the chip may also be initialized by software; see Table 26 (8-bit interface) and Table 27 (4-bit interface).
6	icon control	IM = 0; IB = 0; DM = 0	icons, icon blink and Direct mode disabled
7	display or screen configuration	L = 0; P = 0; Q = 0	default configurations
8	V_{LCD} temperature coefficient	TC1 = 0; TC2 = 0	default temperature coefficient
9	set V_{LCD}	VA = 0; VB = 0	V_{LCD} generator off
10	I^2C-bus interface reset		
11	set HVgen stages	S1 = 1; S0 = 0	V_{LCD} generator voltage multiplier set at factor 4

9. Instructions

Only two PCF2113x registers, the Instruction Register (IR) and the Data Register (DR), can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interfacing to various types of microcontrollers which operate at different speeds or to allow interfacing to peripheral control ICs.

The instruction set for I^2C-bus commands is given in Table 9. Section 11.2.1 discusses how these control and command bytes are embedded in the I^2C-bus protocol.

Table 9. Instruction set for I^2C-bus commands

I^2C-bus commands	Control byte								Command byte								I^2C-bus commands
[1]	Co[2]	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	[1]

[1] R/$\overline{W}$ is set together with the slave address.

[2] For explanation, see Table 11.

The PCF2113x operation is controlled by the instructions shown in Table 10 together with their execution time. Details are explained in subsequent sections.

There are 4 types of instructions:

- Designate PCF2113x functions such as display format, data length
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Other functions

In normal use, data transfer instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the ‘read busy flag’ and ‘read address’ instructions will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, check to ensure it is logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 10. An instruction sent while the busy flag is logic 1 will not be executed.

Table 10. Instruction set with parallel bus commands

Instruction	Control and command bits										Description[1]	Required clock cycles
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
H = 0 or 1 (basic and extended functions)												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	SL	H	sets interface Data Length (DL), number of display lines (M), single line/MUX 1:9 (SL) and extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	AC							reads the Busy Flag (BF), indicating internal operating is being performed, and the Address Counter (AC)	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data to CGRAM or DDRAM	3
H = 0 (basic functions)												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3