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PCF2123

SPI Real time clock/calendar

Rev. 6 — 15 July 2013 Product data sheet

1. General description

The PCF2123 is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power applications. Data is transferred serially via a Serial Peripheral Interface (SPI-bus) with a maximum data rate of 6.25 Mbit/s. An alarm and timer function is also available providing the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine tuning of the clock.

2. Features and benefits

- Real time clock provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Low backup current while running: typical 100 nA at V_{DD} = 2.0 V and T_{amb} = 25 °C
- Resolution: seconds to years
- Watchdog functionality
- Freely programmable timer and alarm with interrupt capability
- Clock operating voltage: 1.1 V to 5.5 V
- 3 line SPI-bus with separate, but combinable data input and output
- Serial interface at V_{DD} = 1.8 V to 5.5 V
- 1 second or 1 minute interrupt output
- Integrated oscillator load capacitors for C_L = 7 pF
- Internal Power-On Reset (POR)
- Open-drain interrupt and clock output pins
- Programmable offset register for frequency adjustment

3. Applications

- Time keeping application
- Battery powered devices
- Metering
- High duration timers
- Daily alarms
- Low standby power applications

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 22.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2123BS	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCF2123TS	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
PCF2123U/10AA	wire bond die	12 bonding pads	PCF2123U/10
PCF2123U/12AA	WLCSP12	wafer level chip size package; 12 bumps	PCF2123U/12
PCF2123U/12HA	WLCSP12	wafer level chip size package; 12 bumps	PCF2123U/12
PCF2123U/5GA	wire bond die	12 bonding pads	PCF2123U/10

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF2123BS/1	935286382512	PCF2123BS/1,512	1	tube, dry pack
	935286382518	PCF2123BS/1,518	1	tape and reel, 13 inch, dry pack
PCF2123TS/1	935286384112	PCF2123TS/1,112	1	tube
	935286384118	PCF2123TS/1,118	1	tape and reel, 13 inch
PCF2123U/10AA/1	935287542005	PCF2123U/10AA/1,00	1	sawn 6 inch wafer on Film Frame Carrier (FFC) for 6 inch wafer
PCF2123U/12AA/1	935290647005	PCF2123U/12AA/1,00	1	sawn 6 inch wafer on plastic Film Frame Carrier (FFC) for 8 inch wafer
PCF2123U/12HA/1	935292966005	PCF2123U/12HA/1,00	1	sawn 6 inch wafer on plastic Film Frame Carrier (FFC) for 8 inch wafer
PCF2123U/5GA/1	935295429015	PCF2123U/5GA/1,015	1	wafer, unsawn

5. Marking

Table 3. Marking codes

Type number	Marking code
PCF2123BS	123
PCF2123TS	PCF2123
PCF2123U/10AA	PC2123-1
PCF2123U/12AA	PC2123-1
PCF2123U/12HA	PC2123-1
PCF2123U/5GA	PC2123-1

6. Block diagram

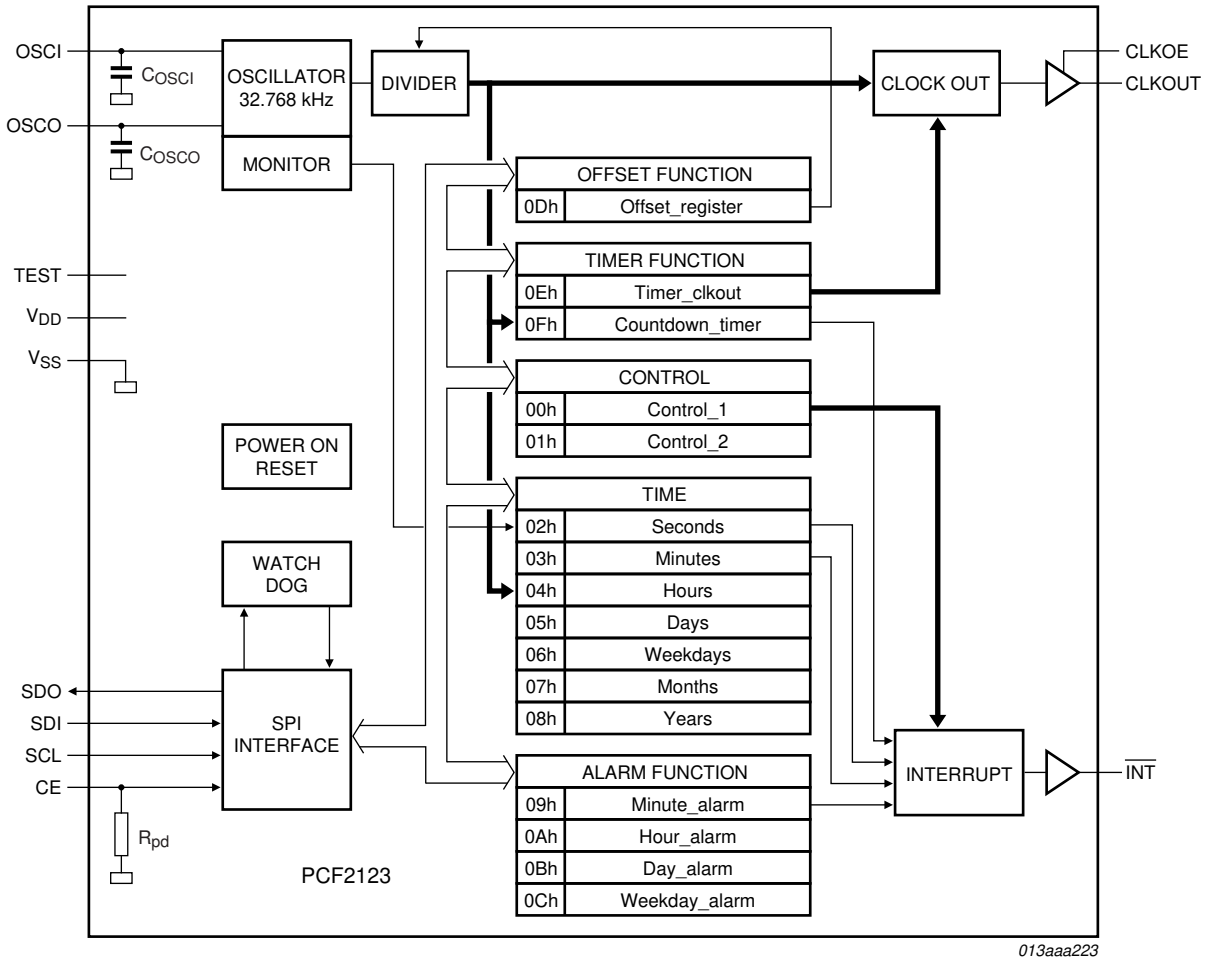
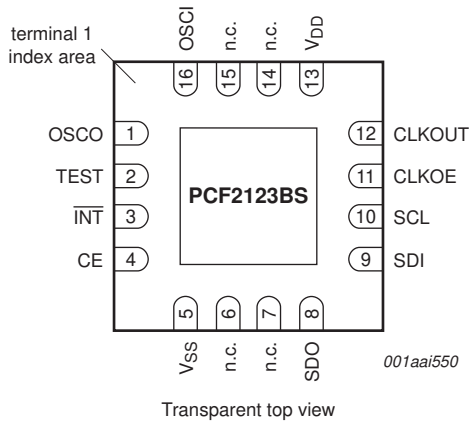


Fig 1. Block diagram of PCF2123

7. Pinning information

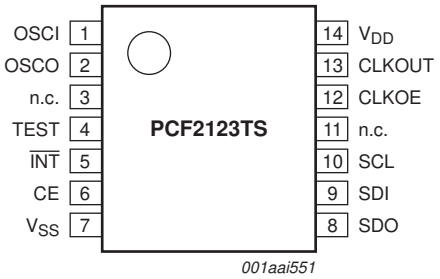
7.1 Pinning



Transparent top view

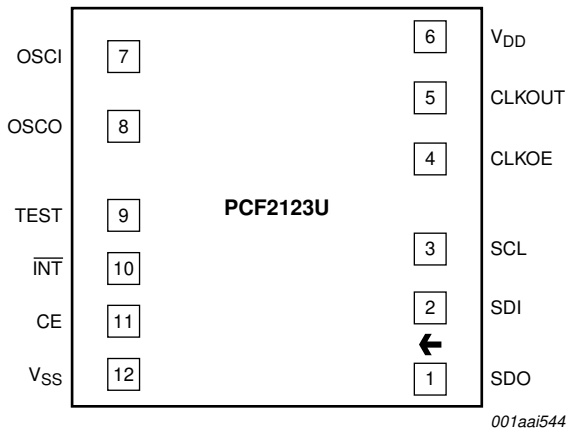
For mechanical details, see Figure 31 on page 45.

Fig 2. Pin configuration for HVQFN16 (PCF2123BS/1)



Top view. For mechanical details, see Figure 32 on page 46.

Fig 3. Pin configuration for TSSOP14 (PCF2123TS/1)



Viewed from active side. For mechanical details, see Figure 33 on page 47 and Figure 34 on page 48.

Fig 4. Pin configuration for PCF2123Ux (bare die)

7.2 Pin description

Table 4. Pin description

Symbol	Pin			Description
	HVQFN16 (PCF2123BS/1)	TSSOP14 (PCF2123TS/1)	PCF2123Ux (bare die)	
OSCI	16	1	7	oscillator input; high-impedance node; minimize wire length between quartz and package
OSCO	1	2	8	oscillator output; high-impedance node; minimize wire length between quartz and package
n.c.	6, 7, 14, 15	3, 11	-	do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
TEST	2	4	9	test pin; not user accessible; connect to V_{SS} or leave floating (internally pulled down)
$\overline{INT}$	3	5	10	interrupt output (open-drain; active LOW)
CE	4	6	11	chip enable input (active HIGH) with internal pull down
V_{SS}	5[1]	7	12[2]	ground
SDO	8	8	1	serial data output, push-pull; high-impedance when not driving; can be connected to SDI for single wire data line
SDI	9	9	2	serial data input; may float when CE is inactive
SCL	10	10	3	serial clock input; may float when CE is inactive
CLKOE	11	12	4	CLKOUT enable or disable pin; enable is active HIGH
CLKOUT	12	13	5	clock output (open-drain)
V_{DD}	13	14	6	supply voltage; positive or negative steps in V_{DD} may affect oscillator performance; recommend 100 nF decoupling close to the device (see Figure 30)

[1] The die paddle (exposed pad) is wired to V_{SS} and should be electrically isolated.

[2] The substrate (rear side of the die) is wired to V_{SS} and should be electrically isolated.

8. Functional description

The PCF2123 contains 16 8-bit registers with an auto-incrementing address counter, an on-chip 32.768 kHz oscillator with two integrated load capacitors, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, and a 6.25 Mbit/s SPI-bus. An offset register allows fine tuning of the clock.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

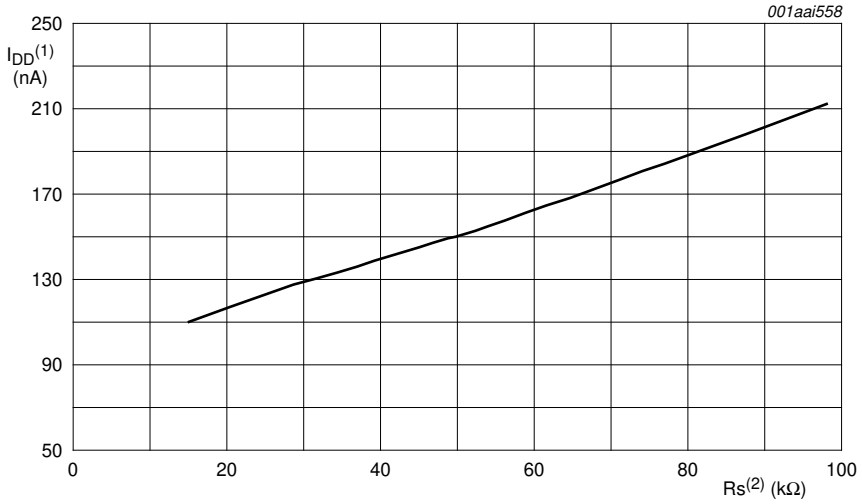
- The first two registers (memory address 00h and 01h) are used as control registers.
- The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years). The registers Seconds, Minutes, Hours, Days, Weekdays, Months, and Years are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read the contents of all counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.
- Addresses 09h through 0Ch define the alarm condition.
- Address 0Dh defines the offset calibration.
- Address 0Eh defines the clock out and timer mode.
- Address registers 0Eh and 0Fh are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 μs up to four hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control_2 (01h).

8.1 Low power operation

Minimum power operation will be achieved by reducing the number and frequency of switching signals inside the IC, i.e., low frequency timer clocks and a low frequency CLKOUT will result in lower operating power. A second prime consideration is the series resistance R_s of the quartz used.

8.1.1 Power consumption with respect to quartz series resistance

The series resistance acts as a loss element. Low R_s will reduce current consumption further.



Configuration: CLKOUT disabled, V_{DD} = 3 V, timer clock set to $^1/_{60}$ Hz.

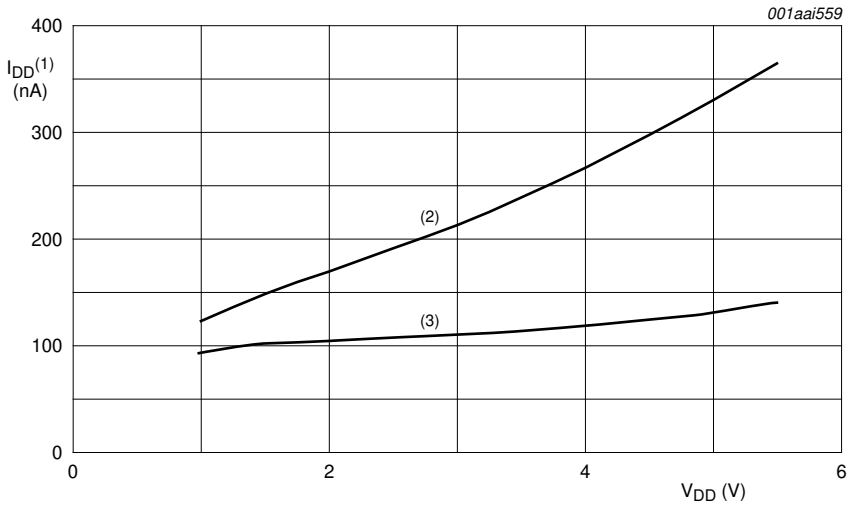
(1) I_{DD} (nA) minimum power mode.

(2) Maximum value for R_S is 100 kΩ.

Fig 5. I_{DD} with respect to quartz R_S

8.1.2 Power consumptions with respect to timer mode

Four source clocks are possible for the timer. The 4.096 kHz source clock will add the greatest part to the power consumption. The selection of 64 Hz, 1 Hz, or $^1/_{60}$ Hz will be almost indistinguishable and add very little.



Configuration: CLKOUT disabled, quartz R_S = 15 kΩ.

(1) I_{DD} (nA) minimum power mode.

(2) Timer clock = 4 kHz.

(3) Timer clock = 64 Hz, 1 Hz, $^1/_{60}$ Hz.

Fig 6. I_{DD} with respect to timer clock selection

8.2 Register overview

16 registers are available. The time registers are encoded in the Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

Table 5. Registers overview

Bit positions labelled as - are not implemented and will return a 0 when read. The bit position labelled as -- is not implemented and will return a 0 or 1 when read. Bit positions labelled with N should always be written with logic 0[1].

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control and status registers									
00h	Control_1	EXT_TEST	N	STOP	SR	N	12_24	CIE	N
01h	Control_2	MI	SI	MSF	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	Seconds	OS	SECONDS (0 to 59)						
03h	Minutes	--	MINUTES (0 to 59)						
04h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 h mode				
				HOURS (0 to 23) in 24 h mode					
05h	Days	-	-	DAYS (1 to 31)					
06h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		
07h	Months	-	-	-	MONTHS (1 to 12)				
08h	Years	YEARS (0 to 99)							
Alarm registers									
09h	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12 h mode				
				HOUR_ALARM (0 to 23) in 24 h mode					
0Bh	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
Offset register									
0Dh	Offset_register	MODE	OFFSET[6:0]						
Timer registers									
0Eh	Timer_clkout	-	COF[2:0]			TE	-	CTD[1:0]	
0Fh	Countdown_timer	COUNTDOWN_TIMER[7:0]							

[1] Except in the case of software reset, see Section 8.3.1.1.

8.3 Control registers

8.3.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0[1]	normal mode	Section 8.10
		1	external clock test mode	
6	N	-	unused	-
5	STOP	0[1]	the RTC source clock runs	Section 8.11
		1	the RTC clock is stopped; RTC divider chain flip-flops are asynchronously set to logic 0; CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available	
4	SR	0[1]	no software reset	Section 8.3.1.1
		1	initiate software reset[2]; this register will always return a 0 when read	
3	N	-	unused	-
2	12_24	0[1]	24 hour mode is selected	-
		1	12 hour mode is selected	
1	CIE	0[1]	no correction interrupt generated	Section 8.9
		1	interrupt pulses will be generated at every correction cycle	
0	N	-	unused	-

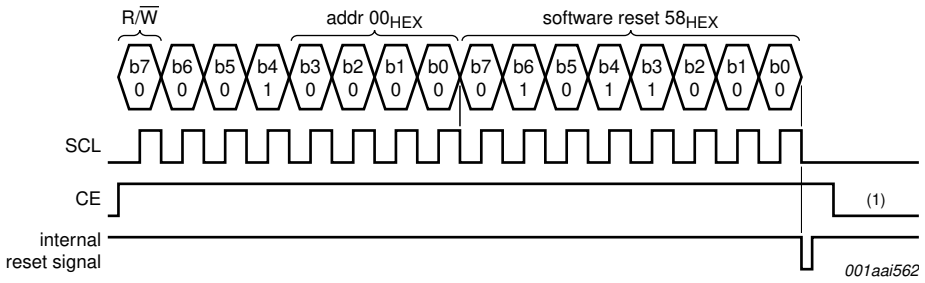
[1] Default value.

[2] For a software reset, 01011000 (58h) must be sent to register Control_1 (see Section 8.3.1.1).

8.3.1.1 Reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. It is generally recommended to make a software reset after power-on.

A software reset can be initiated by setting the bits 6, 4 and 3 in register Control_1 logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see Figure 7. If this bit sequence is not correct, the software reset instruction will be ignored to protect the device from accidently being reset. When sending the software instruction, the other bits are not written.



(1) When CE is inactive, the interface is reset.

Fig 7. Software reset command

After reset, the following mode is entered:

- 32.768 kHz on pin CLKOUT active
- 24 hour mode is selected
- Offset register is set to 0
- No alarms set
- Timer disabled
- No interrupts enabled

Table 7. Register reset values

Bits labeled as - are not implemented. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	0	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Seconds	1	X	X	X	X	X	X	X
03h	Minutes	-	X	X	X	X	X	X	X
04h	Hours	-	-	X	X	X	X	X	X
05h	Days	-	-	X	X	X	X	X	X
06h	Weekdays	-	-	-	-	-	X	X	X
07h	Months	-	-	-	X	X	X	X	X
08h	Years	X	X	X	X	X	X	X	X
09h	Minute_alarm	1	X	X	X	X	X	X	X
0Ah	Hour_alarm	1	-	X	X	X	X	X	X
0Bh	Day_alarm	1	-	X	X	X	X	X	X
0Ch	Weekday_alarm	1	-	-	-	-	X	X	X
0Dh	Offset_register	0	0	0	0	0	0	0	0
0Eh	Timer_clkout	-	0	0	0	0	-	1	1
0Fh	Countdown_timer	X	X	X	X	X	X	X	X

8.3.2 Register Control_2

Table 8. Control_2 - control and status register 2 (address 01h) bits description

Bit	Symbol	Value	Description	Reference
7	MI	0[1]	minute interrupt is disabled	Section 8.6.3
		1	minute interrupt is enabled	
6	SI	0[1]	second interrupt is disabled	
		1	second interrupt is enabled	
5	MSF	0[1]	no minute or second interrupt generated	
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt when TI_IP = 0	
4	TI_TP	0[1]	interrupt pin follows timer flags	Section 8.7.2
		1	interrupt pin generates a pulse	
3	AF	0[1]	no alarm interrupt generated	Section 8.5.5
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
2	TF	0[1]	no countdown timer interrupt generated	Section 8.6.4
		1	flag set when countdown timer interrupt generated; flag must be cleared to clear interrupt when TI_IP = 0	
1	AIE	0[1]	no interrupt generated from the alarm flag	Section 8.7.3
		1	interrupt generated when alarm flag set	
0	TIE	0[1]	no interrupt generated from the countdown timer	Section 8.7.2
		1	interrupt generated by the countdown timer	

[1] Default value.

8.4 Time and date function

The majority of the registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for the seconds in Table 10.

8.4.1 Register Seconds

Table 9. Seconds - seconds register (address 02h) bit description

Bit	Symbol	Value	Place value	Description
7	OS	0	-	clock integrity is guaranteed
		1[1]	-	clock integrity is not guaranteed; oscillator has stopped or has been interrupted
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format, see Table 10
3 to 0		0 to 9	unit place	

[1] Default value.

Table 10. Seconds coded in BCD format

Seconds value (decimal)	Upper-digit (ten's place)				Digit (unit place)			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1

8.4.1.1 OS flag

The PCF2123 includes a flag (OS in register Seconds, see Table 9) which is set whenever the oscillator is stopped (see Figure 8 and Figure 9). The flag will remain set until cleared by software. If the flag cannot be cleared, then the PCF2123 oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

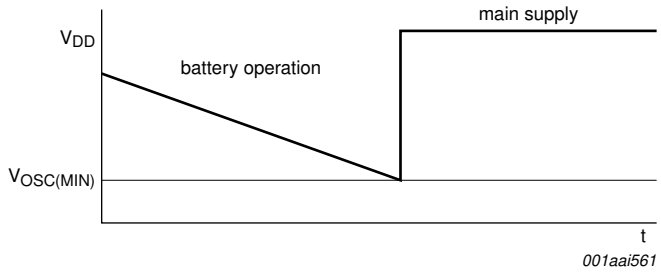


Fig 8. OS set by failing V_{DD}

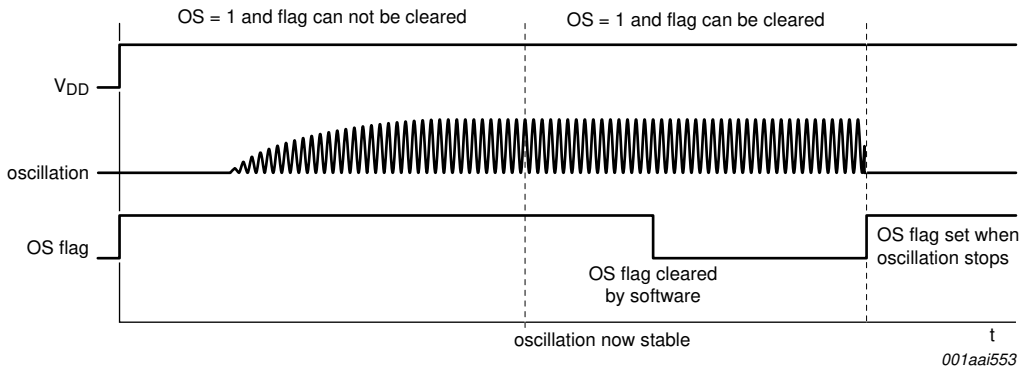


Fig 9. OS flag

The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in the range of 200 ms to 2 s depending on crystal type, temperature and supply voltage. At power-on the OS flag is always set.

8.4.2 Register Minutes

Table 11. Minutes - minutes register (address 03h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

8.4.3 Register Hours

Table 12. Hours - hours register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12 hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOURS	0 to 1	ten's place	actual hours in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 hour mode[1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours in 24 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the 12_24 bit in register Control_1.

8.4.4 Register Days

Table 13. Days - days register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCF2123 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

8.4.5 Register Weekdays

Table 14. Weekdays - weekdays register (address 06h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday values, see Table 15

Table 15. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be re-assigned by the user.

8.4.6 Register Months

Table 16. Months - months register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 17
3 to 0		0 to 9	unit place	

Table 17. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.4.7 Register Years

Table 18. Years - years register (08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

8.4.8 Setting and reading the time

Figure 10 shows the data flow and data dependencies starting from the 1 Hz clock tick.

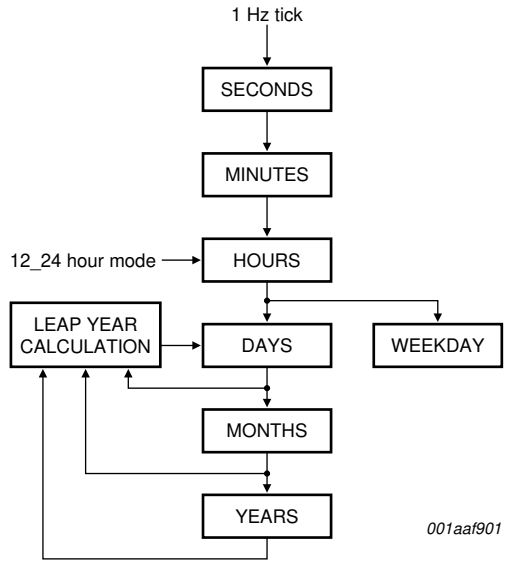


Fig 10. Data flow of the time function

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 11).

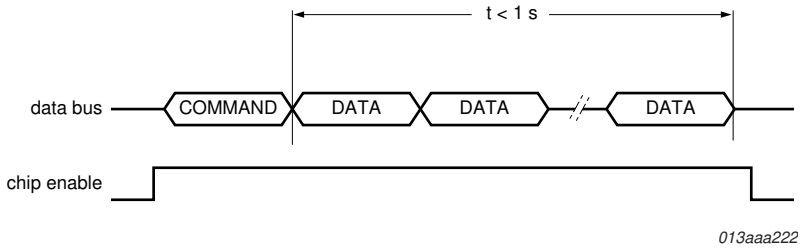


Fig 11. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

8.5 Alarm function

When one or more of these registers are loaded with a valid minute, hour, day, or weekday and its corresponding alarm enable bit (AE_x) is logic 0, then that information will be compared with the current minute, hour, day, and weekday.

8.5.1 Register Minute_alarm

Table 19. Minute_alarm - minute alarm register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.5.2 Register Hour_alarm

Table 20. Hour_alarm - hour alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	hour alarm is enabled
		1[1]	-	hour alarm is disabled
6	-	-	-	unused
12 hour mode[2]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_ALARM	0 to 1	ten's place	hour alarm information coded in BCD format when in 12 hour mode
3 to 0		0 to 9	unit place	
24 hour mode[2]				
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format when in 24 hour mode
3 to 0		0 to 9	unit place	

[1] Default value.

[2] Hour mode is set by the 12_24 bit in register Control_1.

8.5.3 Register Day_alarm

Table 21. Day_alarm - day alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.5.4 Register Weekday_alarm

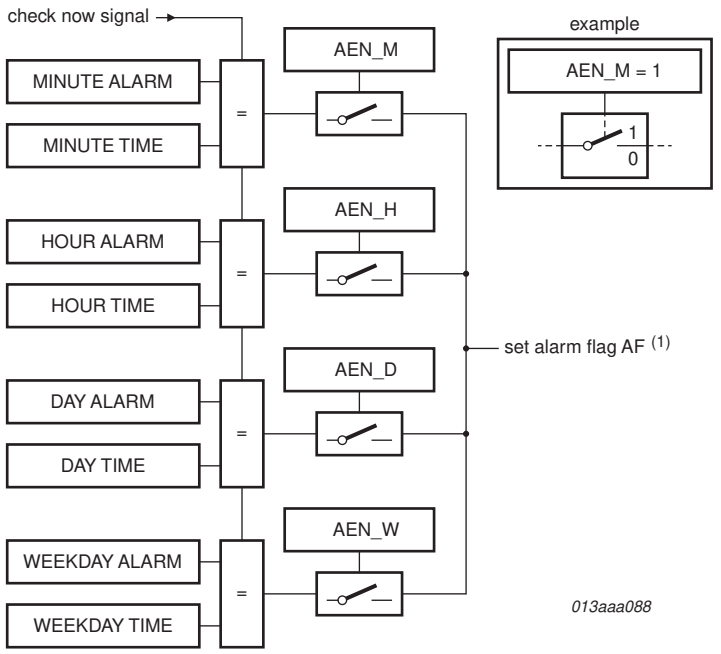
Table 22. Weekday_alarm - weekday alarm register (address 0Ch) bit description

Bit	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information coded in BCD format

[1] Default value.

8.5.5 Alarm flag

By clearing the MSB, AE_x (Alarm Enable), of one or more of the alarm registers the corresponding alarm condition(s) are active. When an alarm occurs, AF (register Control_2, see Table 8) is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared using the interface.



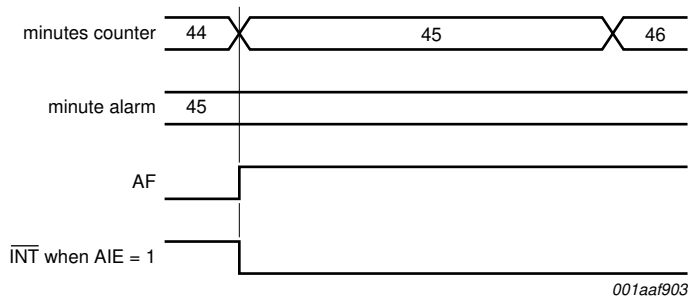
(1) Only when all enabled alarm settings are matching.
It's only on increment to a matched case that the alarm flag is set, see Section 8.5.5.

Fig 12. Alarm function block diagram

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day, or weekday, and its corresponding Alarm Enable bit (AE_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (register Control_2, see Table 8). If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF will remain set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit logic 1 are ignored.

Generation of interrupts from the alarm function is described in Section 8.7.3.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 13. Alarm flag timing

Figure 13, Table 23, and Table 24 show an example for clearing bit AF, but leaving bit MSF and bit TF unaffected. The flags are cleared by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 whilst a flag is not cleared by writing logic 1. Writing logic 1 will result in the flag value remaining unchanged.

Table 23. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 24 shows what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

Table 24. Example to clear only AF (bit 3) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	0	1	-	-

8.6 Timer functions

The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 μs to 4 h 15 min. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. For periods greater than 4 hours, the alarm function can be used. Registers 01h, 0Eh and 0Fh are used to control the timer function and output.

8.6.1 Register Timer_clkout

Table 25. Timer_clkout - timer control register (address 0Eh) bit description

Bit	Symbol	Value	Description	Reference
7	-	-	unused	-
6 to 4	COF[2:0]	[1]	CLKOUT control	Section 8.8
3	TE	0	countdown timer is disabled	Section 8.6.4
		1	countdown timer is enabled	
2	-	-	unused	
1 to 0	CTD[1:0]	00	4.096 kHz countdown timer source clock	
		01	64 Hz countdown timer source clock	
		10	1 Hz countdown timer source clock	
		11[2]	$^1/_{60}$ Hz countdown timer source clock	

[1] Values of COF[2:0] see Table 36.

[2] Default value.

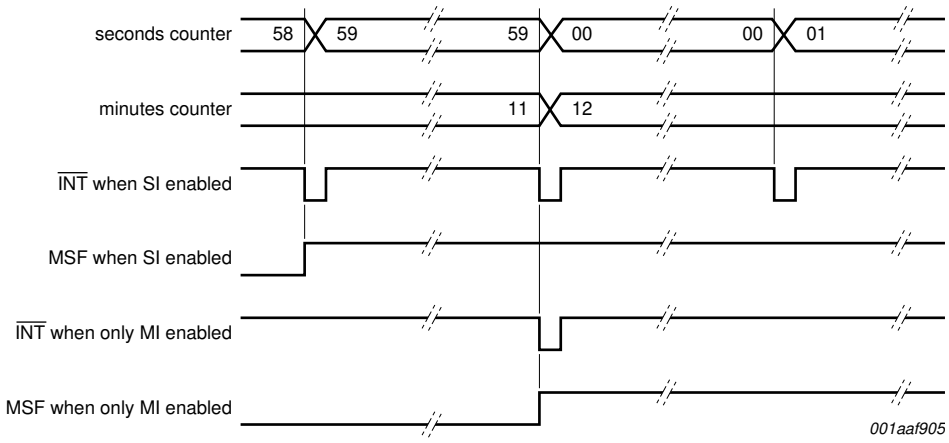
8.6.2 Register Countdown_timer

Table 26. Countdown_timer - countdown timer register (address 0Ah) bit description

Bit	Symbol	Value	Description	Reference
7 to 0	COUNTDOWN_TIMER[7:0]	0h to FFh	countdown period in seconds: $CountdownPeriod = \frac{n}{SourceClockFrequency}$ where n is the countdown value	Section 8.6.4

8.6.3 Minute and second interrupt

The minute and second interrupts (bits MI and SI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time; see Figure 14.



In this example, TI_TP is set to logic 1 resulting in $^{1}/_{64}$ Hz wide interrupt pulse and the MSF flag is not cleared after an interrupt.

Fig 14. $\overline{\text{INT}}$ example for MI and SI

Table 27. Effect of bits MI and SI on $\overline{\text{INT}}$ generation

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	no interrupt generated
1	0	an interrupt once per minute
0	1	an interrupt once per second
1	1	an interrupt once per second

The minute and second flag (bit MSF) is set logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the $\overline{\text{INT}}$ pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an $\overline{\text{INT}}$ pulse will still be generated.

The purpose of the flag is to allow the controlling system to interrogate the PCF2123 and identify the source of the interrupt, i.e., minute or second, countdown timer or alarm.

Table 28. Effect of MI and SI on MSF

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	MSF never set
1	0	MSF set when **minutes** counter increments
0	1	MSF set when **seconds** counter increments
1	1	MSF set when **seconds** counter increments

The duration of both of these timers will be affected by the register Offset_register (see Section 8.9). Only when the Offset_register has the value 00h the periods will be consistent.

8.6.4 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the register Timer_clkout at address 0Eh. The register Timer_clkout selects one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $^1/_{60}$ Hz) and enables or disables the timer.

Table 29. Bits CTD0 and CTD1 for timer frequency selection and countdown timer durations

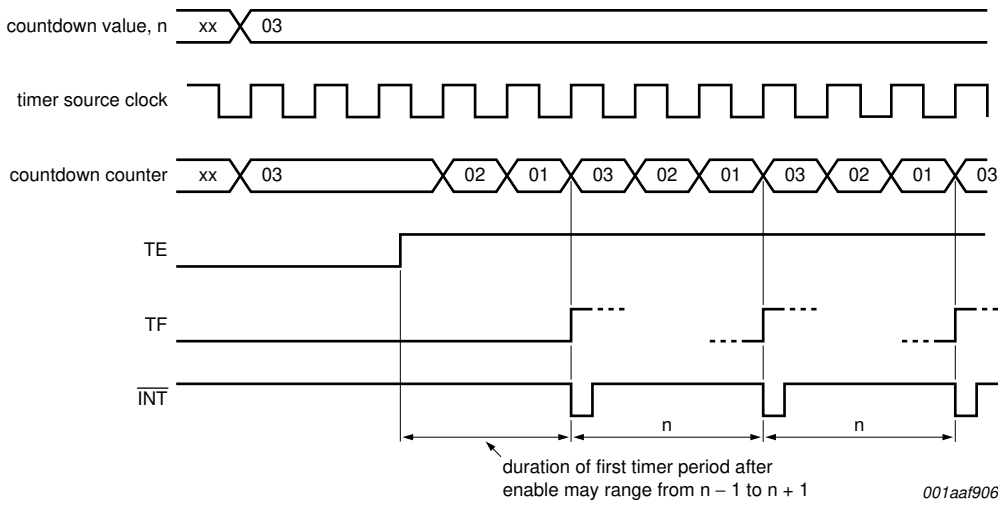
CTD[1:0]	Timer source clock frequency[1]	Delay	
		Minimum timer duration n = 1	Maximum timer duration n = 255
00	4.096 kHz	244 μs	62.256 ms
01	64 Hz	15.625 ms	3.984 s
10	1 Hz[2]	1 s	255 s
11	$^1/_{60}$ Hz[2]	60 s	4 h 15 min

[1] When not in use, CTD must be set to $^1/_{60}$ Hz for power saving.

[2] Time periods can be affected by correction pulses.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value, n. Loading the counter with 0 stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF) will be set and the counter automatically re-loads and starts the next timer period. Reading the timer will return the current value of the countdown counter (see Figure 15).



In this example it is assumed that the timer flag is cleared before the next countdown period expires and that the pin $\overline{INT}$ is set to pulsed mode.

Fig 15. General countdown timer behavior

If a new value of n is written before the end of the current timer period, then this value will take immediate effect. NXP does not recommend changing n without first disabling the counter (by setting bit TE = 0). The update of n is asynchronous to the timer clock,

therefore changing it without setting bit TE = 0 may result in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value n will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ will be generated provided that this mode is enabled. See Section 8.7.2 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods will have no such delay. The amount of delay for the first timer period will depend on the chosen source clock, see Table 30.

Table 30. First period delay for timer counter value n

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n − 1) + $^1/_{64}$ Hz	n + $^1/_{64}$ Hz
$^1/_{60}$ Hz	(n − 1) + $^1/_{64}$ Hz	n + $^1/_{64}$ Hz

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF may only be cleared by software. The asserted bit TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE, see Table 8.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1 Hz and $^1/_{60}$ Hz will be affected by the Offset_register. The duration of a program period will vary according to when the offset is initiated. For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain correction pulses and therefor be longer or shorter depending on the setting of the Offset_register. See Section 8.9 to understand the operation of the Offset_register.

8.6.5 Timer flags

When a minute or second interrupt occurs, bit MSF is set logic 1. Similarly, at the end of a timer countdown or alarm event, bit TF or AF are set logic 1. These bits maintain their value until overwritten by software. If both countdown timer and minute or second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logical AND is performed during a write access. A flag is cleared by writing logic 0 whilst a flag is not cleared by writing logic 1. Writing logic 1 will result in the flag value remaining unchanged.

Three examples are given for clearing the flags. Clearing the flags is made by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

Table 31. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 32, Table 33, and Table 34 show what instruction must be sent to clear the appropriate flag.

Table 32. Example to clear only TF (bit 2) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	1	0	-	-

Table 33. Example to clear only MSF (bit 5) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	1	-	-

Table 34. Example to clear both TF and MSF (bit 2 and bit 5) in register Control_2

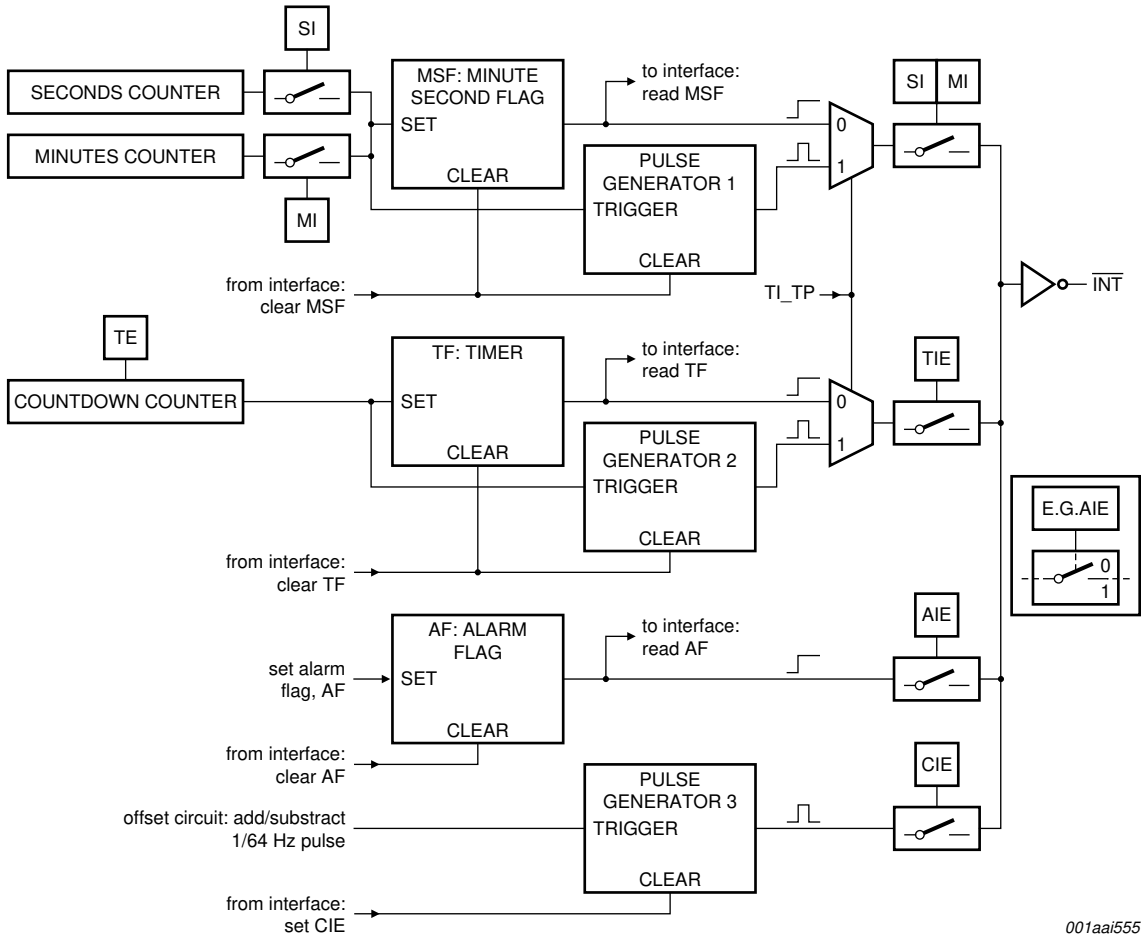
Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	0	-	-

Clearing the alarm flag (bit AF) operates in exactly the same way, see Section 8.5.5.

8.7 Interrupt output

An active LOW interrupt signal is available at pin $\overline{INT}$. Operation is controlled via the bits of register Control_2. Interrupts may be sourced from four places: second and minute timer, countdown timer, alarm function or offset function.

With bit TI_TP, the timer generated interrupts can be configured to either generate a pulse or to follow the status of the interrupt flags (bits TF and MSF). Correction interrupt pulses are always $^{1}/_{128}$ second long. Alarm interrupts always follow the condition of AF.



When bits SI, MI, TIE, AIE, and CIE are all disabled, pin $\overline{INT}$ will remain high-impedance.

Fig 16. Interrupt scheme

Remark: Note that the interrupts from the four sources are wired-OR, meaning they will mask one another (see Figure 16).