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PCF2127AT

Integrated RTC, TCXO and quartz crystal

Rev. 6 — 11 July 2013 **Product data sheet**

1. General description

The PCF2127AT[1] is a CMOS[2] Real Time Clock (RTC) and calendar with an integrated Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal optimized for very high accuracy and very low power consumption. The PCF2127AT has 512 bytes of general purpose static RAM, a selectable I^2C-bus or SPI-bus, a backup battery switch-over circuit, a programmable watchdog function, a timestamp function, and many other features.

2. Features and benefits

- Temperature Compensated Crystal Oscillator (TCXO) with integrated capacitors
- Typical accuracy: ±3 ppm from −15 °C to +60 °C
- Integration of a 32.768 kHz quartz crystal and oscillator in the same package
- Provides year, month, day, weekday, hours, minutes, seconds, and leap year correction
- 512 bytes of general purpose static RAM
- Timestamp function
  - with interrupt capability
  - detection of two different events on one multilevel input pin (for example, for tamper detection)
- Two line bidirectional 400 kHz Fast-mode I^2C-bus interface (I_{OL} = 3 mA at pin SDA/$\overline{CE}$)
- 3 line SPI-bus with separate data input and output (maximum speed 6.5 Mbit/s)
- Battery backup input pin and switch-over circuitry
- Battery backed output voltage
- Battery low detection function
- Extra power fail detection function with input and output pins
- Power-On Reset Override (PORO)
- Oscillator stop detection function
- Interrupt output and system reset pin (open-drain)
- Programmable 1 second or 1 minute interrupt
- Programmable countdown timer with interrupt capability
- Programmable watchdog timer with interrupt and reset capability
- Programmable alarm function with interrupt capability
- Programmable square wave open-drain output pin

1. As well as the PCF2129.
2. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

- Clock operating voltage: 1.2 V to 4.2 V
- Low supply current: typical 0.65 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C

3. Applications

- Electronic metering for electricity, water, and gas
- Precision timekeeping
- Access to accurate time of the day
- GPS equipment to reduce time to first fix
- Applications that require an accurate process timing
- Products with long automated unattended operation time

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2127AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4.1 Ordering options

Table 2. Ordering options

Product type number	IC revision	Sales item (12NC)	Delivery form
PCF2127AT/1[1]	1	935290953512	tube, dry pack
		935290953518	tape and reel, 13 inch, dry pack
PCF2127AT/2	2	935299867518	tape and reel, 13 inch, dry pack

[1] Not to be used for new designs. Replacement part is PCF2127AT/2.

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCF2127AT/1	PCF2127AT
PCF2127AT/2	PCF2127AT

6. Block diagram

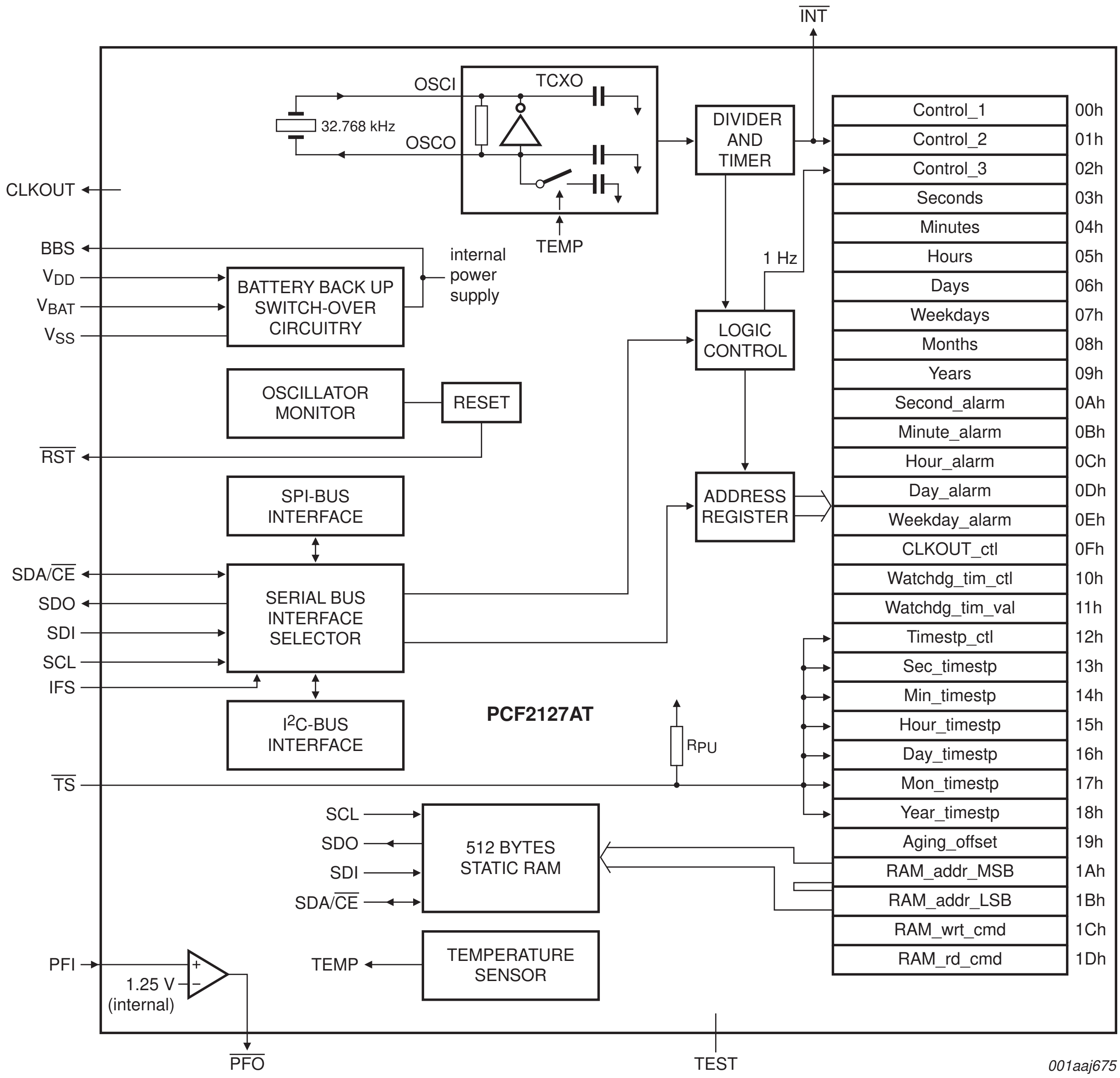
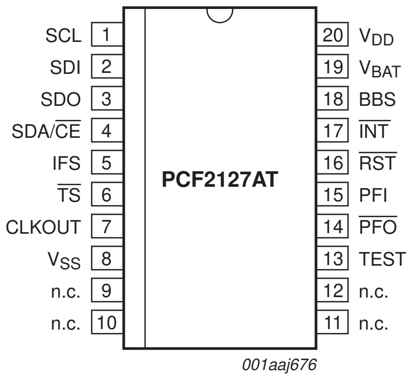


Fig 1. Block diagram of PCF2127AT

7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 53.

Fig 2. Pin configuration for SO20 (PCF2127AT)

7.2 Pin description

Table 4. Pin description of SO20 (PCF2127AT)

Symbol	Pin	Description
SCL	1	combined serial clock input for both I^2C-bus and SPI-bus
SDI	2	serial data input for SPI-bus; connect to pin V_{SS} if I^2C-bus is selected
SDO	3	serial data output for SPI-bus, push-pull
SDA/$\overline{\text{CE}}$	4	combined serial data input and output for the I^2C-bus and chip enable input (active LOW) for the SPI-bus
IFS	5	interface selector input connect to pin V_{SS} to select the SPI-bus connect to pin BBS to select the I^2C-bus
$\overline{\text{TS}}$	6	timestamp input (active LOW) with 200 kΩ internal pull-up resistor (R_{PU})
CLKOUT	7	clock output (open-drain)
V_{SS}	8	ground supply voltage
n.c.	9 to 12	not connected; do not connect; do not use as feed through
TEST	13	do not connect; do not use as feed through
$\overline{\text{PFO}}$	14	power fail output (open-drain; active LOW)
PFI	15	power fail input
$\overline{\text{RST}}$	16	reset output (open-drain; active LOW)
$\overline{\text{INT}}$	17	interrupt output (open-drain; active LOW)

Table 4. Pin description of SO20 (PCF2127AT) *…continued*

Symbol	Pin	Description
BBS	18	output voltage (battery backed)
V_{BAT}	19	battery supply voltage (backup) connect to V_{SS} if battery switch over is not used
V_{DD}	20	supply voltage

8. Functional description

The PCF2127AT is a Real Time Clock (RTC) and calendar with an on-chip Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal integrated into the same package (see Section 8.3.2).

Address and data are transferred by a selectable 400 kHz Fast-mode I^2C-bus or a 3 line SPI-bus with separate data input and output (see Section 9). The maximum speed of the SPI-bus is 6.5 Mbit/s.

The PCF2127AT has a backup battery input pin and backup battery switch-over circuit which monitors the main power supply. The backup battery switch-over circuit automatically switches to the backup battery when a power failure condition is detected (see Section 8.6.1). Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery (see Section 8.6.3). When the battery voltage drops below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

8.1 Register overview

The PCF2127AT contains an auto-incrementing address register: the built-in address register will increment automatically after each read or write of a data byte up to the register 1Bh. After register 1Bh, the auto-incrementing will wrap around to address 00h (see Figure 3).

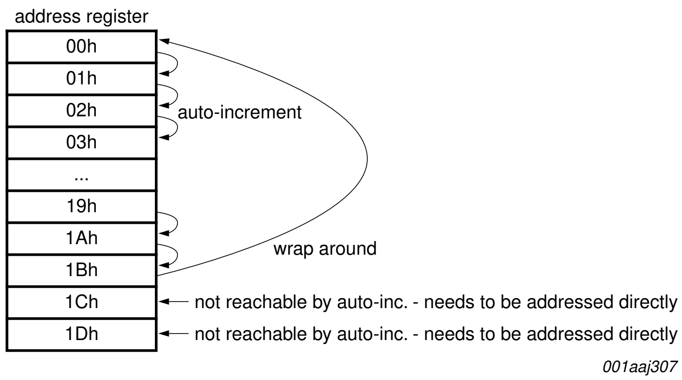


Fig 3. Handling address registers

- The first three registers (memory address 00h, 01h, and 02h) are used as control registers (see Section 8.2).
- The registers at addresses 03h through to 09h are used as counters for the clock function (seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see Section 8.9).
- The registers at addresses 0Ah through 0Eh define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see Section 8.10).

- The register at address 0Fh defines the temperature measurement period and the clock out mode. The temperature measurement can be selected from every 4 minutes (default) down to every 30 seconds (see Table 10). CLKOUT frequencies of 32.768 kHz (default) down to 1 Hz for use as system clock, microcontroller clock, and so on, can be chosen (see Table 11).
- The registers at addresses 10h and 11h are used for the watchdog and countdown timer functions. The watchdog timer has four selectable source clocks allowing for timer periods from less than 1 ms to greater than 4 hours (see Table 37). Either the watchdog timer **or** the countdown timer can be enabled (see Section 8.11). For the watchdog timer, it is possible to select whether an interrupt or a pulse on the reset pin will be generated when the watchdog times out. For the countdown timer, it is only possible that an interrupt will be generated at the end of the countdown.
- The registers at addresses 12h to 18h are used for the timestamp function. When the trigger event happens, the actual time is saved in the timestamp registers (see Section 8.12).
- The register at address 19h is used for the correction of the crystal aging effect (see Section 8.4.1).
- The registers at addresses 1Ah and 1Bh define the RAM address. The register at address 1Ch (RAM_wrt_cmd) is the RAM write command; the register at 1Dh (RAM_rd_cmd) is the RAM read command. Data is transferred to or from the RAM by the serial interface (see Section 8.5).
- The registers Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

When one of the RTC registers is written or read, the content of all counters is temporarily frozen. This prevents a faulty writing or reading of the clock and calendar during a carry condition (see Section 8.9.8).

Table 5. Register overview

Bit positions labeled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value
		7	6	5	4	3	2	1	0	
Control registers										
00h	Control_1	EXT_ TEST	T	STOP	TSF1	POR_ OVRD	12_24	MI	SI	0000 0000
01h	Control_2	MSF	WDTF	TSF2	AF	CDTF	TSIE	AIE	CDTIE	0000 0000
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE	0000 0000
Time and date registers										
03h	Seconds	OSF	SECONDS (0 to 59)							1XXX XXXX
04h	Minutes	-	MINUTES (0 to 59)							- XXX XXXX
05h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 h mode					- - XX XXXX
				HOURS (0 to 23) in 24 h mode						- - XX XXXX
06h	Days	-	-	DAYS (1 to 31)						- - XX XXXX
07h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			- - - - - XXX
08h	Months	-	-	-	MONTHS (1 to 12)					- - - X XXXX
09h	Years	YEARS (0 to 99)								XXXX XXXX
Alarm registers										
0Ah	Second_alarm	AE_S	SECOND_ALARM (0 to 59)							1XXX XXXX
0Bh	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)							1XXX XXXX
0Ch	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12 h mode					1 - XX XXXX
			-	HOUR_ALARM (0 to 23) in 24 h mode						1 - XX XXXX
0Dh	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)						1 - XX XXXX
0Eh	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)			1 - - - - XXX
CLKOUT control register										
0Fh	CLKOUT_ctl	TCR[1:0]		-	-	-	COF[2:0]			00 - - - 000
Watchdog registers										
10h	Watchdg_tim_ctl	WD_CD[1:0]		TI_TP	-	-	-	TF[1:0]		000 - - - 11
11h	Watchdg_tim_val	WATCHDG_TIM_VAL[7:0]								XXXX XXXX
Timestamp registers										
12h	Timestp_ctl	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]					00 - X XXXX
13h	Sec_timestp	-	SECOND_TIMESTP (0 to 59)							- XXX XXXX
14h	Min_timestp	-	MINUTE_TIMESTP (0 to 59)							- XXX XXXX
15h	Hour_timestp	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12 h mode					- - XX XXXX
				HOUR_TIMESTP (0 to 23) in 24 h mode						- - XX XXXX
16h	Day_timestp	-	-	DAY_TIMESTP (1 to 31)						- - XX XXXX
17h	Mon_timestp	-	-	-	MONTH_TIMESTP (1 to 12)					- - - X XXXX
18h	Year_timestp	YEAR_TIMESTP (0 to 99)								XXXX XXXX
Aging offset register										
19h	Aging_offset	-	-	-	-	AO[3:0]				- - - - 1000

Table 5. Register overview *...continued*

Bit positions labeled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value
		7	6	5	4	3	2	1	0	
RAM registers										
1Ah	RAM_addr_MSB	-	-	-	-	-	-	-	RA8	- - - - - - - 0
1Bh	RAM_addr_LSB	RA[7:0]								0000 0000
1Ch	RAM_wrt_cmd	X	X	X	X	X	X	X	X	XXXX XXXX
1Dh	RAM_rd_cmd	X	X	X	X	X	X	X	X	XXXX XXXX

8.2 Control registers

The first 3 registers of the PCF2127AT, with the addresses 00h, 01h, and 02h, are used as control registers.

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value		Description	Reference
7	EXT_TEST	0	[1]	normal mode	Section 8.14
		1		external clock test mode	
6	T	0	[2]	unused	-
5	STOP	0	[1]	RTC source clock runs	Section 8.15
		1		RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available	
4	TSF1	0	[1]	no timestamp interrupt generated	Section 8.12.1
		1		flag set when $\overline{TS}$ input is driven to an intermediate level between power supply and ground; flag must be cleared to clear interrupt	
3	POR_OVRD	0	[1]	Power-On Reset Override (PORO) facility disabled; **set logic 0 for normal operation**	Section 8.8.2
		1		Power-On Reset Override (PORO) sequence reception enabled	
2	12_24	0	[1]	24 hour mode selected	Table 23
		1		12 hour mode selected	
1	MI	0	[1]	minute interrupt disabled	Section 8.13
		1		minute interrupt enabled	
0	SI	0	[1]	second interrupt disabled	
		1		second interrupt enabled	

[1] Default value.

[2] When writing to the register this bit always has to be set logic 0.

8.2.2 Register Control_2

Table 7. Control_2 - control and status register 2 (address 01h) bit description

Bit	Symbol	Value		Description	Reference
7	MSF	0	[1]	no minute or second interrupt generated	Section 8.13
		1		flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
6	WDTF	0	[1]	no watchdog timer interrupt or reset generated	Section 8.13.4
		1		flag set when watchdog timer interrupt or reset generated; flag cannot be cleared by command (read-only)	
5	TSF2	0	[1]	no timestamp interrupt generated	Section 8.12.1
		1		flag set when $\overline{TS}$ input is driven to ground; flag must be cleared to clear interrupt	
4	AF	0	[1]	no alarm interrupt generated	Section 8.10.6
		1		flag set when alarm triggered; flag must be cleared to clear interrupt	
3	CDTF	0	[1]	no countdown timer interrupt generated	Section 8.11.4
		1		flag set when countdown timer interrupt generated; flag must be cleared to clear interrupt	
2	TSIE	0	[1]	no interrupt generated from timestamp flag	Section 8.13.6
		1		interrupt generated when timestamp flag set	
1	AIE	0	[1]	no interrupt generated from the alarm flag	Section 8.13.5
		1		interrupt generated when alarm flag set	
0	CDTIE	0	[1]	no interrupt generated from countdown timer flag	Section 8.13.2
		1		interrupt generated when countdown timer flag set	

[1] Default value.

8.2.3 Register Control_3

Table 8. Control_3 - control and status register 3 (address 02h) bit description

Bit	Symbol	Value	Description	Reference
7 to 5	PWRMNG[2:0]	[1]	control of the battery switch-over, battery low detection, and extra power fail detection functions	Section 8.6
4	BTSE	0 [2]	no timestamp when battery switch-over occurs	Section 8.12.4
		1	time-stamped when battery switch-over occurs	
3	BF	0 [2]	no battery switch-over interrupt generated	Section 8.6.1
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt	
2	BLF	0 [2]	battery status ok; no battery low interrupt generated	Section 8.6.3
		1	battery status low; flag cannot be cleared by command	
1	BIE	0 [2]	no interrupt generated from the battery flag (BF)	Section 8.13.7
		1	interrupt generated when BF is set	
0	BLIE	0 [2]	no interrupt generated from battery low flag (BLF)	Section 8.13.8
		1	interrupt generated when BLF is set	

[1] Values see Table 18.

[2] Default value.

8.3 Register CLKOUT_ctl

Table 9. CLKOUT_ctl - CLKOUT control register (address 0Fh) bit description

Bit	Symbol	Value	Description
7 to 6	TCR[1:0]	see Table 10	temperature measurement period
5 to 3	-	-	unused
2 to 0	COF[2:0]	see Table 11	CLKOUT frequency selection

8.3.1 Temperature compensated crystal oscillator

The frequency of tuning fork quartz crystal oscillators is temperature-dependent. In the PCF2127AT, the frequency deviation caused by temperature variation is corrected by adjusting the load capacitance of the crystal oscillator.

The load capacitance is changed by switching between two load capacitance values using a modulation signal with a programmable duty cycle. In order to compensate the spread of the quartz parameters every chip is factory calibrated.

The frequency accuracy can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT. However, the selection of f_{CLKOUT} = 32.768 kHz (default value) leads to inaccurate measurements. Accurate frequency measurement occurs when f_{CLKOUT} = 16.384 kHz or lower is selected (see Table 11).

8.3.1.1 Temperature measurement

The PCF2127AT has a temperature sensor circuit used to perform the temperature compensation of the frequency. The temperature is measured immediately after power-on and then periodically with a period set by the temperature conversion rate TCR[1:0] in the register CLKOUT_ctl.

Table 10. Temperature measurement period

TCR[1:0]		Temperature measurement period
00	[1]	4 min
01		2 min
10		1 min
11		30 seconds

[1] Default value.

8.3.2 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] control bits in register CLKOUT_ctl. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as system clock, microcontroller clock, charge pump input, or for calibrating the oscillator.

CLKOUT is an open-drain output and enabled at power-on. When disabled, the output is high-impedance.

The duty cycle of the selected clock is not controlled, however, due to the nature of the clock generation all but the 32.768 kHz frequencies will be 50 : 50.

Table 11. CLKOUT frequency selection

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]
000[2][3]	32768	60 : 40 to 40 : 60
001	16384	50 : 50
010	8192	50 : 50
011	4096	50 : 50
100	2048	50 : 50
101	1024	50 : 50
110	1	50 : 50
111	CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] The specified accuracy of the RTC can be only achieved with CLKOUT frequencies not equal to 32.768 kHz or if CLKOUT is disabled.

8.4 Register Aging_offset

Table 12. Aging_offset - crystal aging offset register (address 19h) bit description

Bit	Symbol	Value	Description
7 to 4	-	-	unused
3 to 0	AO[3:0]	see Table 13	aging offset value

8.4.1 Crystal aging correction

The PCF2127AT has an offset register Aging_offset to correct the crystal aging effects[3].

The accuracy of the frequency of a quartz crystal depends on its aging. The aging offset adds an adjustment, positive or negative, in the temperature compensation circuit which allows correcting the aging effect.

At 25 °C, the aging offset bits allow a frequency correction of typically 1 ppm per AO[3:0] value, from –7 ppm to +8 ppm.

Table 13. Frequency correction at 25 °C, typical

AO[3:0]		ppm
Decimal	Binary	
0	0000	+8
1	0001	+7
2	0010	+6
3	0011	+5
4	0100	+4
5	0101	+3
6	0110	+2
7	0111	+1
8	1000 [1]	0
9	1001	–1
10	1010	–2
11	1011	–3
12	1100	–4
13	1101	–5
14	1110	–6
15	1111	–7

[1] Default value.

3. For further information, refer to the application note Ref. 3 "AN10857".

8.5 General purpose 512 bytes static RAM

The PCF2127AT contains a general purpose 512 bytes static RAM. This integrated SRAM is battery backed and can therefore be used to store data which is essential for the application to survive a power outage.

9 bits, RA[8:0], define the RAM address pointer in registers RAM_addr_MSB and RAM_addr_LSB. The register address pointer increments after each read or write automatically up to 1Bh and then wraps around to address 00h (see Figure 3 on page 6).

Data is transferred to or from the RAM by the interface. To write to the RAM, the register RAM_wrt_cmd, to read from the RAM the register RAM_rd_cmd must be addressed explicitly.

8.5.1 Register RAM_addr_MSB

Table 14. RAM_addr_MSB - RAM address MSB register (address 1Ah) bit description

Bit	Symbol	Description
7 to 1	-	unused
0	RA8	RAM address, MSB (9th bit)

8.5.2 Register RAM_addr_LSB

Table 15. RAM_addr_LSB - RAM address LSB register (address 1Bh) bit description

Bit	Symbol	Description
7 to 0	RA[7:0]	RAM address, LSB (1st to 8th bit)

8.5.3 Register RAM_wrt_cmd

Table 16. RAM_wrt_cmd - RAM write command register (address 1Ch) bit description

Bit	Symbol	Description
7 to 0	-	data to be written into RAM

8.5.4 Register RAM_rd_cmd

Table 17. RAM_rd_cmd - RAM read command register (address 1Dh) bit description

Bit	Symbol	Description
7 to 0	-	data to be read from RAM

8.5.5 Operation examples

8.5.5.1 Writing to the RAM

1. Set RAM address:
   - Select register RAM_addr_MSB (send address 1Ah).
   - Set value for bit RA8 (data byte of register 1Ah).
     Note: register address will be incremented automatically to 1Bh.
   - Set value for array RA[7:0] (data byte of register 1Bh).
2. Send RAM write command:
   - Select register RAM_wrt_cmd (send address 1Ch).
3. Write data into the RAM:
   - Write n data byte into RAM.

For details, see Figure 44 on page 62.

8.5.5.2 Reading from the RAM

1. Set RAM address:
   - Select register RAM_addr_MSB (send address 1Ah).
   - Set value for bit RA8 (data byte of register 1Ah).
     Note: register address will be incremented automatically to 1Bh.
   - Set value for array RA[7:0] (data byte of register 1Bh).
2. Send RAM read command:
   - Select register RAM_rd_cmd (send address 1Dh).
3. Read from the RAM:
   - Read n data byte from the RAM.

For details, see Figure 45 on page 63.

8.6 Power management functions

The PCF2127AT has two power supply pins and one power output pin:

- V_{DD} - the main power supply input pin
- V_{BAT} - the battery backup input pin
- BBS - battery backed output voltage pin (equal to the internal power supply)

The PCF2127AT has three power management functions implemented:

- Battery switch-over function
- Battery low detection function
- Extra power fail detection function

The power management functions are controlled by the control bits PWRMNG[2:0] in register Control_3:

Table 18. Power management control bit description

PWRMNG[2:0]		Function
000	[1]	battery switch-over function is enabled in standard mode; battery low detection function is enabled; extra power fail detection function is enabled
001		battery switch-over function is enabled in standard mode; battery low detection function is disabled; extra power fail detection function is enabled
010		battery switch-over function is enabled in standard mode; battery low detection function is disabled; extra power fail detection function is disabled
011		battery switch-over function is enabled in direct switching mode; battery low detection function is enabled; extra power fail detection function is enabled
100		battery switch-over function is enabled in direct switching mode; battery low detection function is disabled; extra power fail detection function is enabled
101		battery switch-over function is enabled in direct switching mode; battery low detection function is disabled; extra power fail detection function is disabled
110	[2]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is disabled; extra power fail detection function is enabled
111	[2]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is disabled; extra power fail detection function is disabled

[1] Default value.

[2] When the battery switch-over function is disabled, the PCF2127AT works only with the power supply V_{DD}; V_{BAT} must be put to ground and the battery low detection function is disabled.

8.6.1 Battery switch-over function

The PCF2127AT has a backup battery switch-over circuit which monitors the main power supply V_{DD}. When a power failure condition is detected, it automatically switches to the backup battery.

One of two operation modes can be selected:

- **Standard mode:** the power failure condition happens when:
  $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$
  $V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. The battery switch-over in standard mode works only for $V_{DD} > 2.5$ V.
- **Direct switching mode:** the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BF (register Control_3) is set logic 1.
2. An interrupt is generated if the control bit BIE (register Control_3) is enabled (see Section 8.13.7).
3. If the control bit BTSE (register Control_3) is logic 1, the timestamp registers store the time and date when the battery switch occurred (see Section 8.12.4).
4. The battery switch flag BF is cleared by command; it must be cleared to clear the interrupt.

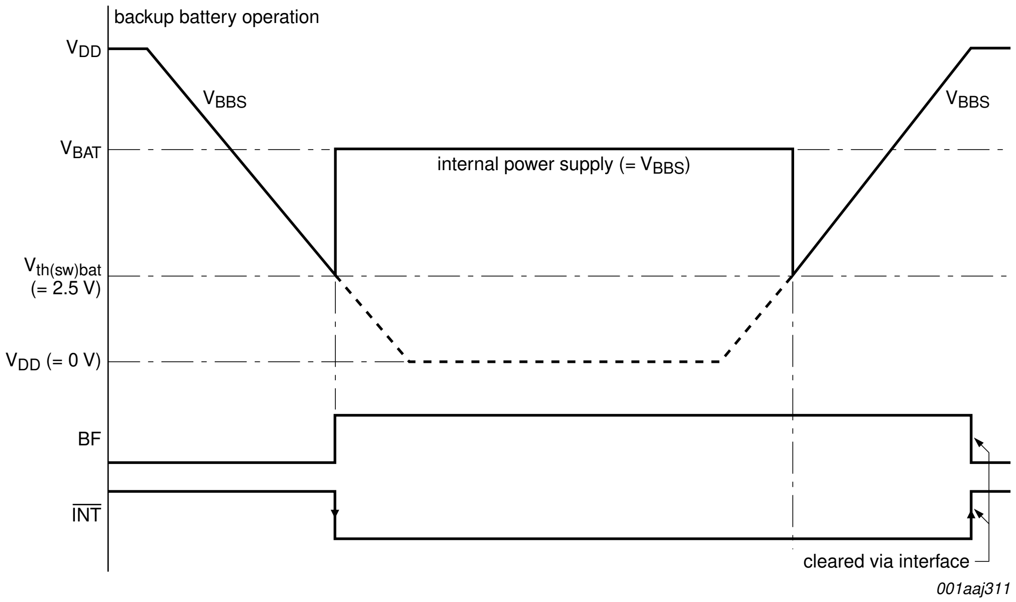
The interface is disabled in battery backup operation:

- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

8.6.1.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$, the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$, the internal power supply is V_{BAT}.



$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. In standard mode, the battery switch-over works only for $V_{DD} > 2.5$ V.

V_{DD} may be lower than V_{BAT} (for example $V_{DD} = 3$ V, $V_{BAT} = 4.1$ V).

Fig 4. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled)

8.6.1.2 Direct switching mode

If $V_{DD} > V_{BAT,}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$, the internal power supply is V_{BAT}.

The direct switching mode is useful in systems where V_{DD} is higher than V_{BAT} at all times. This mode is not recommended if the V_{DD} and V_{BAT} values are similar (for example, $V_{DD} = 3.3$ V, $V_{BAT} \geq 3.0$ V). In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

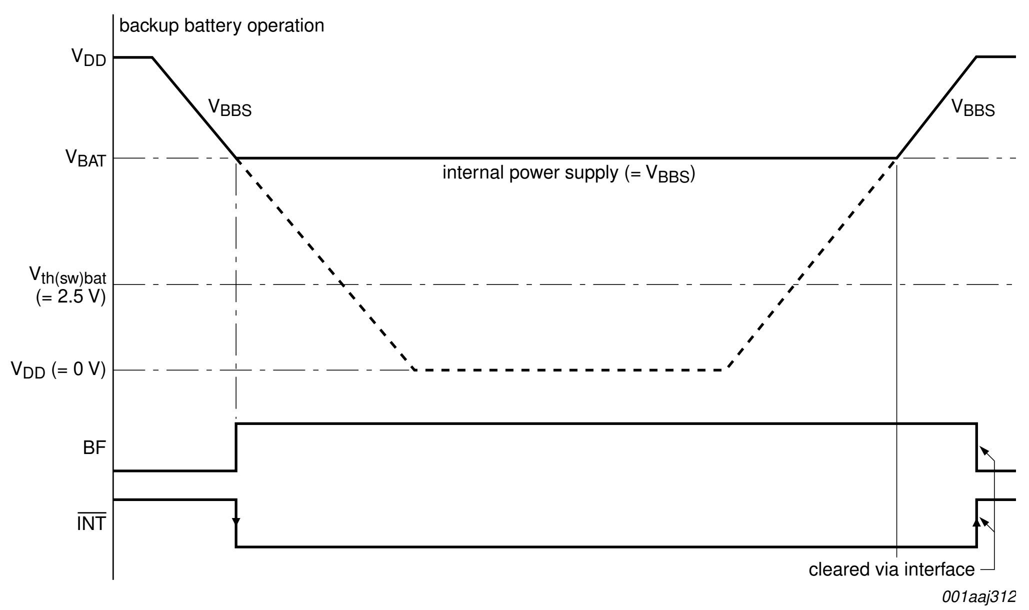


Fig 5. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled)

8.6.1.3 Battery switch-over disabled: only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to ground
- The internal power supply, available at the output pin BBS, is equal to V_{DD}
- The battery flag (BF) is always logic 0

8.6.1.4 Battery switch-over architecture

The architecture of the battery switch-over circuit is shown in Figure 6.

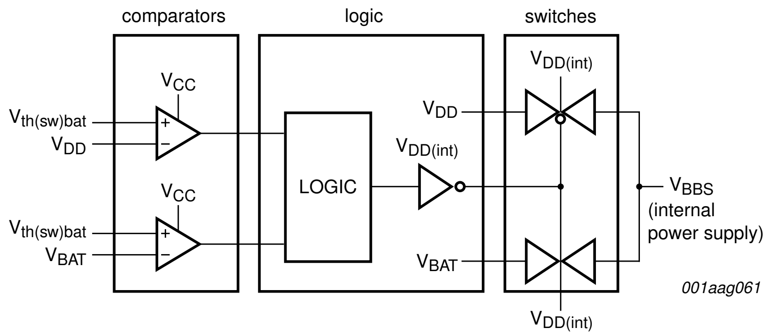


Fig 6. Battery switch-over circuit, simplified block diagram

The internal power supply (available on pin BBS) is equal to V_{DD} or V_{BAT}. It has to be assured that there are decoupling capacitors on the pins V_{DD}, V_{BAT}, and BBS.

8.6.2 Battery backup supply

The V_{BBS} voltage on the output pin BBS is equal to the internal power supply, depending on the selected battery switch-over function mode:

Table 19. Output pin BBS

Battery switch-over function mode	Conditions	V_{BBS} equals
standard	$V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$	V_{DD}
	$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$	V_{BAT}
direct switching	$V_{DD} > V_{BAT}$	V_{DD}
	$V_{DD} < V_{BAT}$	V_{BAT}
disabled	only V_{DD} available, V_{BAT} must be put to ground	V_{DD}

The output pin BBS can be used as a supply for external devices with battery backup needs, such as SRAM (see Ref. 3 “AN10857”). For this case, Figure 7 shows the typical driving capability when V_{BBS} is driven from V_{DD}.

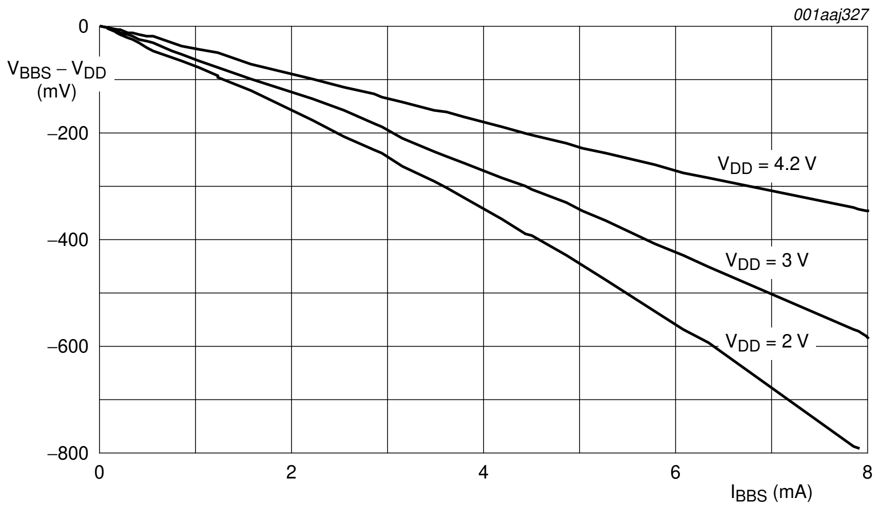


Fig 7. Typical driving capability of V_{BBS}: ($V_{BBS} - V_{DD}$) with respect to the output load current I_{BBS}

8.6.3 Battery low detection function

The PCF2127AT has a battery low detection circuit which monitors the status of the battery V_{BAT}.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typically 2.5 V), the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery cannot prevent that the supply voltage drops below V_{low} (typical 1.2 V) and with that the data integrity gets lost.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 8):

1. The battery low flag BLF is set logic 1.
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled (see Section 8.13.8).
3. The flag BLF remains logic 1 until the battery is replaced. BLF cannot be cleared by command. It is cleared automatically by the battery low detection circuit when the battery is replaced.

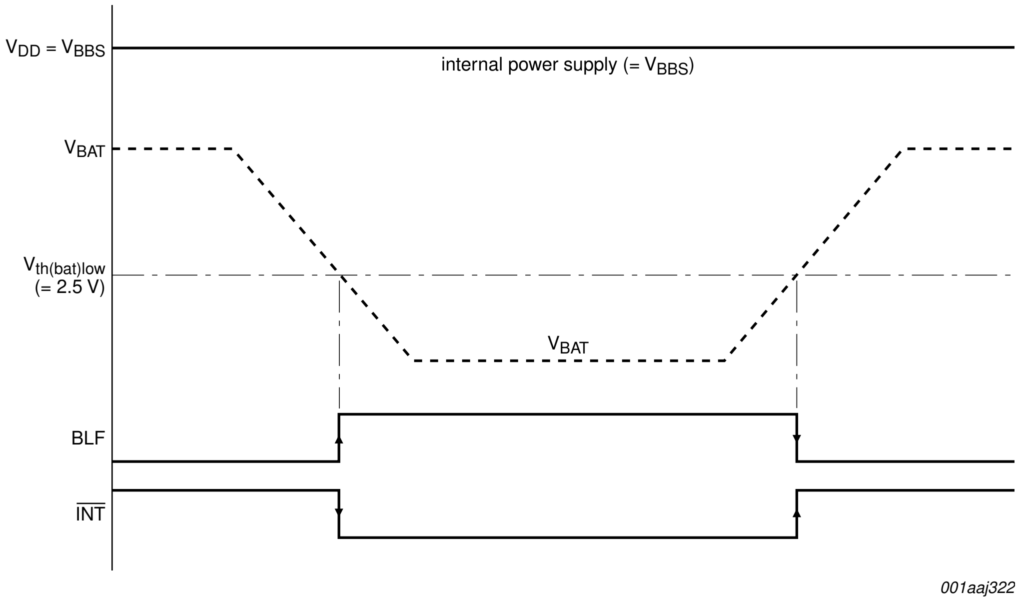


Fig 8. Battery low detection behavior with bit BLIE set logic 1 (enabled)

8.6.4 Extra power fail detection function

The PCF2127AT has an extra power fail detection circuit which compares the voltage at the power fail input pin PFI to an internal reference voltage equal to 1.25 V.

If V_{PFI} < 1.25 V, the power fail output $\overline{PFO}$ is driven LOW. $\overline{PFO}$ is an open-drain, active LOW output which requires an external pull-up resistor in any application.

The extra power fail detection function is typically used as a low voltage detection for the main power supply V_{DD} (see Figure 9).

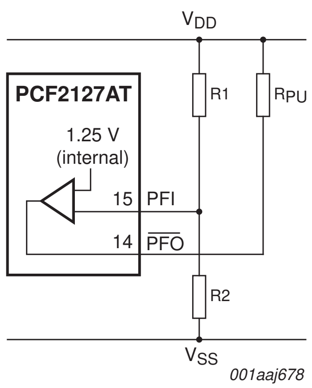


Fig 9. Typical application of the extra power fail detection function

Usually R1 and R2 should be chosen such that the voltage at pin PFI

- is higher than 1.25 V at start-up
- falls below 1.25 V when V_{DD} falls below a desired threshold voltage, $V_{th(uvp)}$, defined by Equation 1:

$$V_{th(uvp)} = \left(\frac{R_1}{R_2} + 1\right) \times 1.25V \quad (1)$$

$V_{th(uvp)}$ value is usually set to a value that there are several milliseconds before V_{DD} falls below the minimum operating voltage of the system, in order to allow the microcontroller to perform early backup operations.

If the extra power fail detection function is not used, pin PFI must be connected to V_{SS} and pin $\overline{\text{PFO}}$ must be left open circuit.

8.6.4.1 Extra power fail detection when the battery switch over function is enabled

- When the power switches to the backup battery supply V_{BAT}, the power fail comparator is switched off and the power fail output at pin $\overline{\text{PFO}}$ goes (or remains) LOW
- When the power switches back to the main V_{DD}, the pin $\overline{\text{PFO}}$ is not driven LOW anymore and is pulled HIGH through the external pull-up resistance for a certain time (t_{rec} = 15.63 ms to 31.25 ms) and then the power fail comparator is enabled again

For illustration, see Figure 10 and Figure 11.

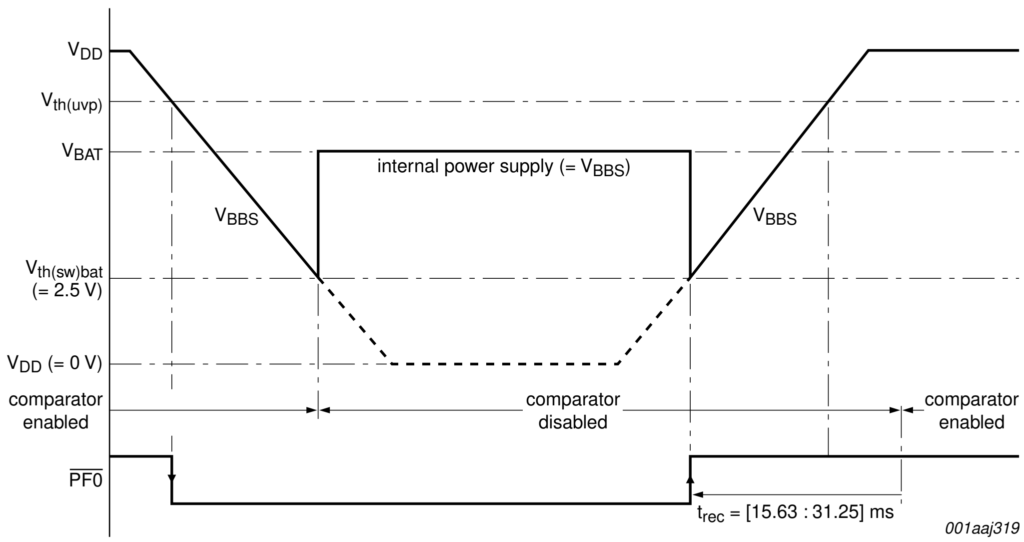


Fig 10. $\overline{\text{PFO}}$ signal behavior when battery switch-over is enabled in standard mode and $V_{th(uvp)} > (V_{BAT}, V_{th(sw)bat})$