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PCF2129

Accurate RTC with integrated quartz crystal for industrial applications

Rev. 7 — 19 December 2014 Product data sheet

1. General description

The PCF2129 is a CMOS[1] Real Time Clock (RTC) and calendar with an integrated Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal optimized for very high accuracy and very low power consumption. The PCF2129 has a selectable I²C-bus or SPI-bus, a backup battery switch-over circuit, a programmable watchdog function, a timestamp function, and many other features.

For a selection of NXP Real-Time Clocks, see Table 83 on page 75

2. Features and benefits

- Operating temperature range from −40 °C to +85 °C
- Temperature Compensated Crystal Oscillator (TCXO) with integrated capacitors
- Typical accuracy:
  - PCF2129AT: ±3 ppm from −15 °C to +60 °C
  - PCF2129T: ±3 ppm from −30 °C to +80 °C
- Integration of a 32.768 kHz quartz crystal and oscillator in the same package
- Provides year, month, day, weekday, hours, minutes, seconds, and leap year correction
- Timestamp function
  - with interrupt capability
  - detection of two different events on one multilevel input pin (for example, for tamper detection)
- Two line bidirectional 400 kHz Fast-mode I²C-bus interface
- 3 line SPI-bus with separate data input and output (maximum speed 6.5 Mbit/s)
- Battery backup input pin and switch-over circuitry
- Battery backed output voltage
- Battery low detection function
- Power-On Reset Override (PORO)
- Oscillator stop detection function
- Interrupt output (open-drain)
- Programmable 1 second or 1 minute interrupt
- Programmable watchdog timer with interrupt
- Programmable alarm function with interrupt capability
- Programmable square output

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

- Clock operating voltage: 1.8 V to 4.2 V
- Low supply current: typical 0.70 μA at V_{DD} = 3.3 V

3. Applications

- Electronic metering for electricity, water, and gas
- Precision timekeeping
- Access to accurate time of the day
- GPS equipment to reduce time to first fix
- Applications that require an accurate process timing
- Products with long automated unattended operation time

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2129AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCF2129T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF2129AT/2	PCF2129AT/2,518	935295732518	tape and reel, 13 inch, dry pack	2
PCF2129T/2	PCF2129T/2,518	935297464518	tape and reel, 13 inch, dry pack	2

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCF2129AT/2	PCF2129AT
PCF2129T/2	PCF2129T

6. Block diagram

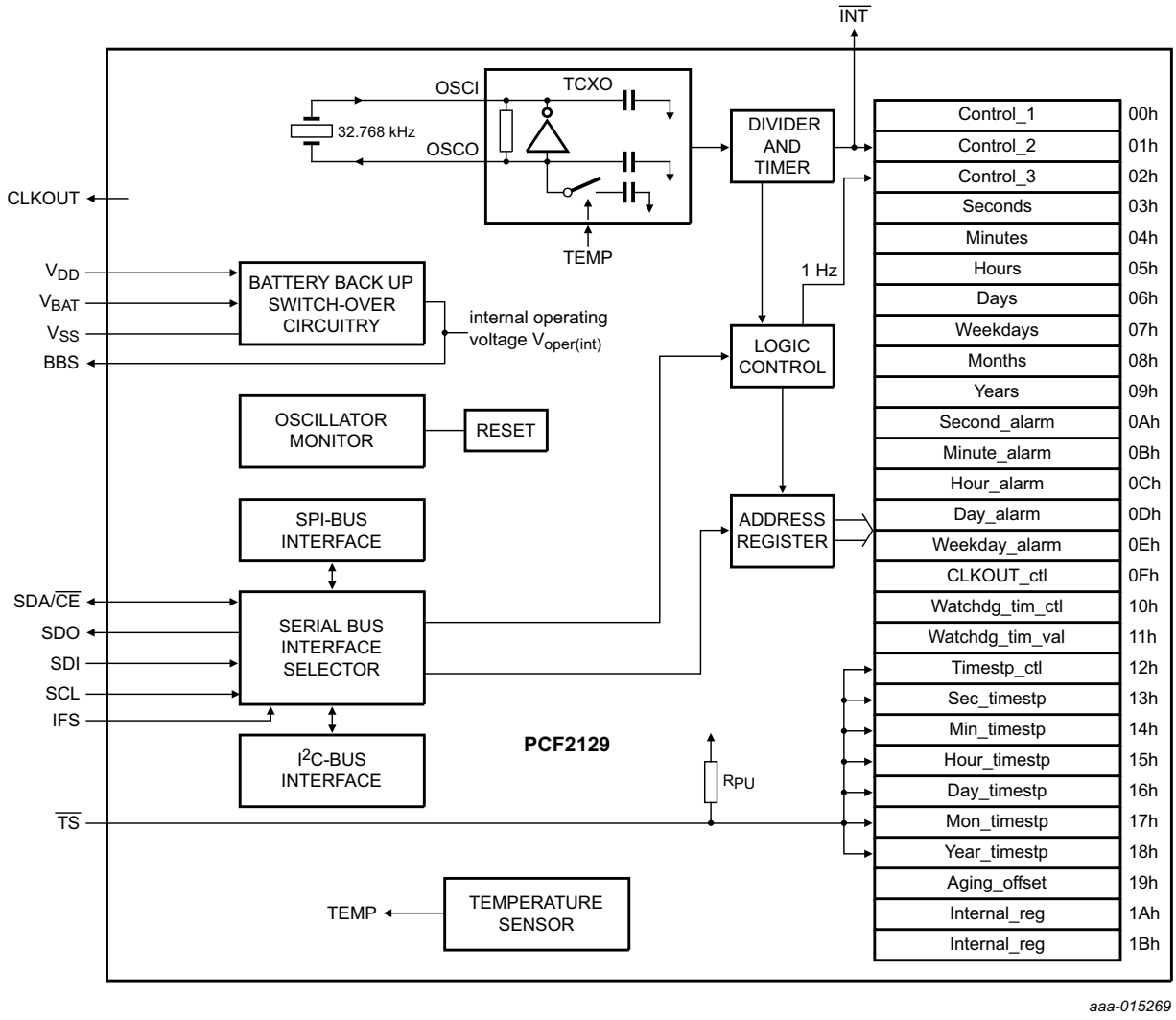
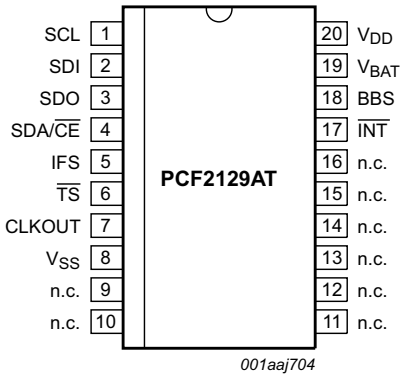


Fig 1. Block diagram of PCF2129

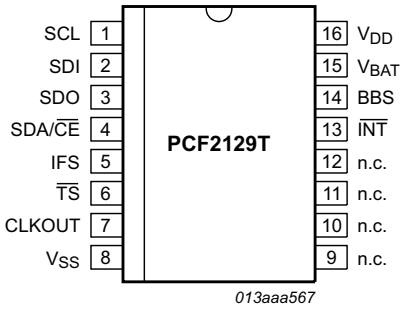
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 50.

Fig 2. Pin configuration for PCF2129AT (SO20)



Top view. For mechanical details, see Figure 50.

Fig 3. Pin configuration for PCF2129T (SO16)

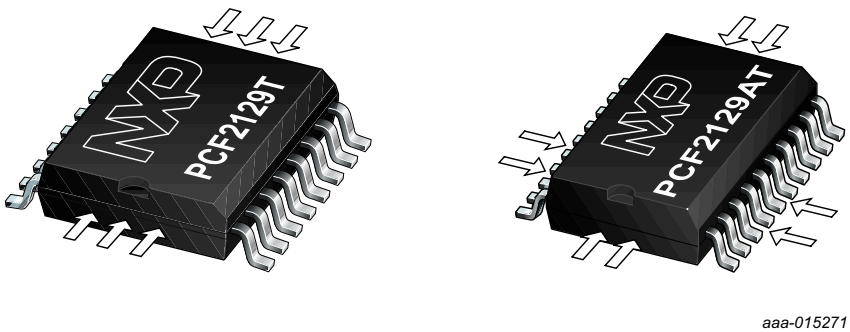


Fig 4. Position of the stubs from the package assembly process

After lead forming and cutting, there remain stubs from the package assembly process. These stubs are present at the edge of the package as illustrated in Figure 4. The stubs are at an electrical potential. To avoid malfunction of the PCF2129, it has to be ensured that they are not shorted with another electrical potential (e.g. by condensation).

7.2 Pin description

Table 4. Pin description of PCF2129

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin		Description
	PCF2129AT	PCF2129T	
SCL	1	1	combined serial clock input for both I²C-bus and SPI-bus
SDI	2	2	serial data input for SPI-bus connect to pin V_{SS} if I²C-bus is selected
SDO	3	3	serial data output for SPI-bus, push-pull
SDA/$\overline{CE}$	4	4	combined serial data input and output for the I²C-bus and chip enable input (active LOW) for the SPI-bus
IFS	5	5	interface selector input connect to pin V_{SS} to select the SPI-bus connect to pin BBS to select the I²C-bus
$\overline{TS}$	6	6	timestamp input (active LOW) with 200 kΩ internal pull-up resistor (R_{PU})
CLKOUT	7	7	clock output (open-drain)
V_{SS}	8	8	ground supply voltage
n.c.	9 to 16	9 to 12	not connected; do not connect; do not use as feed through
$\overline{INT}$	17	13	interrupt output (open-drain; active LOW)
BBS	18	14	output voltage (battery backed)
V_{BAT}	19	15	battery supply voltage (backup) connect to V_{SS} if battery switch over is not used
V_{DD}	20	16	supply voltage

8. Functional description

The PCF2129 is a Real Time Clock (RTC) and calendar with an on-chip Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal integrated into the same package (see Section 8.3.3).

Address and data are transferred by a selectable 400 kHz Fast-mode I^2C-bus or a 3 line SPI-bus with separate data input and output (see Section 9). The maximum speed of the SPI-bus is 6.5 Mbit/s.

The PCF2129 has a backup battery input pin and backup battery switch-over circuit which monitors the main power supply. The backup battery switch-over circuit automatically switches to the backup battery when a power failure condition is detected (see Section 8.5.1). Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery (see Section 8.5.2). When the battery voltage drops below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

8.1 Register overview

The PCF2129 contains an auto-incrementing address register: the built-in address register will increment automatically after each read or write of a data byte up to the register 1Bh. After register 1Bh, the auto-incrementing will wrap around to address 00h (see Figure 5).

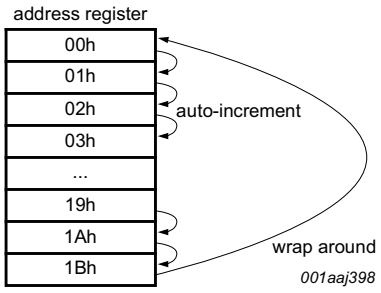


Fig 5. Handling address registers

- The first three registers (memory address 00h, 01h, and 02h) are used as control registers (see Section 8.2).
- The memory addresses 03h through to 09h are used as counters for the clock function (seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see Section 8.8).
- The registers at addresses 0Ah through 0Eh define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see Section 8.9).
- The register at address 0Fh defines the temperature measurement period and the clock out mode. The temperature measurement can be selected from every 4 minutes (default) down to every 30 seconds (see Table 14). CLKOUT frequencies of

32.768 kHz (default) down to 1 Hz for use as system clock, microcontroller clock, and so on, can be chosen (see Table 15).

- The registers at addresses 10h and 11h are used for the watchdog timer functions. The watchdog timer has four selectable source clocks allowing for timer periods from less than 1 ms to greater than 4 hours (see Table 52). An interrupt is generated when the watchdog times out.
- The registers at addresses 12h to 18h are used for the timestamp function. When the trigger event happens, the actual time is saved in the timestamp registers (see Section 8.11).
- The register at address 19h is used for the correction of the crystal aging effect (see Section 8.4.1).
- The registers at addresses 1Ah and 1Bh are for internal use only.
- The registers Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

When one of the RTC registers is written or read, the content of all counters is temporarily frozen. This prevents a faulty writing or reading of the clock and calendar during a carry condition (see Section 8.8.8).

Table 5. Register overview

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
Control registers											
00h	Control_1	EXT_TEST	T	STOP	TSF1	POR_OVRD	12_24	MI	SI	0000 1000	Table 7 on page 10
01h	Control_2	MSF	WDTF	TSF2	AF	T	TSIE	AIE	T	0000 0000	Table 9 on page 11
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE	0000 0000	Table 11 on page 12
Time and date registers											
03h	Seconds	OSF	SECONDS (0 to 59)							1XXX XXXX	Table 22 on page 25
04h	Minutes	-	MINUTES (0 to 59)							- XXX XXXX	Table 25 on page 26
05h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode					- - XX XXXX	Table 27 on page 27
				HOURS (0 to 23) in 24-hour mode						- - XX XXXX	
06h	Days	-	-	DAYS (1 to 31)						- - XX XXXX	Table 29 on page 27
07h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			- - - - - XXX	Table 31 on page 28
08h	Months	-	-	-	MONTHS (1 to 12)					- - - X XXXX	Table 34 on page 29
09h	Years	YEARS (0 to 99)								XXXX XXXX	Table 37 on page 30
Alarm registers											
0Ah	Second_alarm	AE_S	SECOND_ALARM (0 to 59)							1XXX XXXX	Table 39 on page 33
0Bh	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)							1XXX XXXX	Table 41 on page 33
0Ch	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode					1 - XX XXXX	Table 43 on page 34
				HOUR_ALARM (0 to 23) in 24-hour mode						1 - XX XXXX	
0Dh	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)						1 - XX XXXX	Table 45 on page 34
0Eh	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)			1 - - - - XXX	Table 47 on page 35
CLKOUT control register											
0Fh	CLKOUT_ctl	TCR[1:0]		OTPR	-	-	COF[2:0]			00X - - 000	Table 13 on page 12
Watchdog registers											
10h	Watchdg_tim_ctl	WD_CD	T	TI_TP	-	-	-	TF[1:0]		000 - - - 11	Table 49 on page 36
11h	Watchdg_tim_val	WATCHDG_TIM_VAL[7:0]								XXXX XXXX	Table 51 on page 36
Timestamp registers											
12h	Timestp_ctl	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]					00 - X XXXX	Table 58 on page 41

Table 5. Register overview *…continued*

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
13h	Sec_timestp	-	SECOND_TIMESTP (0 to 59)							- XXX XXXX	Table 60 on page 41
14h	Min_timestp	-	MINUTE_TIMESTP (0 to 59)							- XXX XXXX	Table 62 on page 42
15h	Hour_timestp	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					- - XX XXXX	Table 64 on page 42
				HOUR_TIMESTP (0 to 23) in 24-hour mode						- - XX XXXX	
16h	Day_timestp	-	-	DAY_TIMESTP (1 to 31)						- - XX XXXX	Table 66 on page 43
17h	Mon_timestp	-	-	-	MONTH_TIMESTP (1 to 12)					- - - X XXXX	Table 68 on page 43
18h	Year_timestp	YEAR_TIMESTP (0 to 99)								XXXX XXXX	Table 70 on page 43
Aging offset register											
19h	Aging_offset	-	-	-	-	AO[3:0]				- - - - 1000	Table 17 on page 14
Internal registers											
1Ah	Internal_reg	-	-	-	-	-	-	-	-	- - - - - - - -	-
1Bh	Internal_reg	-	-	-	-	-	-	-	-	- - - - - - - -	-

8.2 Control registers

The first 3 registers of the PCF2129, with the addresses 00h, 01h, and 02h, are used as control registers.

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit allocation

Bits labeled as T must always be written with logic 0.

Bit	7	6	5	4	3	2	1	0
Symbol	EXT_TEST	T	STOP	TSF1	POR_OVRD	12_24	MI	SI
Reset value	0	0	0	0	1	0	0	0

Table 7. Control_1 - control and status register 1 (address 00h) bit description

Bits labeled as T must always be written with logic 0.

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0	normal mode	Section 8.13
		1	external clock test mode	
6	T	0	unused	-
5	STOP	0	RTC source clock runs	Section 8.14
		1	RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available	
4	TSF1	0	no timestamp interrupt generated	Section 8.11.1
		1	flag set when $\overline{TS}$ input is driven to an intermediate level between power supply and ground; flag must be cleared to clear interrupt	
3	POR_OVRD	0	Power-On Reset Override (PORO) facility disabled; **set logic 0 for normal operation**	Section 8.7.2
		1	Power-On Reset Override (PORO) sequence reception enabled	
2	12_24	0	24-hour mode selected	Table 27, Table 43, Table 64
		1	12-hour mode selected	
1	MI	0	minute interrupt disabled	Section 8.12.1
		1	minute interrupt enabled	
0	SI	0	second interrupt disabled	
		1	second interrupt enabled	

8.2.2 Register Control_2

Table 8. Control_2 - control and status register 2 (address 01h) bit allocation

Bits labeled as T must always be written with logic 0.

Bit	7	6	5	4	3	2	1	0
Symbol	MSF	WDTF	TSF2	AF	T	TSIE	AIE	T
Reset value	0	0	0	0	0	0	0	0

Table 9. Control_2 - control and status register 2 (address 01h) bit description

Bits labeled as T must always be written with logic 0.

Bit	Symbol	Value	Description	Reference
7	MSF	0	no minute or second interrupt generated	Section 8.12
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
6	WDTF	0	no watchdog timer interrupt or reset generated	Section 8.12.3
		1	flag set when watchdog timer interrupt or reset generated; flag cannot be cleared by command (read-only)	
5	TSF2	0	no timestamp interrupt generated	Section 8.11.1
		1	flag set when $\overline{TS}$ input is driven to ground; flag must be cleared to clear interrupt	
4	AF	0	no alarm interrupt generated	Section 8.9.6
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
3	T	0	unused	-
2	TSIE	0	no interrupt generated from timestamp flag	Section 8.12.5
		1	interrupt generated when timestamp flag set	
1	AIE	0	no interrupt generated from the alarm flag	Section 8.12.4
		1	interrupt generated when alarm flag set	
0	T	0	unused	-

8.2.3 Register Control_3

Table 10. Control_3 - control and status register 3 (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
Reset value	0	0	0	0	0	0	0	0

Table 11. Control_3 - control and status register 3 (address 02h) bit description

Bit	Symbol	Value	Description	Reference
7 to 5	PWRMNG[2:0]	see Table 19	control of the battery switch-over, battery low detection, and extra power fail detection functions	Section 8.5
4	BTSE	0	no timestamp when battery switch-over occurs	Section 8.11.4
		1	time-stamped when battery switch-over occurs	
3	BF	0	no battery switch-over interrupt generated	Section 8.5.1 and Section 8.11.4
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt	
2	BLF	0	battery status ok; no battery low interrupt generated	Section 8.5.2
		1	battery status low; flag cannot be cleared by command	
1	BIE	0	no interrupt generated from the battery flag (BF)	Section 8.12.6
		1	interrupt generated when BF is set	
0	BLIE	0	no interrupt generated from battery low flag (BLF)	Section 8.12.7
		1	interrupt generated when BLF is set	

8.3 Register CLKOUT_ctl

Table 12. CLKOUT_ctl - CLKOUT control register (address 0Fh) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	TCR[1:0]		OTPR	-	-	COF[2:0]		
Reset value	0	0	X	-	-	0	0	0

Table 13. CLKOUT_ctl - CLKOUT control register (address 0Fh) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7 to 6	TCR[1:0]	see Table 14	temperature measurement period
5	OTPR	0	no OTP refresh
		1	OTP refresh performed
4 to 3	-	-	unused
2 to 0	COF[2:0]	see Table 15	CLKOUT frequency selection

8.3.1 Temperature compensated crystal oscillator

The frequency of tuning fork quartz crystal oscillators is temperature-dependent. In the PCF2129, the frequency deviation caused by temperature variation is corrected by adjusting the load capacitance of the crystal oscillator.

The load capacitance is changed by switching between two load capacitance values using a modulation signal with a programmable duty cycle. In order to compensate the spread of the quartz parameters every chip is factory calibrated.

The frequency accuracy can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT. However, the selection of f_{CLKOUT} = 32.768 kHz (default value) leads to inaccurate measurements. Accurate frequency measurement occurs when f_{CLKOUT} = 16.384 kHz or lower is selected (see Table 15).

8.3.1.1 Temperature measurement

The PCF2129 has a temperature sensor circuit used to perform the temperature compensation of the frequency. The temperature is measured immediately after power-on and then periodically with a period set by the temperature conversion rate TCR[1:0] in the register CLKOUT_ctl.

Table 14. Temperature measurement period

TCR[1:0]	Temperature measurement period
00 [1]	4 min
01	2 min
10	1 min
11	30 seconds

[1] Default value.

8.3.2 OTP refresh

Each IC is calibrated during production and testing of the device. The calibration parameters are stored on EPROM cells called One Time Programmable (OTP) cells. It is recommended to process an OTP refresh once after the power is up and the oscillator is operating stable. The OTP refresh takes less than 100 ms to complete.

To perform an OTP refresh, bit OTPR has to be cleared (set to logic 0) and then set to logic 1 again.

8.3.3 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] control bits in register CLKOUT_ctl. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as system clock, microcontroller clock, charge pump input, or for calibrating the oscillator.

CLKOUT is an open-drain output and enabled at power-on. When disabled, the output is high-impedance.

Table 15. CLKOUT frequency selection

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]
000 [2][3]	32768	60 : 40 to 40 : 60
001	16384	50 : 50
010	8192	50 : 50
011	4096	50 : 50
100	2048	50 : 50
101	1024	50 : 50
110	1	50 : 50
111	CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] The specified accuracy of the RTC can be only achieved with CLKOUT frequencies not equal to 32.768 kHz or if CLKOUT is disabled.

The duty cycle of the selected clock is not controlled, however, due to the nature of the clock generation all but the 32.768 kHz frequencies are 50 : 50.

8.4 Register Aging_offset

Table 16. Aging_offset - crystal aging offset register (address 19h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	AO[3:0]			
Reset value	-	-	-	-	1	0	0	0

Table 17. Aging_offset - crystal aging offset register (address 19h) bit description

Bit positions labeled as - are not implemented and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	-	-	unused
3 to 0	AO[3:0]	see Table 18	aging offset value

8.4.1 Crystal aging correction

The PCF2129 has an offset register Aging_offset to correct the crystal aging effects[2].

The accuracy of the frequency of a quartz crystal depends on its aging. The aging offset adds an adjustment, positive or negative, in the temperature compensation circuit which allows correcting the aging effect.

At 25 °C, the aging offset bits allow a frequency correction of typically 1 ppm per AO[3:0] value, from −7 ppm to +8 ppm.

2. For further information, refer to the application note Ref. 3 “AN11186”.

Table 18. Frequency correction at 25 °C, typical

AO[3:0]		ppm
Decimal	**Binary**	
0	0000	+8
1	0001	+7
2	0010	+6
3	0011	+5
4	0100	+4
5	0101	+3
6	0110	+2
7	0111	+1
8	1000 [1]	0
9	1001	−1
10	1010	−2
11	1011	−3
12	1100	−4
13	1101	−5
14	1110	−6
15	1111	−7

[1] Default value.

8.5 Power management functions

The PCF2129 has two power supplies:

V_{DD} — the main power supply

V_{BAT} — the battery backup supply

Internally, the PCF2129 is operating with the internal operating voltage $V_{oper(int)}$ which is also available as V_{BBS} on the battery backed output voltage pin, BBS. Depending on the condition of the main power supply and the selected power management function, $V_{oper(int)}$ is either on the potential of V_{DD} or V_{BAT} (see Section 8.5.3).

Two power management functions are implemented:

Battery switch-over function — monitoring the main power supply V_{DD} and switching to V_{BAT} in case a power fail condition is detected (see Section 8.5.1).

Battery low detection function — monitoring the status of the battery, V_{BAT} (see Section 8.5.2).

The power management functions are controlled by the control bits PWRMNG[2:0] (see Table 19) in register Control_3 (see Table 11):

Table 19. Power management control bit description

PWRMNG[2:0]	Function
000 [1]	battery switch-over function is enabled in standard mode; battery low detection function is enabled
001	battery switch-over function is enabled in standard mode; battery low detection function is disabled
010	battery switch-over function is enabled in standard mode; battery low detection function is disabled
011	battery switch-over function is enabled in direct switching mode; battery low detection function is enabled
100	battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
101	battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
111 [2]	battery switch-over function is disabled, only one power supply (V_{DD}); battery low detection function is disabled

[1] Default value.

[2] When the battery switch-over function is disabled, the PCF2129 works only with the power supply V_{DD}. V_{BAT} must be put to ground and the battery low detection function is disabled.

8.5.1 Battery switch-over function

The PCF2129 has a backup battery switch-over circuit which monitors the main power supply V_{DD}. When a power failure condition is detected, it automatically switches to the backup battery.

One of two operation modes can be selected:

Standard mode — the power failure condition happens when:
$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$
$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. The battery switch-over in standard mode works only for $V_{DD} > 2.5$ V

Direct switching mode — the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BF (register Control_3) is set logic 1.
2. An interrupt is generated if the control bit BIE (register Control_3) is enabled (see Section 8.12.6).
3. If the control bit BTSE (register Control_3) is logic 1, the timestamp registers store the time and date when the battery switch occurred (see Section 8.11.4).
4. The battery switch flag BF is cleared by command; it must be cleared to clear the interrupt.

The interface is disabled in battery backup operation:

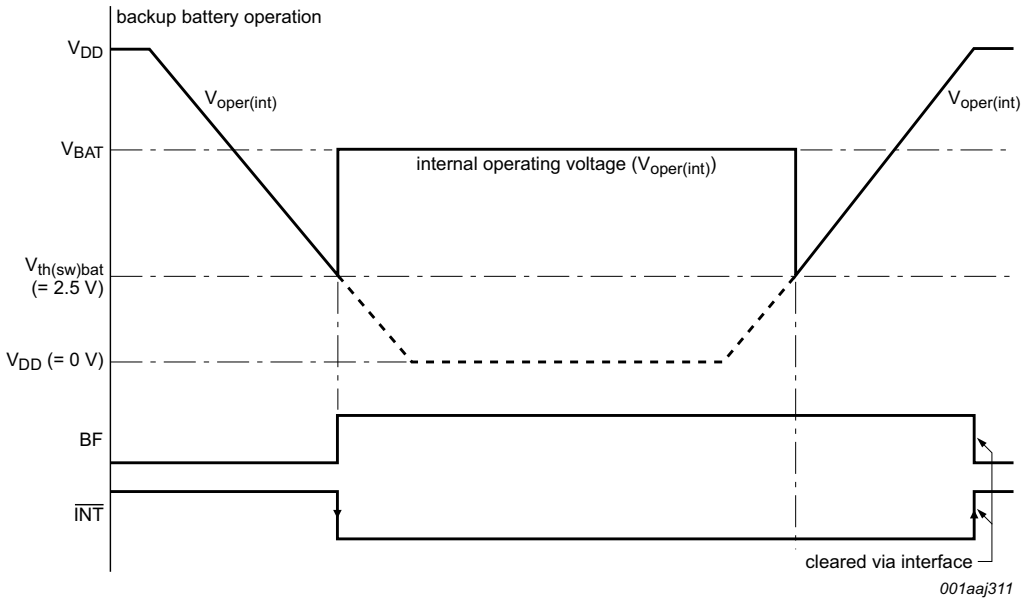
- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

For further information about I^2C-bus communication and battery backup operation, see Section 9.3 on page 56.

8.5.1.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{DD} potential.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{BAT} potential.



$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. In standard mode, the battery switch-over works only for $V_{DD} > 2.5$ V.

V_{DD} may be lower than V_{BAT} (for example V_{DD} = 3 V, V_{BAT} = 4.1 V).

Fig 6. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled)

8.5.1.2 Direct switching mode

If $V_{DD} > V_{BAT}$: $V_{oper(int)}$ is at V_{DD} potential.

If $V_{DD} < V_{BAT}$: $V_{oper(int)}$ is at V_{BAT} potential.

The direct switching mode is useful in systems where V_{DD} is always higher than V_{BAT}. This mode is not recommended if the V_{DD} and V_{BAT} values are similar (for example, V_{DD} = 3.3 V, $V_{BAT} \geq 3.0$ V). In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

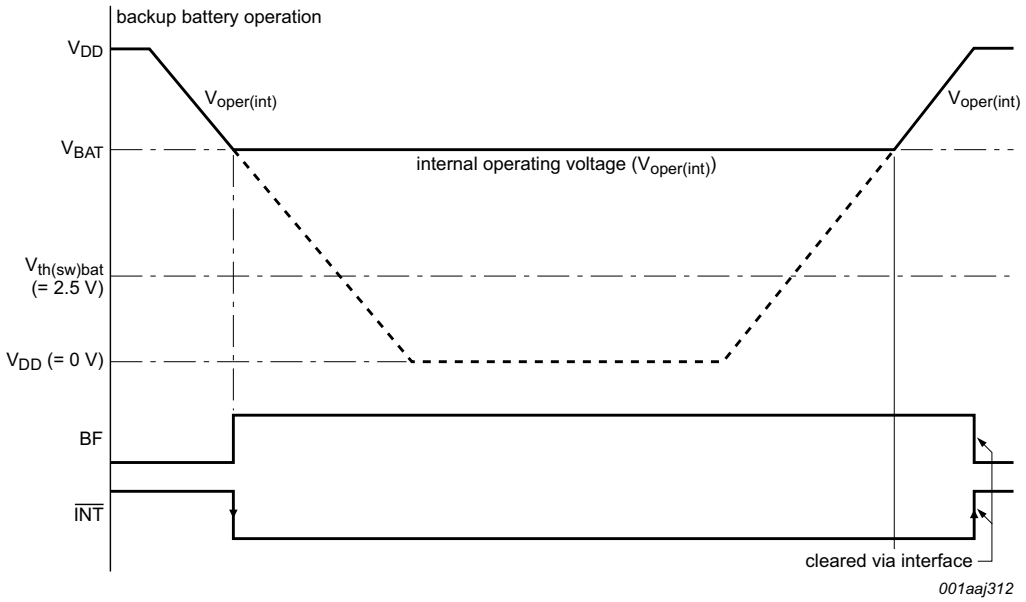


Fig 7. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled)

8.5.1.3 Battery switch-over disabled: only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to ground
- $V_{oper(int)}$ is at V_{DD} potential
- The battery flag (BF) is always logic 0

8.5.1.4 Battery switch-over architecture

The architecture of the battery switch-over circuit is shown in Figure 8.

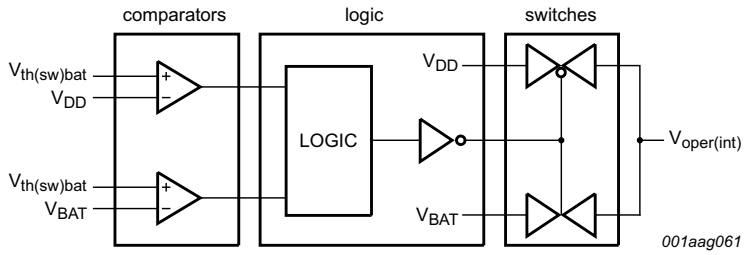


Fig 8. Battery switch-over circuit, simplified block diagram

$V_{oper(int)}$ is at V_{DD} or V_{BAT} potential.

Remark: It has to be assured that there are decoupling capacitors on the pins V_{DD}, V_{BAT}, and BBS.

8.5.2 Battery low detection function

The PCF2129 has a battery low detection circuit which monitors the status of the battery V_{BAT}.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typically 2.5 V), the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery cannot prevent that the supply voltage drops below V_{low} (typical 1.2 V) and with that the data integrity gets lost. (For further information about V_{low} see Section 8.6.)

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 9):

1. The battery low flag BLF is set logic 1.
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled (see Section 8.12.7).
3. The flag BLF remains logic 1 until the battery is replaced. BLF cannot be cleared by command. It is automatically cleared by the battery low detection circuit when the battery is replaced or when the voltage rises again above the threshold value. This could happen if a super capacitor is used as a backup source and the main power is applied again.

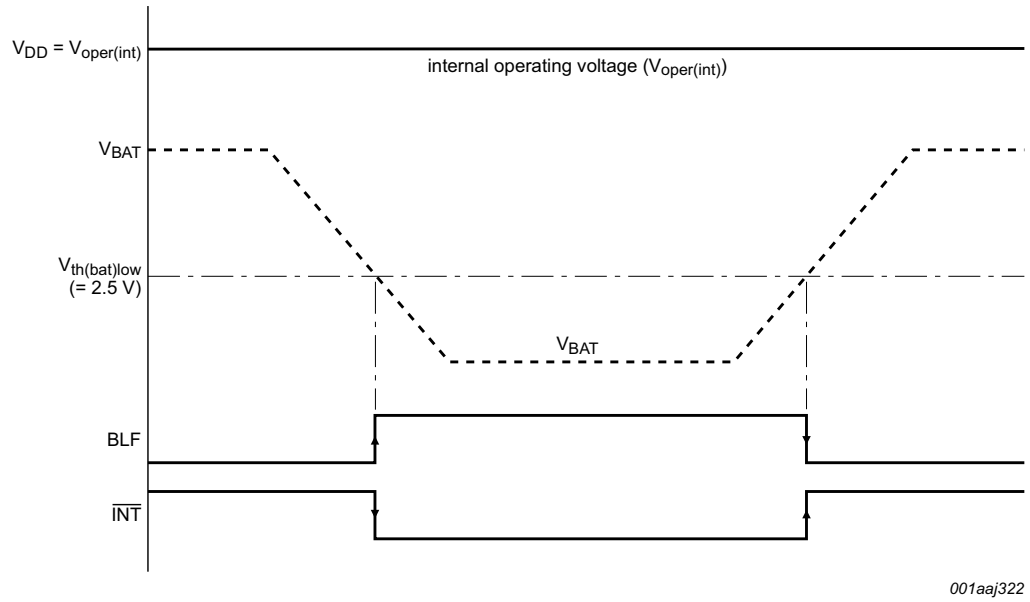


Fig 9. Battery low detection behavior with bit BLIE set logic 1 (enabled)

8.5.3 Battery backup supply

The V_{BBS} voltage on the output pin BBS is at the same potential as the internal operating voltage $V_{oper(int)}$, depending on the selected battery switch-over function mode:

Table 20. Output pin BBS

Battery switch-over function mode	Conditions	Potential of $V_{oper(int)}$ and V_{BBS}
standard	$V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$	V_{DD}
	$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$	V_{BAT}
direct switching	$V_{DD} > V_{BAT}$	V_{DD}
	$V_{DD} < V_{BAT}$	V_{BAT}
disabled	only V_{DD} available, V_{BAT} must be put to ground	V_{DD}

The output pin BBS can be used as a supply for external devices with battery backup needs, such as SRAM (see Ref. 3 “AN11186”). For this case, Figure 10 shows the typical driving capability when V_{BBS} is driven from V_{DD}.

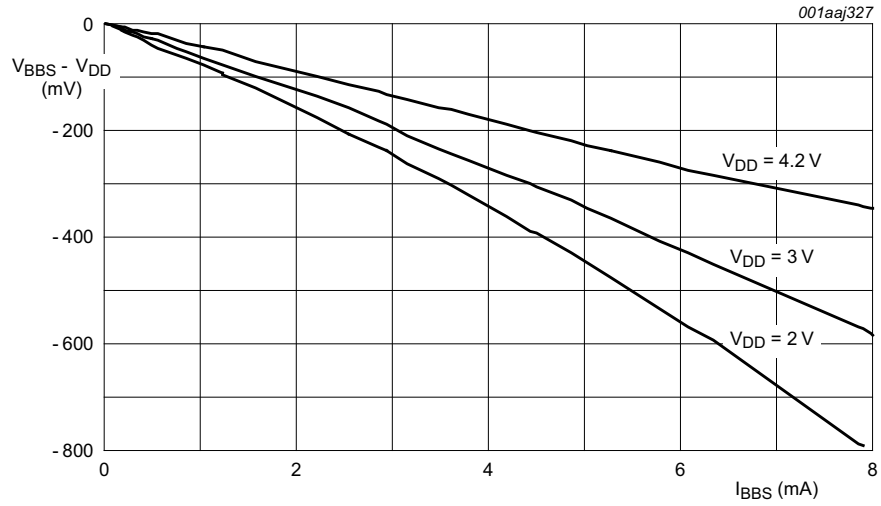
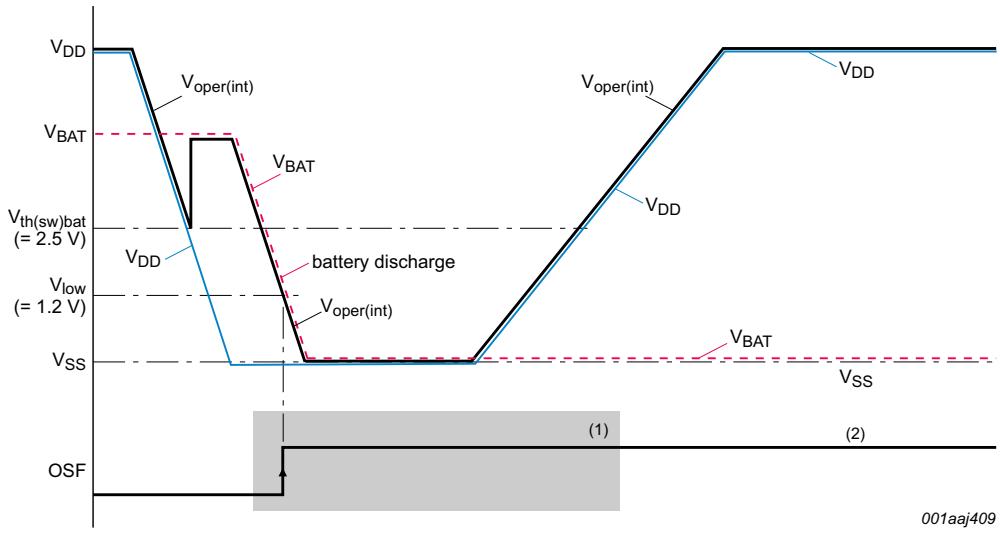


Fig 10. Typical driving capability of V_{BBS}: (V_{BBS} − V_{DD}) with respect to the output load current I_{BBS}

8.6 Oscillator stop detection function

The PCF2129 has an on-chip oscillator detection circuit which monitors the status of the oscillation: whenever the oscillation stops, a reset occurs and the oscillator stop flag OSF (in register Seconds) is set logic 1.

- **Power-on:**
  a. The oscillator is not running, the chip is in reset (OSF is logic 1).
  b. When the oscillator starts running and is stable after power-on, the chip exits from reset.
  c. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.
- **Power supply failure:**
  a. When the power supply of the chip drops below a certain value (V_{low}), typically 1.2 V, the oscillator stops running and a reset occurs.
  b. When the power supply returns to normal operation, the oscillator starts running again, the chip exits from reset.
  c. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.



(1) Theoretical state of the signals since there is no power.

(2) The oscillator stop flag (OSF), set logic 1, indicates that the oscillation has stopped and a reset has occurred since the flag was last cleared (OSF set logic 0). In this case, the integrity of the clock information is not guaranteed. The OSF flag is cleared by command.

Fig 11. Power failure event due to battery discharge: reset occurs

8.7 Reset function

The PCF2129 has a Power-On Reset (POR) and a Power-On Reset Override (PORO) function implemented.

8.7.1 Power-On Reset (POR)

The POR is active whenever the oscillator is stopped. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance (see Figure 12). This time may be in the range of 200 ms to 2 s depending on temperature and supply voltage. Whenever an internal reset occurs, the oscillator stop flag is set (OSF set logic 1).

The OTP refresh (see Section 8.3.2 on page 13) should ideally be executed as the first instruction after start-up and also after a reset due to an oscillator stop.

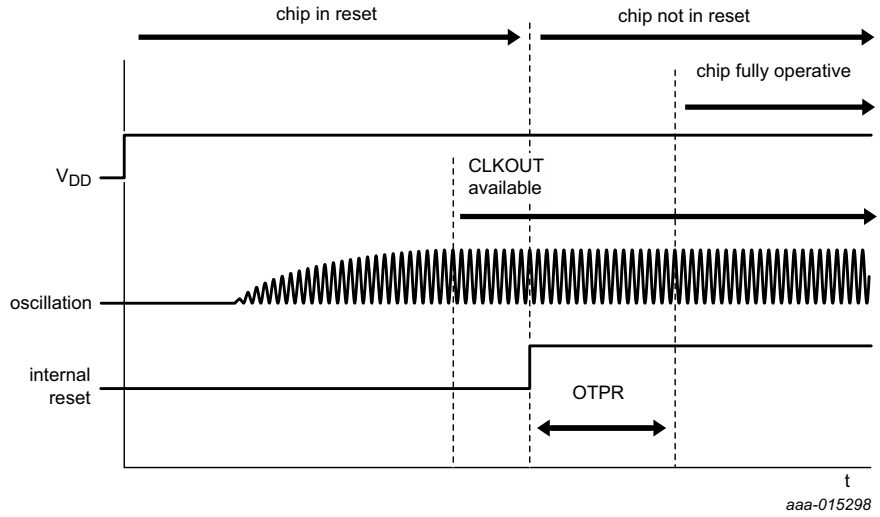


Fig 12. Dependency between POR and oscillator

After POR, the following mode is entered:

- 32.768 kHz CLKOUT active
- Power-On Reset Override (PORO) available to be set
- 24-hour mode is selected
- Battery switch-over is enabled
- Battery low detection is enabled

The register values after power-on are shown in Table 5 on page 8.

8.7.2 Power-On Reset Override (PORO)

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and therefore speed up the on-board test of the device.

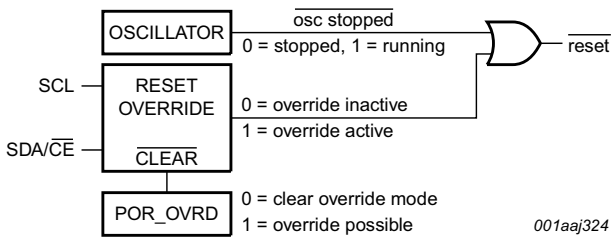


Fig 13. Power-On Reset (POR) system

The setting of the PORO mode requires that POR_OVRD in register Control_1 is set logic 1 and that the signals at the interface pins SDA/$\overline{CE}$ and SCL are toggled as illustrated in Figure 14. All timings shown are required minimum.

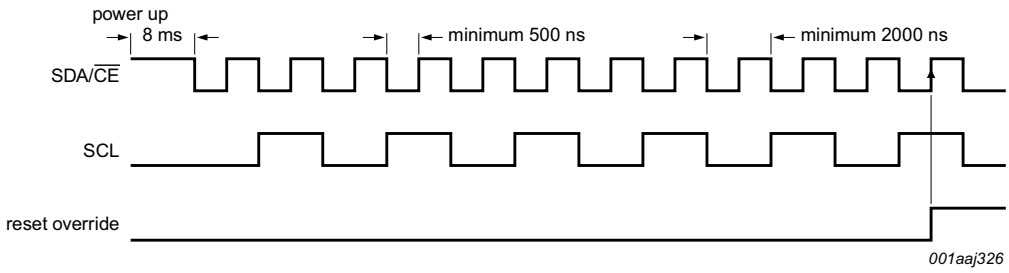


Fig 14. Power-On Reset Override (PORO) sequence, valid for both I²C-bus and SPI-bus

Once the override mode is entered, the device is immediately released from the reset state and the set-up operation can commence.

The PORO mode is cleared by writing logic 0 to POR_OVRD. POR_OVRD must be logic 1 before a re-entry into the override mode is possible. Setting POR_OVRD logic 0 during normal operation has no effect except to prevent accidental entry into the PORO mode.

8.8 Time and date function

Most of these registers are coded in the Binary Coded Decimal (BCD) format.

8.8.1 Register Seconds

Table 21. Seconds - seconds and clock integrity register (address 03h) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	OSF	SECONDS (0 to 59)						
Reset value	1	X	X	X	X	X	X	X

Table 22. Seconds - seconds and clock integrity register (address 03h) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	OSF	0	-	clock integrity is guaranteed
		1	-	clock integrity is not guaranteed: oscillator has stopped and chip reset has occurred since flag was last cleared
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	