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PCF85132

LCD driver for low multiplex rates

Rev. 4 — 24 April 2015 Product data sheet

1. General description

The PCF85132 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 160 segments. It can easily be cascaded for larger LCD applications. The PCF85132 is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

For a selection of NXP LCD segment drivers, see Table 29 on page 56.

2. Features and benefits

- Single-chip LCD controller and driver for up to 640 elements
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- 160 segment drives:
  - Up to 80 7-segment numeric characters
  - Up to 40 14-segment alphanumeric characters
  - Any graphics of up to 640 elements
- May be cascaded for large LCD applications (up to 5120 elements possible)
- 160 × 4-bit RAM for display data storage
- Software programmable frame frequency in steps of 5 Hz in the range of 60 Hz to 90 Hz; factory calibrated
- Wide LCD supply range: from 1.8 V for low threshold LCDs and up to 8.0 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Internal LCD bias generation with voltage-follower buffers
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Wide power supply range: from 1.8 V to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption, typical: I_{DD} = 4 μA, $I_{DD(LCD)}$ = 30 μA
- 400 kHz I^2C-bus interface
- Auto-incremental display data loading across device subaddress boundaries
- Versatile blinking modes
- Compatible with Chip-On-Glass (COG) technology
- No external components required
- Two sets of backplane outputs for optimal COG configurations of the application

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 18 on page 58.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF85132U	bare die	197 bumps; 6.5 × 1.16 × 0.40 mm	PCF85132U

3.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF85132U/2DA/1	PCF85132U/2DA/1,02	935293465026	chips with bumps in tray	1

4. Marking

Table 3. Marking codes

Product type number	Marking code
PCF85132U/2DA/1	PC85132/232-1

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5. Block diagram

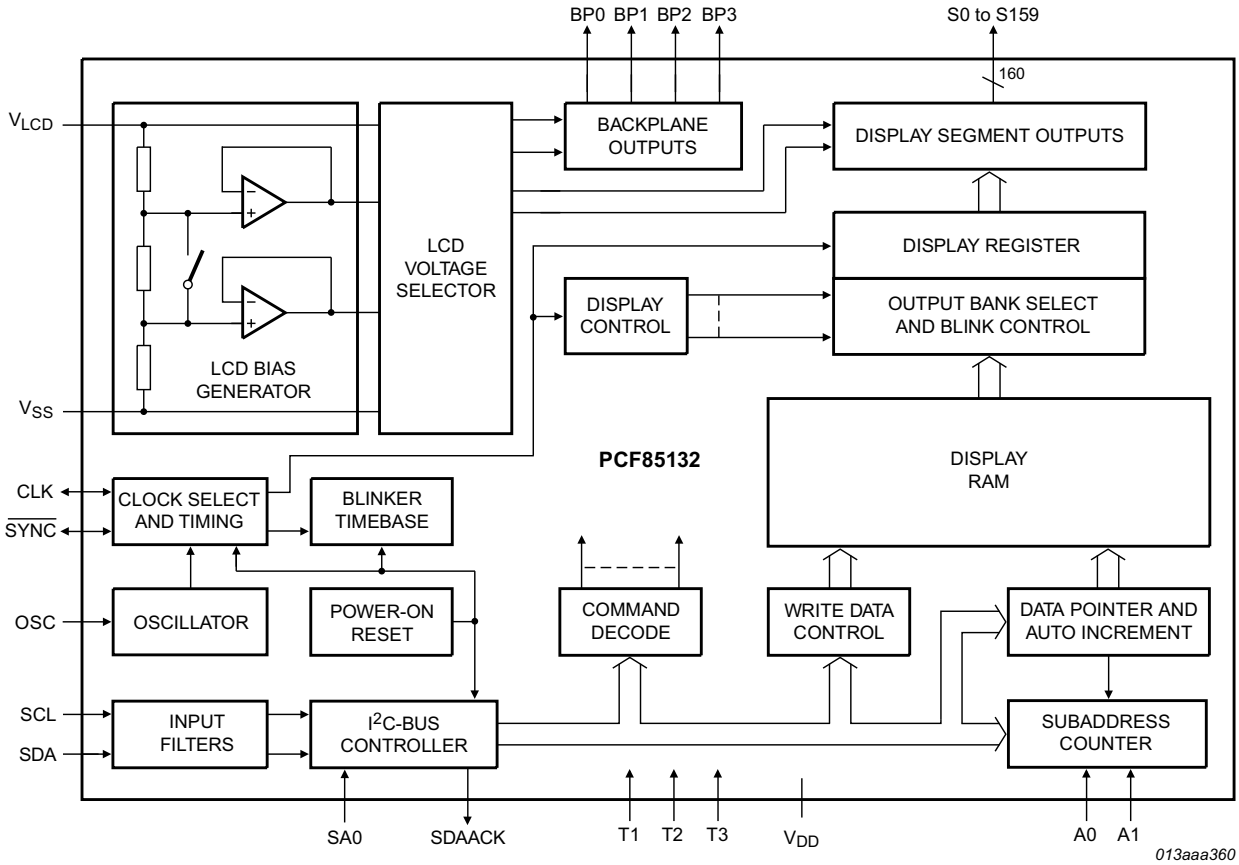

Fig 1. Block diagram of PCF85132

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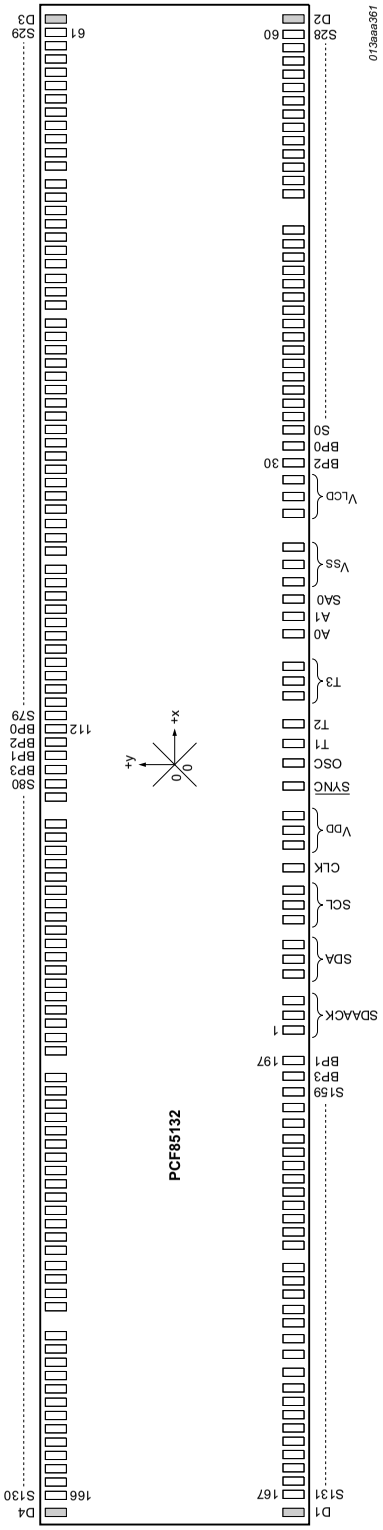
6. Pinning information

6.1 Pinning



Viewed from active side. For mechanical details, see Figure 37 on page 49.

Fig 2. Pinning diagram of PCF85132

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6.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
SDAACK[1]	1 to 3	I^2C-bus acknowledge output
SDA[1]	4 to 6	I^2C-bus serial data input
SCL	7 to 9	I^2C-bus serial clock input
CLK	10	clock input and output
V_{DD}	11 to 13	supply voltage
$\overline{SYNC}$	14	cascade synchronization input and output
OSC	15	selection of internal or external clock
T1, T2, and T3	16, 17, and 18 to 20	dedicated testing pins; to be tied to V_{SS} in application mode
A0 and A1	21, 22	subaddress inputs
SA0	23	I^2C-bus slave address input
V_{SS}[2]	24 to 26	ground supply voltage
V_{LCD}	27 to 29	LCD supply voltage
BP2 and BP0	30, 31	LCD backplane outputs
S0 to S79	32 to 111	LCD segment outputs
BP0, BP2, BP1, and BP3	112 to 115	LCD backplane outputs
S80 to S159	116 to 195	LCD segment outputs
BP3 and BP1	196, 197	LCD backplane outputs

[1] For most applications SDA and SDAACK are shorted together (see Section 14.3 on page 44).

[2] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

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7. Functional description

The PCF85132 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 160 segments.

7.1 Commands of PCF85132

The commands available to the PCF85132 are defined in Table 5.

Table 5. Definition of PCF85132 commands

Command	Operation code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	1	1	0	0	E	B	M[1:0]		Table 6
load-data-pointer-MSB	0	0	0	0	P[7:4]				Table 7
load-data-pointer-LSB	0	1	0	0	P[3:0]				Table 8
device-select	1	1	1	0	0	0	A[1:0]		Table 9
bank-select	1	1	1	1	1	0	I	O	Table 10
blink-select	1	1	1	1	0	AB	BF[1:0]		Table 11
frequency-ctrl	1	1	1	0	1	F[2:0]			Table 12

7.1.1 Command: mode-set

The mode-set command allows configuring the multiplex mode, the bias levels and enabling or disabling the display.

Table 6. Mode-set - command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**[1]
		0[2]	disabled (blank)[3]
		1	enabled
2	B		**LCD bias configuration**[4]
		0[2]	1/3 bias
		1	1/2 bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00[2]	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control. The enable bit determines also whether the internal clock signal is available at the CLK pin (see Section 7.1.6.2 on page 9).

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[4] Not applicable for static drive mode.

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7.1.2 Command: load-data-pointer

The load-data-pointer command defines the display RAM address where the following display data will be sent to.

Table 7. Load-data-pointer-MSB - command bit description

See Section 7.5.1 on page 24.

Bit	Symbol	Value	Description
7 to 4	-	0000	fixed value
3 to 0	P[7:4]	0000[1] to 1001	**defines the first 4 (most significant) bits of the data-pointer** the data-pointer indicates one of the 160 display RAM addresses

[1] Default value.

Table 8. Load-data-pointer-LSB - command bit description

See Section 7.5.1 on page 24.

Bit	Symbol	Value	Description
7 to 4	-	0100	fixed value
3 to 0	P[3:0]	0000[1] to 1111	**defines the last 4 (least significant) bits of the data-pointer** the data-pointer indicates one of the 160 display RAM addresses

[1] Default value.

7.1.3 Command: device-select

The device-select command allows defining the subaddress counter value.

Table 9. Device-select - command bit description

See Section 7.5.2 on page 24.

Bit	Symbol	Value	Description
7 to 2	-	111000	fixed value
1 to 0	A[1:0]	00[1] to 11	**defines one of four hardware subaddresses** (see Table 23 on page 44)

[1] Default value.

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7.1.4 Command: bank-select

The bank-select command controls where data is written to RAM and where it is displayed from.

Table 10. Bank-select - command bit description

See Section 7.5.4 on page 26.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7 to 2	-	111110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

[2] Default value.

7.1.5 Command: blink-select

The blink-select command allows configuring the blink mode and the blink frequency.

Table 11. Blink-select - command bit description

See Section 7.1.6.6 on page 10.

Bit	Symbol	Value	Description
7 to 3	-	11110	fixed value
2	AB		**blink mode selection**
		0[1]	normal blinking[2]
		1	alternate RAM bank blinking[3]
1 to 0	BF[1:0]		**blink frequency selection**
		00[1]	off
		01	1
		10	2
		11	3

[1] Default value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.1.6 Clock frequency and timing

The timing of the PCF85132 organizes the internal data flow of the device. The timing includes the transfer of display data from the display RAM to the display segment outputs and therefore the frame frequency.

7.1.6.1 Clock source selection

The PCF85132 can be configured to use either the built-in oscillator or an external clock as clock source:

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Internal clock — To enable the internal oscillator, pin OSC has to be connected to V_{SS}. Pin CLK then becomes an output. For further information on the internal clock, see Section 7.1.6.2.

External clock — To enable the use of an external clock, pin OSC has to be connected to V_{DD}. Pin CLK then becomes an input for the external clock frequency $f_{clk(ext)}$. For further information on the external clock, see Section 7.1.6.3.

Figure 3 illustrates the frequency generation of the PCF85132.

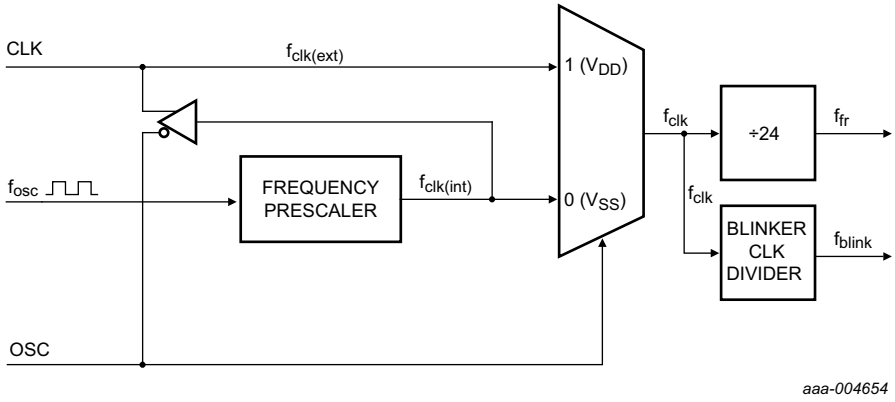

Fig 3. Frequency generation of the PCF85132

Remark: A clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.1.6.2 Internal clock

If the internal oscillator is used, the timing of the PCF85132 is derived from the built-in oscillator by a pre-scaler which can be configured with the frequency-ctrl command (see Table 12).

The internal oscillator is calibrated within an accuracy of ±3.9 % (at V_{DD} = 5.0 V; T_{amb} = 30 °C).

The frequency-ctrl command determines the division factor between the oscillator frequency f_{osc} and the internal clock frequency $f_{clk(int)}$. If the internal oscillator is used, the frame frequency is derived from the internal clock frequency $f_{clk(int)}$ by the fixed division shown in Equation 1 on page 10.

If the display is enabled (see bit E in Table 6), $f_{clk(int)}$ on pin CLK provides the clock signal for cascaded LCD drivers in the system. For further information about cascading, see Section 14.4 on page 44. The value range of f_{osc} is specified in Table 22 on page 38.

7.1.6.3 External clock

If the external clock source is selected, the timing frequency of the PCF85132 is the external clock frequency. In this case, the frequency-ctrl command has no influence on the clock frequency nor the frame frequency. The frame frequency is derived from the external clock frequency $f_{clk(ext)}$ by the fixed division as shown in Equation 1.

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7.1.6.4 Frame frequency

Sourced by the internal oscillator or an external clock, the frame frequency is derived from the clock frequency f_{clk} by Equation 1.

$$f_{fr} = \frac{f_{clk}}{24} \quad (1)$$

7.1.6.5 Command: frequency-ctrl

Table 12. Frequency-ctrl - command bit description

Bit	Symbol	Value	Description		
			Equation	Nominal clock frequency[1]	Nominal frame frequency[1]
7 to 4	-	11101	fixed value		
3 to 0	F[2:0]		**defines the division factor**		
		000	$f_{clk(int)} = \frac{64}{80} \times f_{osc}$	1440 Hz	60 Hz
		001	$f_{clk(int)} = \frac{64}{74} \times f_{osc}$	1557 Hz	65 Hz
		010	$f_{clk(int)} = \frac{64}{68} \times f_{osc}$	1694 Hz	70 Hz
		011[2], 111	$f_{clk(int)} = f_{osc}$	1800 Hz	75 Hz
		100	$f_{clk(int)} = \frac{64}{60} \times f_{osc}$	1920 Hz	80 Hz
		101	$f_{clk(int)} = \frac{64}{56} \times f_{osc}$	2057 Hz	85 Hz
		110	$f_{clk(int)} = \frac{64}{53} \times f_{osc}$	2174 Hz	90 Hz

[1] Calculated with the oscillator frequency of f_{osc} = 1.800 Hz. The frame frequency is derived from the internal clock frequency by Equation 1.

[2] Default value.

7.1.6.6 Blinking

The display blinking capabilities of the PCF85132 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 11). The blink frequencies are derived from the clock frequency (f_{clk}). The ratios between the clock and blink frequencies depend on the blink mode in which the device is operating (see Table 13).

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Table 13. Blink frequencies

Assuming that f_{clk} = 1.800 kHz.

Blink mode	Operating mode ratio	Blink frequency
off	-	blinking off
1	$f_{blink} = \frac{f_{clk}}{768}$	~2.34 Hz
2	$f_{blink} = \frac{f_{clk}}{1536}$	~1.17 Hz
3	$f_{blink} = \frac{f_{clk}}{3072}$	~0.59 Hz

An additional feature is for an arbitrary selection of LCD elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads: With the output bank selector, the displayed RAM banks are exchanged (see Section 7.5.4 on page 26) with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command (see Table 11 on page 8).

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD elements can blink selectively by changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blinking frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 6).

7.2 Power-On Reset (POR)

At power-on, the PCF85132 resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled (bit E = 0, see Table 6 on page 6)
- If internal oscillator is selected (pin OSC connected to V_{SS}), then there is no clock signal on pin CLK

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.3 Possible display configurations

The display configurations possible with the PCF85132 depend on the required number of active backplane outputs. A selection of display configurations is given in Table 14.

All of the display configurations given in Table 14 can be implemented in a typical system as shown in Figure 5.

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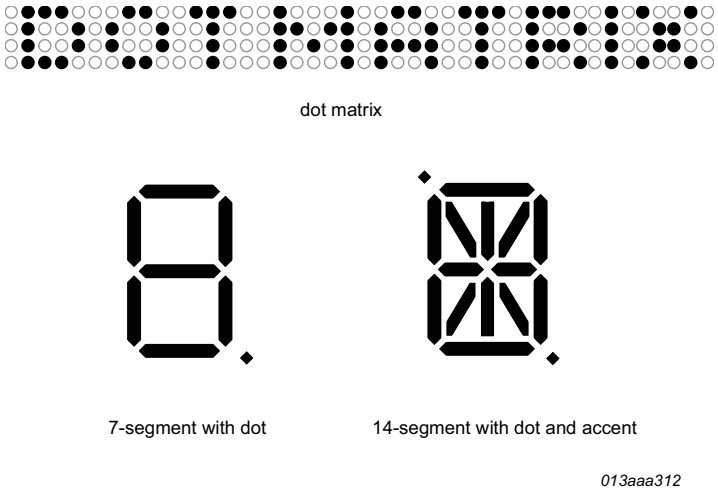

Fig 4. Example of displays suitable for PCF85132

Table 14. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment	**14-segment**	
4	640	80	40	640 dots (4 × 160)
3	480	60	30	480 dots (3 × 160)
2	320	40	20	320 dots (2 × 160)
1	160	20	10	160 dots (1 × 160)

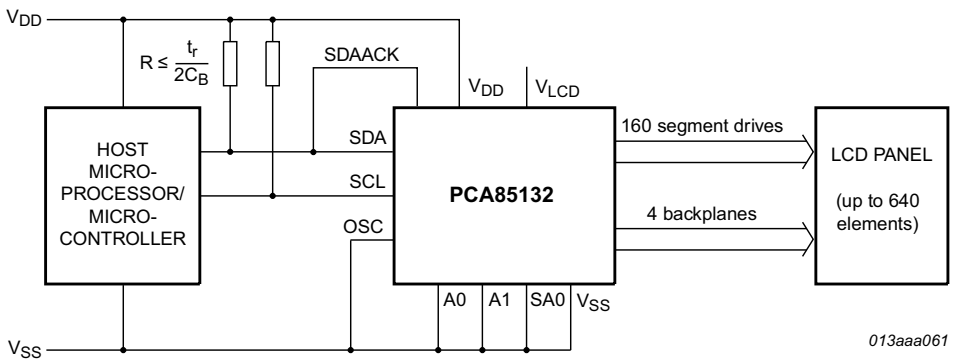

Fig 5. Typical system configuration

The host microcontroller maintains the 2-line I²C-bus communication channel with the PCF85132.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

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7.3.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between pins V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the ½ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

7.3.2 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.3.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 15.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 15. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (2)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

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n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 3:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (3)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 4:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (4)$$

Using Equation 4, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3 V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltages, at which a pixel is switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 6. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (5)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (6)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a (see Equation 2), n (see Equation 4), and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

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It is important to match the module properties to those of the driver in order to achieve optimum performance.

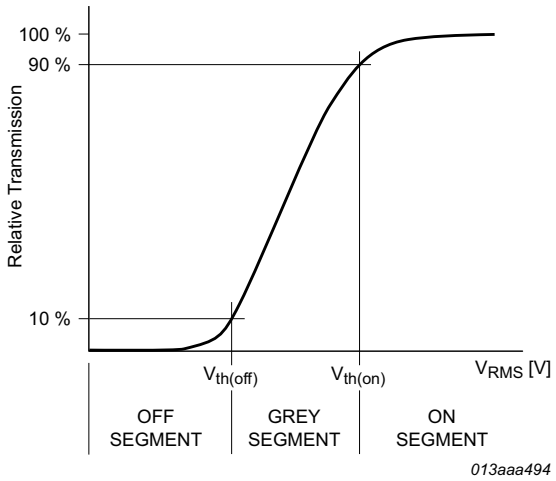

Fig 6. Electro-optical characteristic: relative transmission curve of the liquid

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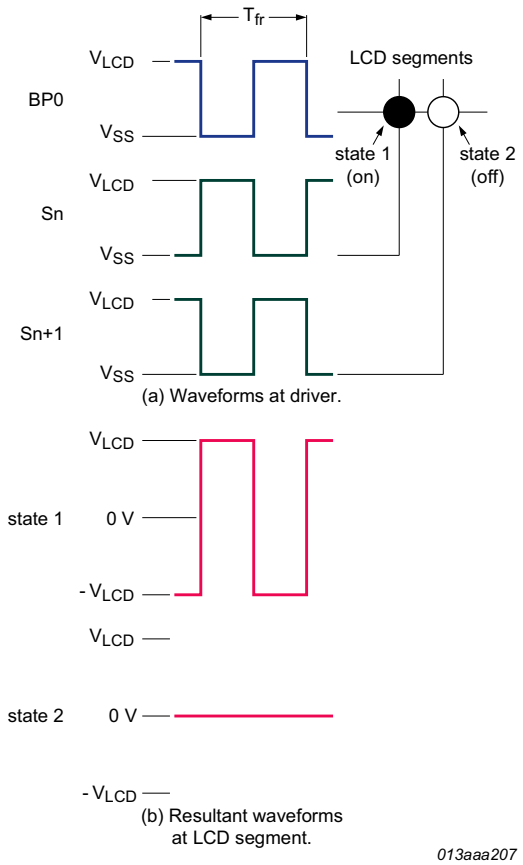
7.3.4 LCD drive mode waveforms

7.3.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 7.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 7. Static drive mode waveforms

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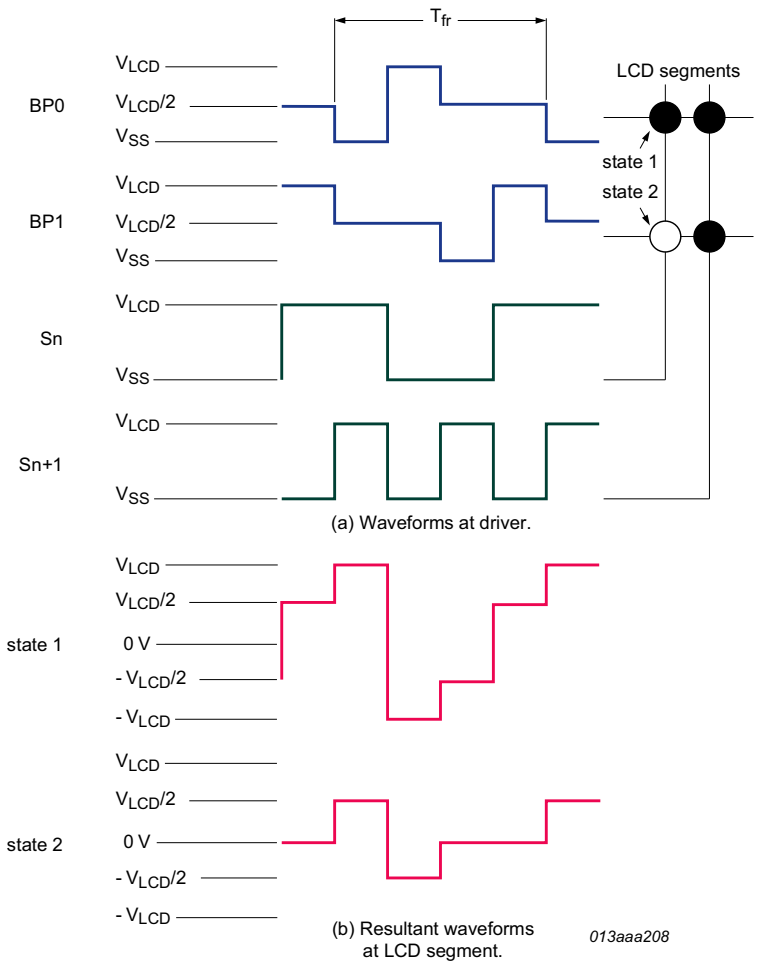
7.3.4.2 1:2 multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF85132 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 8 and Figure 9.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791 V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354 V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with ½ bias

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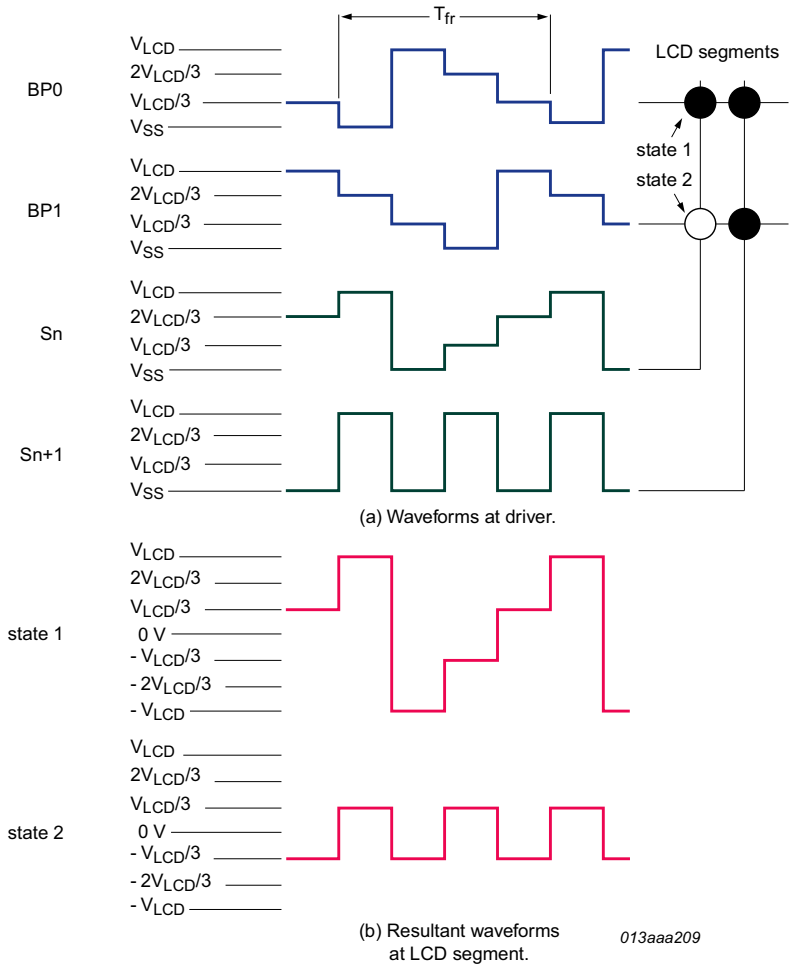

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

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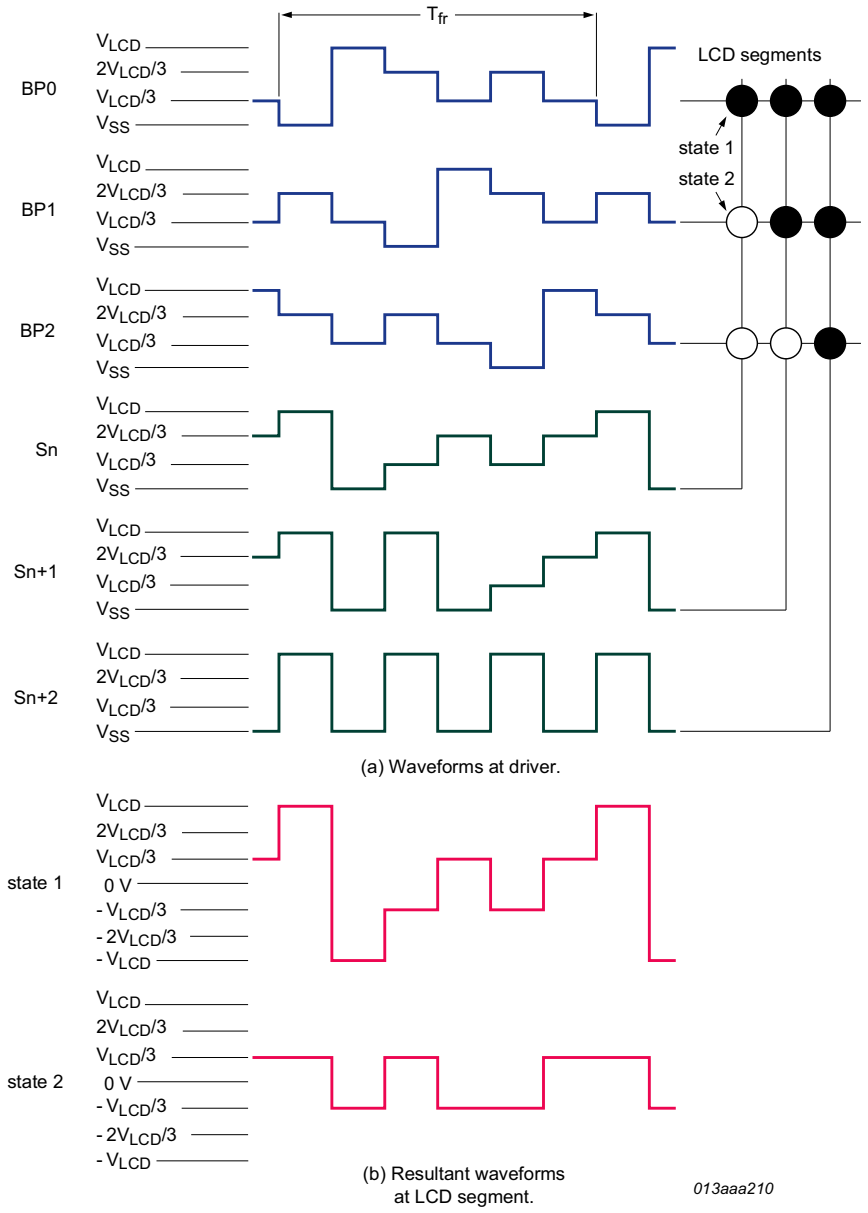
7.3.4.3 1:3 multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in Figure 10.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

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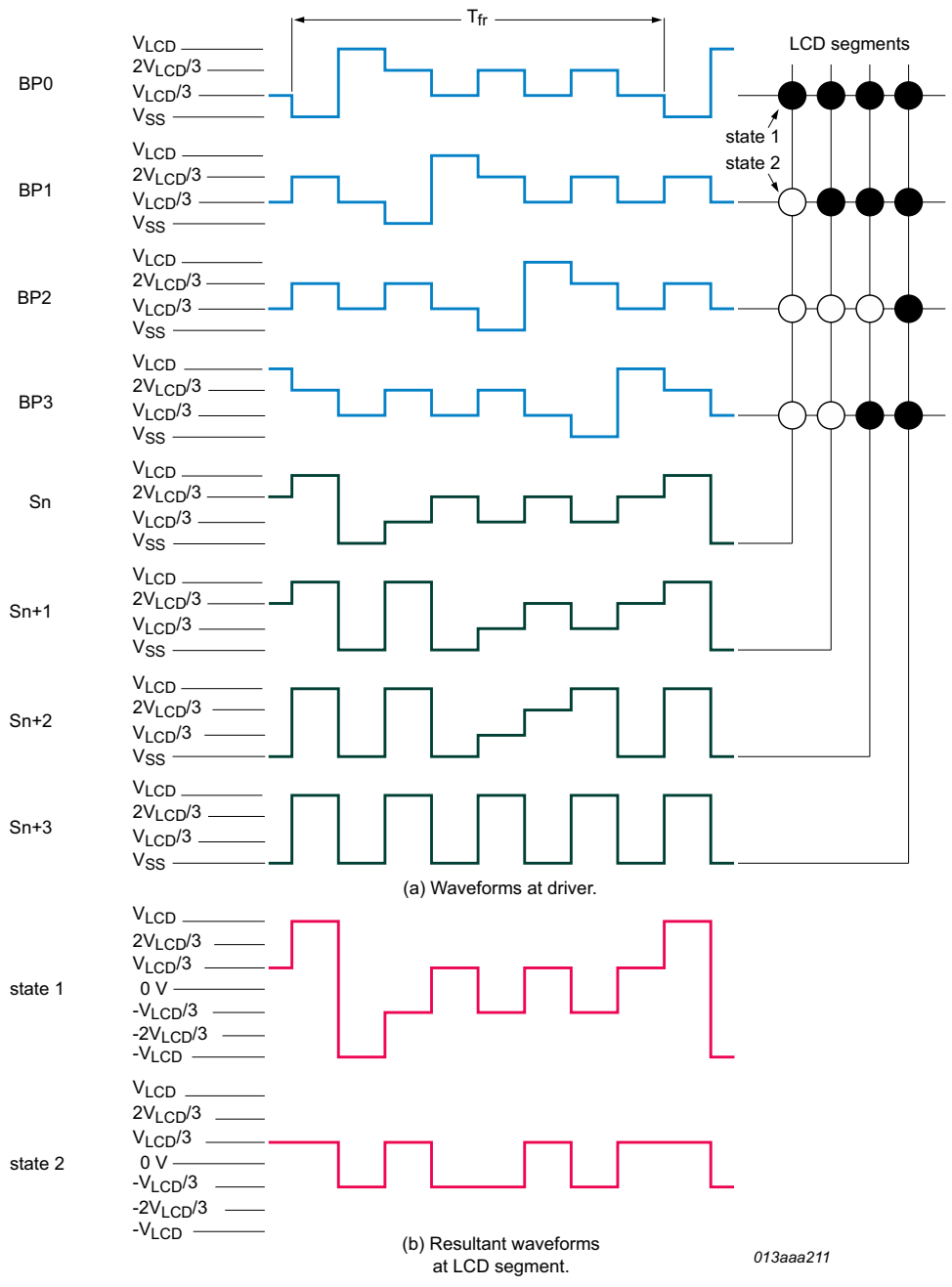
7.3.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 11.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 11. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

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7.4 Backplane and segment outputs

7.4.1 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In the 1:4 multiplex drive mode BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities.
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

The pins for the four backplanes BP0 to BP3 are available on both pin bars of the chip. In applications, it is possible to use either the pins for the backplanes

- on the top pin bar
- on the bottom pin bar
- or both of them to increase the driving strength of the device.

When using all backplanes available they may be connected to the respective sibling (BP0 on the top pin bar with BP0 on the bottom pin bar, and so on).

7.4.2 Segment outputs

The LCD drive section includes 160 segment outputs (S0 to S159) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display register. When less than 160 segment outputs are required, the unused segment outputs must be left open-circuit.

7.5 Display RAM

The display RAM is a static 160 $\times$ 4 bit RAM which stores LCD data. There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

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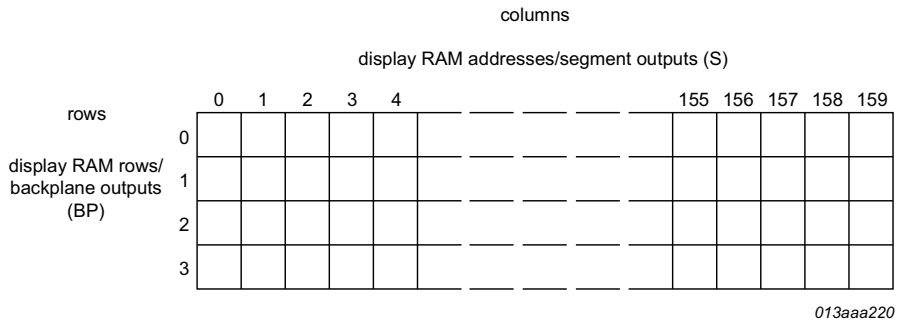
The display RAM bitmap, Figure 12, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 159 which correspond with the segment outputs S0 to S159. In multiplexed LCD applications the segment data of the first, second, third, and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM addresses and the segment outputs; and between the bits in a RAM word and the backplane outputs.

Fig 12. Display RAM bitmap

When display data is transmitted to the PCF85132, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 13. The RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 13:

- In static drive mode the eight transmitted data bits are placed in row 0 as 1 byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as four successive 2-bit RAM words.
- In 1:3 multiplex drive mode the 8 bits are placed in triples into row 0, 1, and 2 as 3 successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.5.3 on page 25).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as 2 successive 4-bit RAM words.

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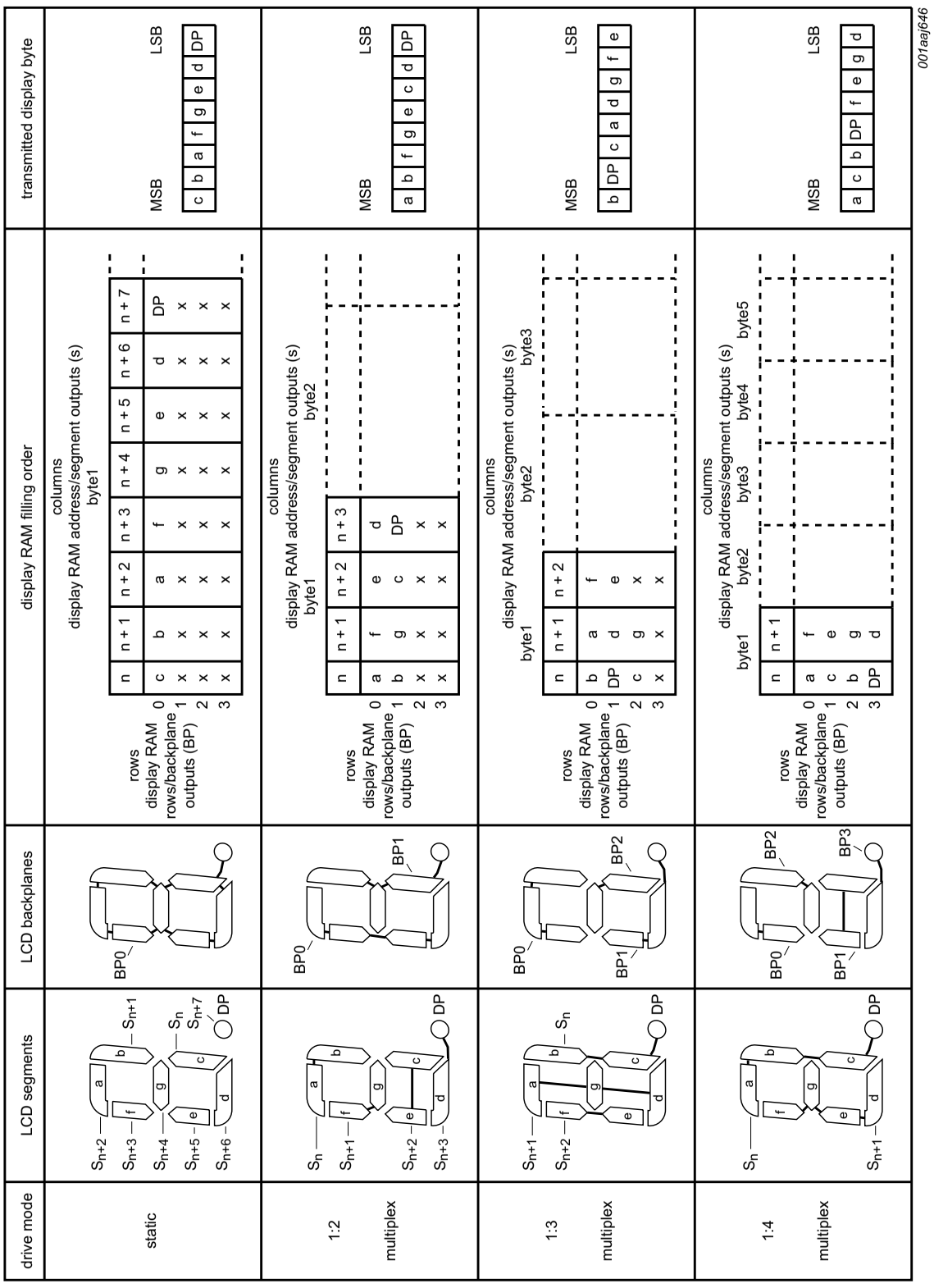

x = data bit unchanged

Fig 13. Relationships between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

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7.5.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see 7 on page 7 and Table 8 on page 7). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 13.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I^2C-bus data access is terminated early, then the state of the data pointer is unknown. The data pointer should be re-written before further RAM accesses.

7.5.2 Subaddress counter

The storage of display data is conditioned by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter matches with the hardware subaddress applied to A0 and A1. The subaddress counter value is defined by the device-select command (see Table 9 on page 7). If the content of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF85132 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the I^2C-bus interface.

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7.5.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 16 (see Figure 13 as well).

Table 16. Standard RAM filling in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 17.

Table 17. Entire RAM filling by rewriting in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 17 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8, and so on, have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written
- The data-pointer (see Section 7.1.2 on page 7) has to be set to the address of bit a1
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6
- The data-pointer has to be set to the address of bit b1
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

7.5.4 Bank selection

7.5.4.1 Output bank selector

The output bank selector (see Table 10 on page 8) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

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