Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PCF85134

Universal 60 x 4 LCD segment driver for multiplex rates up to 1:4

Rev. 4 — 11 May 2017 — Product data sheet

1. General description

The PCF85134 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 60 segments. It can be easily cascaded for larger LCD applications. The PCF85134 is compatible with most microcontrollers and communicates via the two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

Although there is a small difference in typical frequency frame and ESD test condition PCF85134 can be used as drop-in replacement to PCF8534 without any system circuit or firmware change.

For a selection of NXP LCD segment drivers, see Table 25 on page 45.

2. Features and benefits

- Single-chip LCD controller and driver
- Selectable backplane drive configurations: static, 2, 3, or 4 backplane multiplexing
- 60 segment outputs allowing to drive:
  - 30 7-segment alphanumeric characters
  - 15 14-segment alphanumeric characters
  - Any graphics of up to 240 elements
- Cascading supported for larger applications
- 60 × 4-bit display data storage RAM
- Wide LCD supply range: from 2.5 V for low threshold LCDs up to 6.5 V for high threshold twisted nematic LCDs
- Internal LCD bias generation with voltage follower buffers
- Selectable display bias configurations: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Wide logic power supply range: from 1.8 V to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption
- 400 kHz I²C-bus interface

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

- No external components required
- Display memory bank switching in static and duplex drive mode
- Versatile blinking modes
- Silicon gate CMOS process

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCF85134	PCF85134HL	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCF85134HL/1	PCF85134HL/1,118	LQFP80	REEL 13" Q1/T1 *STANDARD MARK SMD	1000	T_{amb} = −40 °C to +85 °C

4. Block diagram

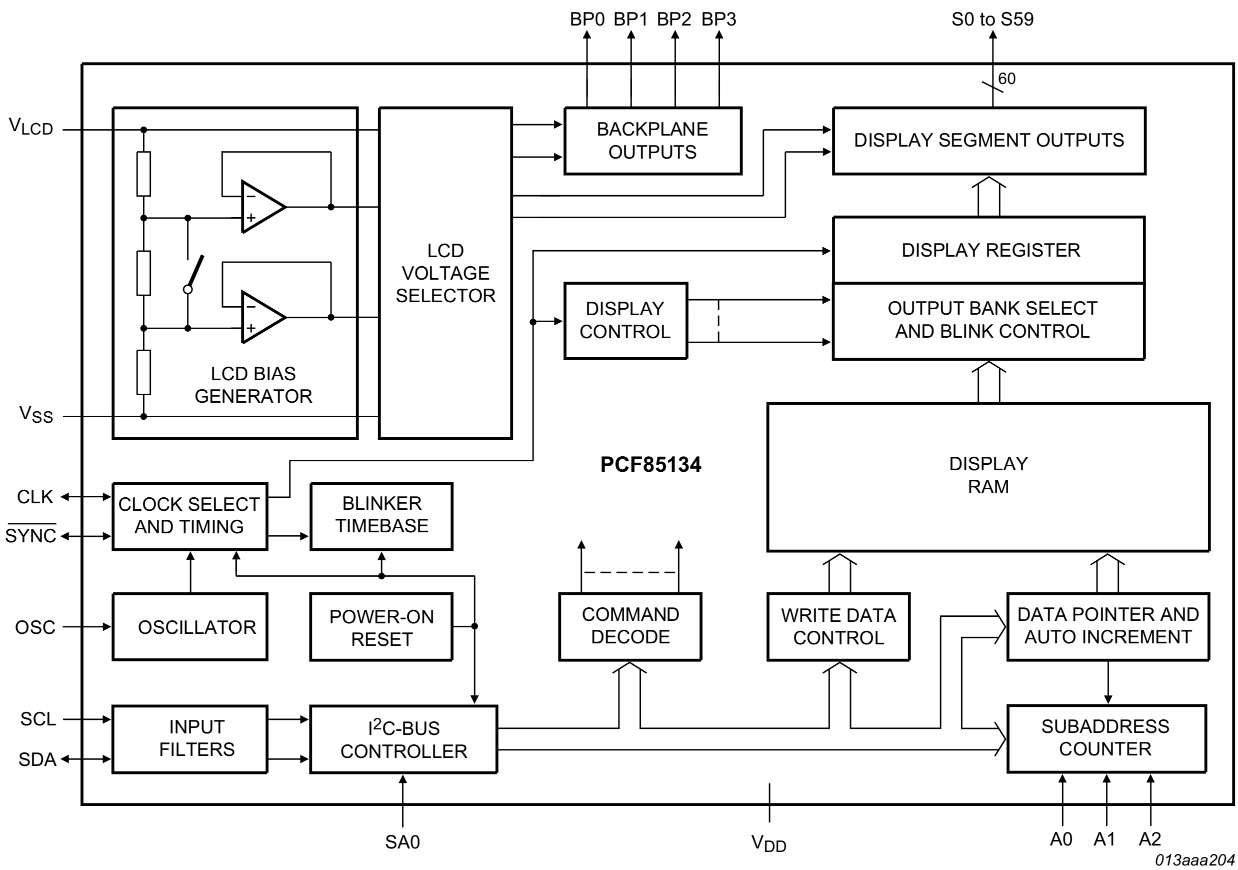
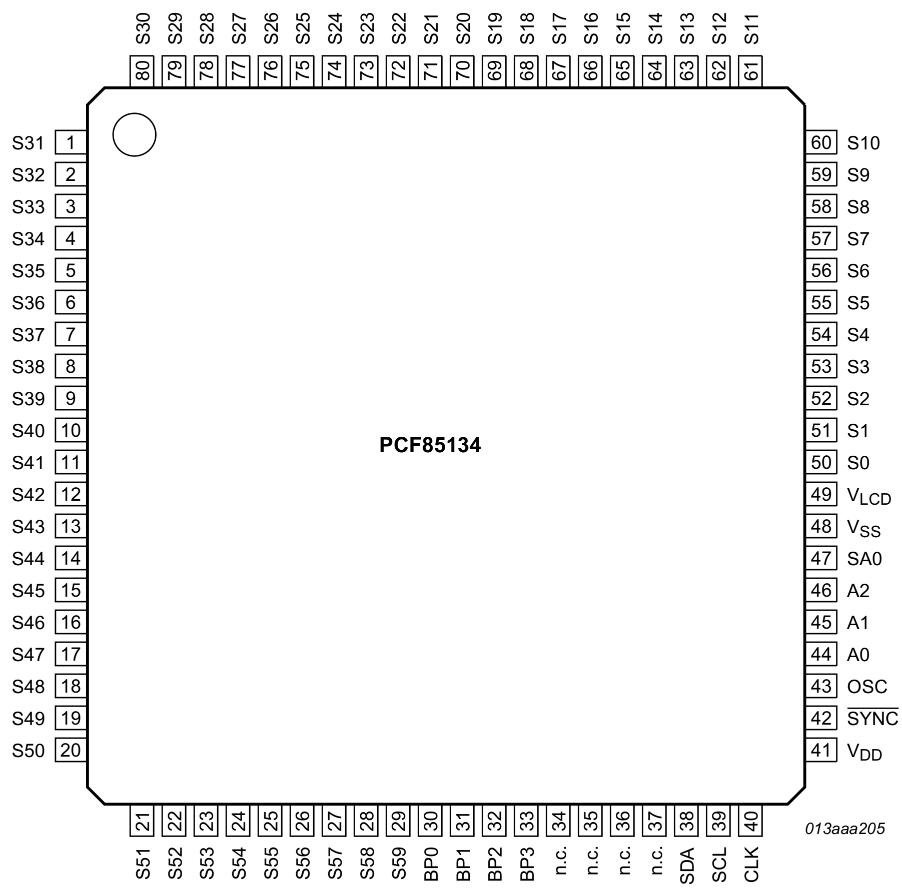


Fig 1. Block diagram of PCF85134

5. Pinning information

5.1 Pinning



Top view. For mechanical details, see Figure 24.

Fig 2. Pin configuration for SOT315-1 (PCF85134)

5.2 Pin description

Table 3. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
S31 to S59	1 to 29	output	LCD segment output 31 to 59
BP0 to BP3	30 to 33	output	LCD backplane output 0 to 3
n.c.	34 to 37	-	not connected; do not connect and do not use as feed through
SDA	38	input/output	I^{2}C-bus serial data input and output
SCL	39	input	I^{2}C-bus serial clock input
CLK	40	input/output	external clock input and internal clock output
V_{DD}	41	supply	supply voltage
$\overline{SYNC}$	42	input/output	cascade synchronization input and output (active LOW)
OSC	43	input	enable input for internal oscillator
A0 to A2	44 to 46	input	subaddress counter input 0 to 2
SA0	47	input	I^{2}C-bus slave address input 0
V_{SS}	48	supply	ground supply voltage
V_{LCD}	49	supply	input of LCD supply voltage
S0 to S30	50 to 80	output	LCD segment output 0 to 30

6. Functional description

The PCF85134 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 3). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 60 segments.

The display configurations possible with the PCF85134 depend on the required number of active backplane outputs. A selection of display configurations is given in Table 4.

All of the display configurations given in Table 4 can be implemented in a typical system as shown in Figure 4.

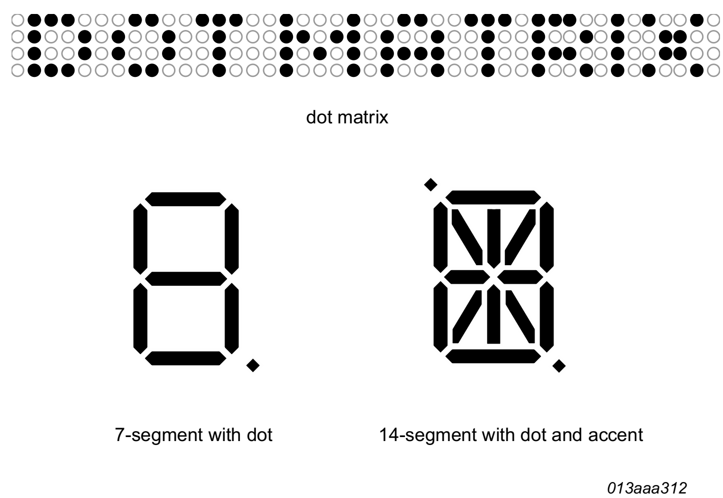


Fig 3. Example of displays suitable for PCF85134

Table 4. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment[1]	**14-segment[2]**	
4	240	30	15	240 (4 × 60)
3	180	22	11	180 (3 × 60)
2	120	15	7	120 (2 × 60)
1	60	7	3	60 (1 × 60)

[1] 7-segment display has eight elements including the decimal point.

[2] 14-segment display has 16 elements including decimal point and accent dot.

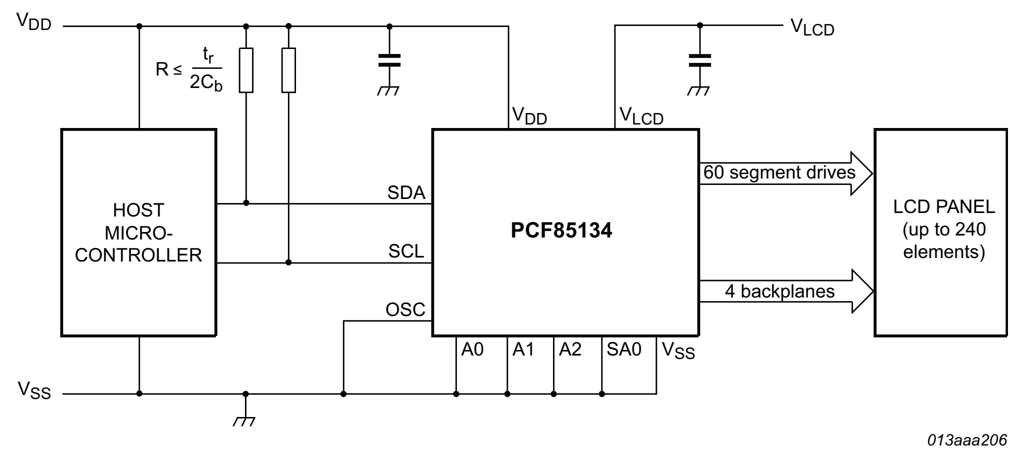


Fig 4. Typical system configuration

The host microcontroller maintains the 2-line I²C-bus communication channel with the PCF85134.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (pins V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

6.1 Power-On Reset (POR)

At power-on the PCF85134 resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I²C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled (bit E = 0, see Table 11)

Remark: Do not transfer data on the I²C-bus for at least 1 ms after a power-on to allow the reset action to complete.

6.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between V_{LCD} and V_{SS}. If the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex drive mode configuration is selected, the center impedance is bypassed by switch. The LCD voltage can be temperature compensated externally, using the supply to pin V_{LCD}.

6.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 5.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 5. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1 + a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

6.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determines the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 5. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes just named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

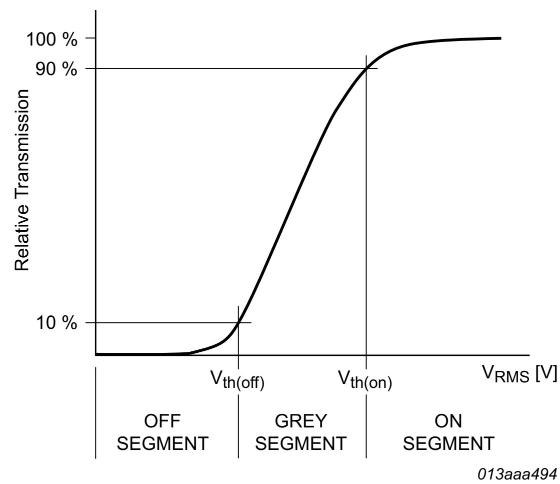
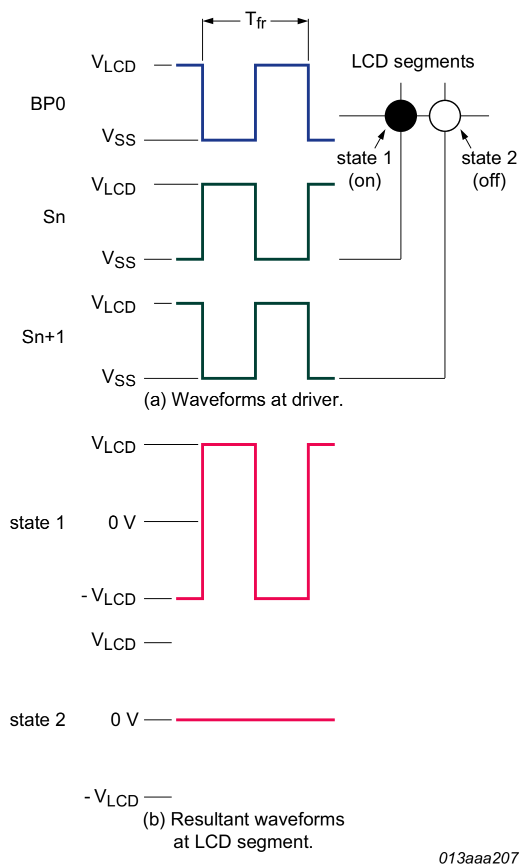


Fig 5. Electro-optical characteristic: relative transmission curve of the liquid

6.4 LCD drive mode waveforms

6.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 6.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

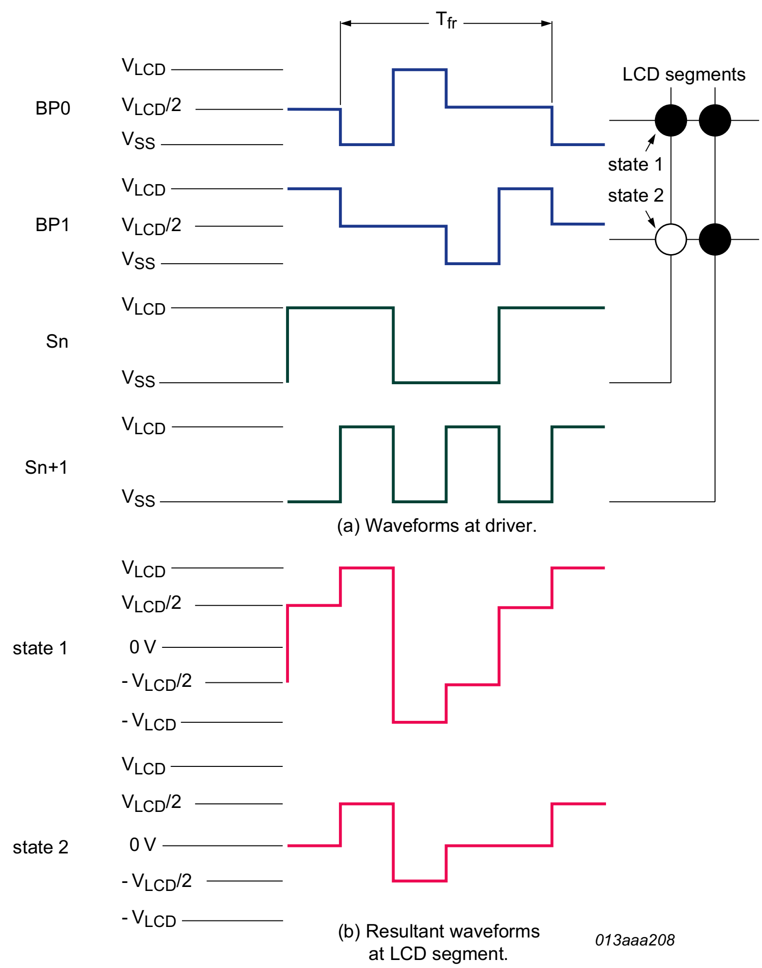
$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 6. Static drive mode waveforms

6.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF85134 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 7 and Figure 8.



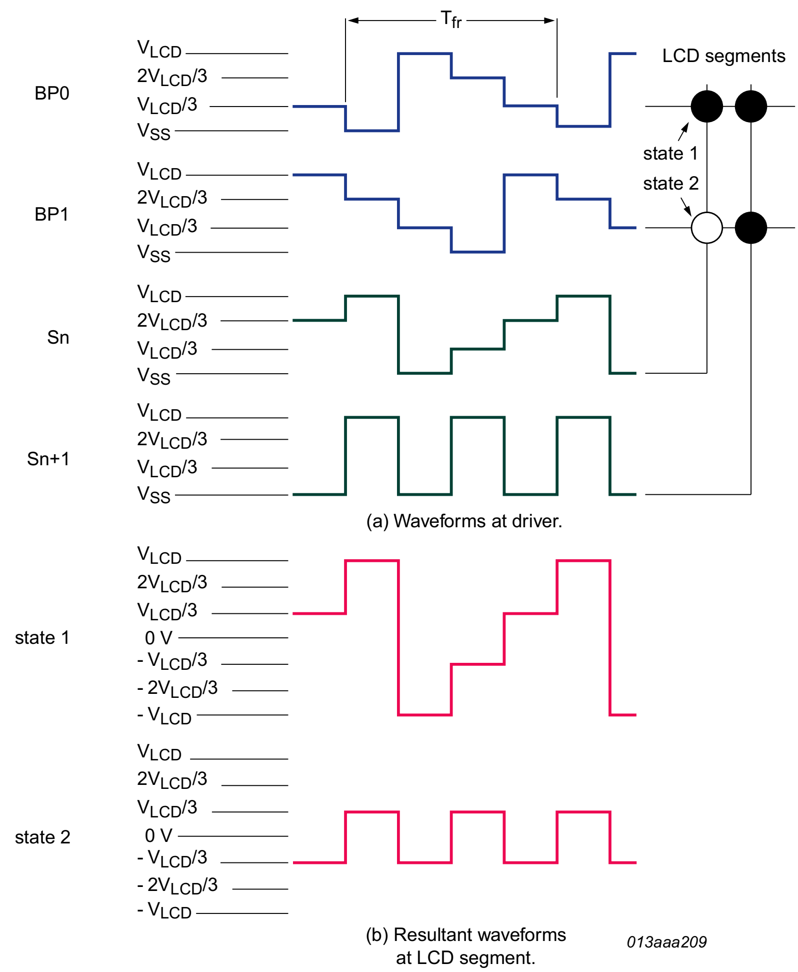
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791 V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354 V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

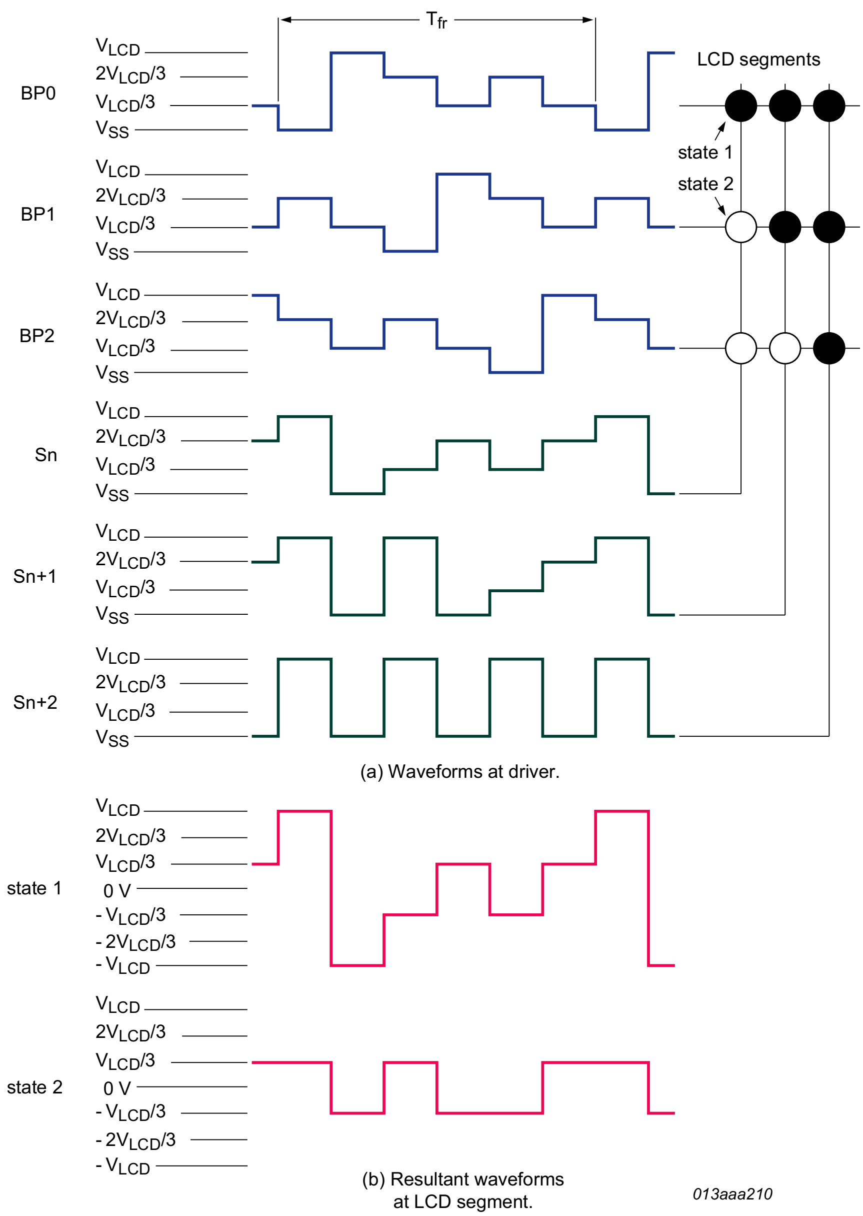
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

6.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 9.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

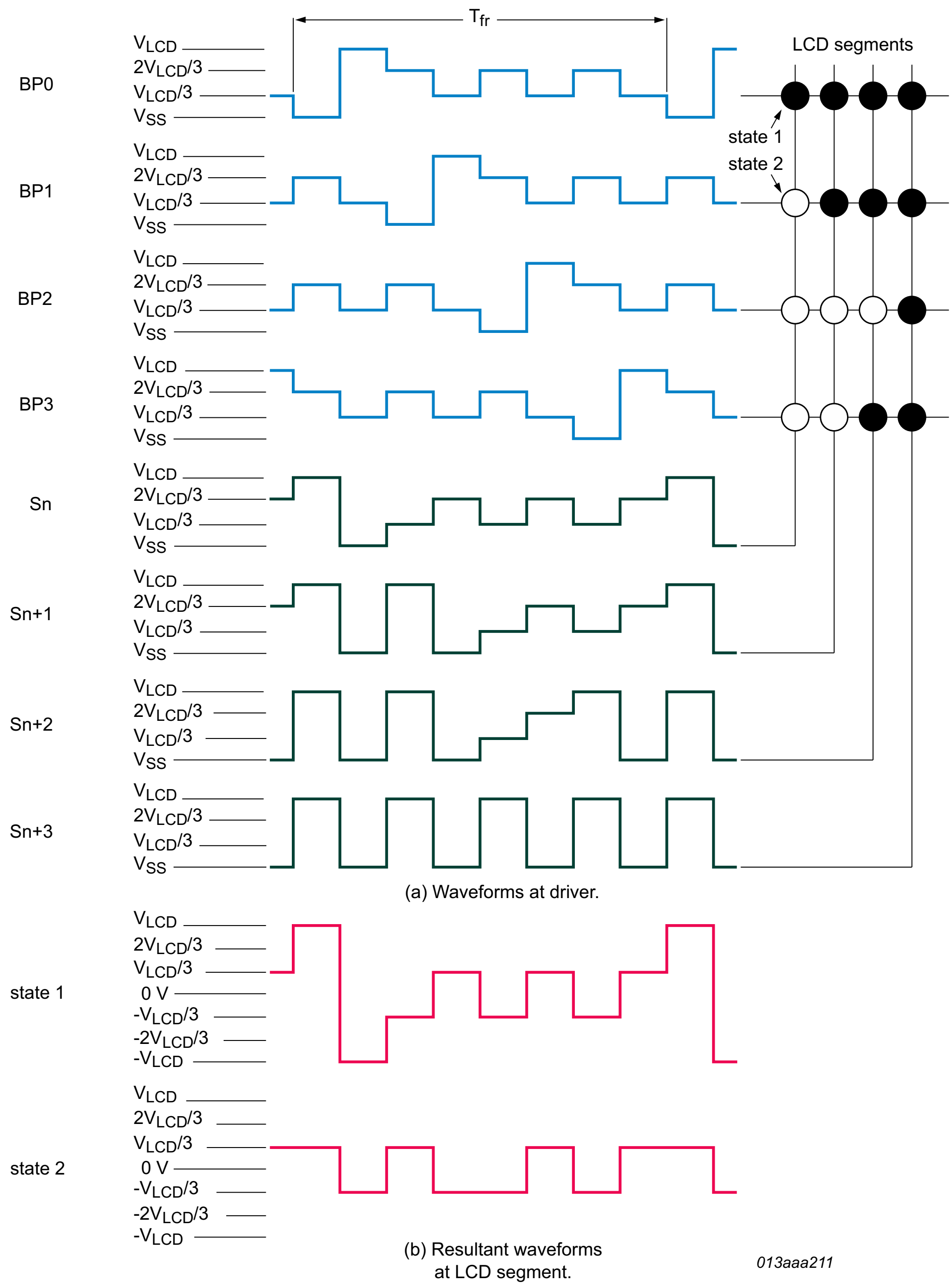
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

6.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 10.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

6.5 Oscillator

The internal logic and the LCD drive signals of the PCF85134 are timed by the frequency f_{clk}. It equals either the built-in oscillator frequency f_{osc} or the external clock frequency $f_{clk(ext)}$. The clock frequency f_{clk} determines the LCD frame frequency (f_{fr}).

6.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case, the output from pin CLK is the clock signal for any cascaded PCF85134 in the system.

6.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

Remark: A clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

6.6 Timing and frame frequency

The PCF85134 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF85134 in the system is maintained by the synchronization signal at pin $\overline{SYNC}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock.

Table 6. LCD frame frequencies

Operating mode ratio	Frame frequency with respect to f_{clk} (typical)	Unit
	f_{clk} = 1970 Hz	
$f_{fr} = \frac{f_{clk}}{24}$	82	Hz

6.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

6.8 Segment outputs

The LCD drive section includes 60 segment outputs (S0 to S59) which should be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 60 segment outputs are required, the unused segment outputs must be left open-circuit.

6.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode BP0 and BP2, respectively, BP1 and BP3 carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

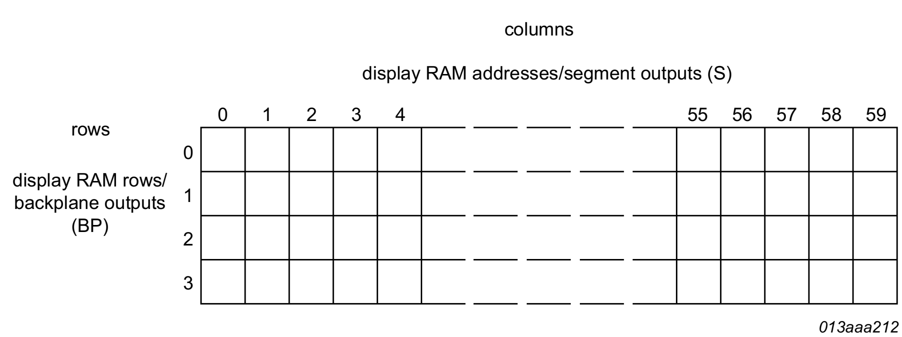
6.10 Display RAM

The display RAM is a static 60 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit map indicates the on-state ($V_{on(RMS)}$) of the corresponding LCD element. Similarly, a logic 0 indicates the off-state ($V_{off(RMS)}$). For more information on $V_{on(RMS)}$ and $V_{off(RMS)}$, see Section 6.3.

There is a one-to-one correspondence between

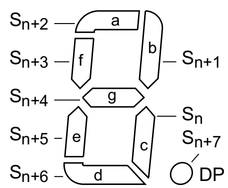
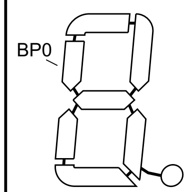
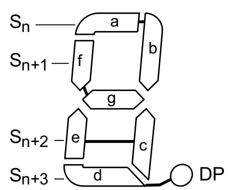
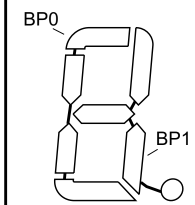
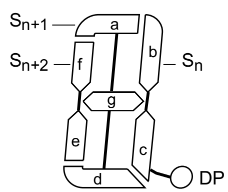
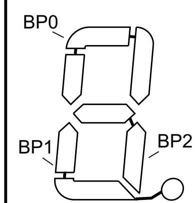
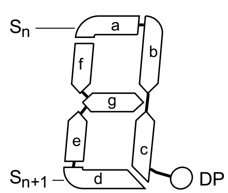
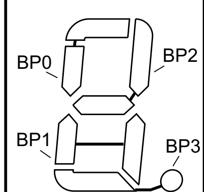
- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

The display RAM bit map, Figure 11, shows row 0 to row 3 which correspond with the backplane outputs BP0 to BP3, and column 0 to column 59 which correspond with the segment outputs S0 to S59. In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with BP0, row 1 with BP1, and so on).



The display RAM bit map shows the direct relationship between the display RAM addresses and the segment outputs and between the bits in a RAM word and the backplane outputs.

Fig 11. Display RAM bit map

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static			see static table below	MSB c b a f g e d DP LSB
1:2 multiplex			see 1:2 table below	MSB a b f g e c d DP LSB
1:3 multiplex			see 1:3 table below	MSB b DP c a d g f e LSB
1:4 multiplex			see 1:4 table below	MSB a c b DP f e g d LSB

static — columns: display RAM address/segment outputs (s), byte1; rows: display RAM rows/backplane outputs (BP)

rows	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
0	c	b	a	f	g	e	d	DP
1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

1:2 multiplex — columns: display RAM address/segment outputs (s), byte1, byte2; rows: display RAM rows/backplane outputs (BP)

rows	n	n + 1	n + 2	n + 3
0	a	f	e	d
1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

1:3 multiplex — columns: display RAM address/segment outputs (s), byte1, byte2, byte3; rows: display RAM rows/backplane outputs (BP)

rows	n	n + 1	n + 2
0	b	a	f
1	DP	d	e
2	c	g	x
3	x	x	x

1:4 multiplex — columns: display RAM address/segment outputs (s), byte1, byte2, byte3, byte4, byte5; rows: display RAM rows/backplane outputs (BP)

rows	n	n + 1
0	a	f
1	c	e
2	b	g
3	DP	d

001aaj646

x = data bit unchanged.

Fig 12. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

When display data is transmitted to the PCF85134, the display bytes received are stored in the display RAM in accordance with the selected LCD multiplex drive mode. The data is stored as it arrives and depending on the current multiplex drive mode, data is stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 12. The RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 12:

- In static drive mode the eight transmitted data bits are placed into row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and row 1 as four successive 2-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, row 1, and row 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address. But care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 6.10.3).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, row 1, row 2, and row 3 as two successive 4-bit RAM words.

6.10.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 10). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 12. After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^2C-bus data access terminates early, then the state of the data pointer is unknown. Consequently, the data pointer must be rewritten before further RAM accesses.

6.10.2 Subaddress counter

The storage of display data is determined by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter matches with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 13). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

In cascaded applications each PCF85134 in the cascade must be addressed separately. Initially, the first PCF85134 is selected by sending the device-select command matching the first hardware subaddress. Then the data pointer is set to the preferred display RAM address by sending the load-data-pointer command.

Once the display RAM of the first PCF85134 has been written, the second PCF85134 is selected by sending the device-select command again. This time however the command matches the hardware subaddress of the second device. Next the load-data-pointer command is sent to select the preferred display RAM address of the second PCF85134.

This last step is very important because during writing data to the first PCF85134, the data pointer of the second PCF85134 is incremented. In addition, the hardware subaddress should not be changed while the device is being accessed on the I^2C-bus interface.

6.10.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 7 (see Figure 12 as well).

Table 7. Standard RAM filling in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. ***are not connected*** *to any elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)									
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 8.

Table 8. Entire RAM filling by rewriting in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. ***are connected*** *to elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 8 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8, and so on, have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written.
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6.
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6.

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used. But it has to be considered in the module layout process as well as in the driver software design.

6.10.4 Bank selector

6.10.4.1 Output bank selector

The output bank selector (see Table 14) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The $\overline{\text{SYNC}}$ signal resets these sequences to the following starting points:

- row 3 for 1:4 multiplex
- row 2 for 1:3 multiplex
- row 1 for 1:2 multiplex
- row 0 for static mode

The PCF85134 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.10.4.2 Input bank selector

The input bank selector loads display data into the display data in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 14). The input bank selector functions independently to the output bank selector.

6.11 Blinking

The display blinking capabilities of the PCF85134 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 15). The blink frequencies are derived from the clock frequency. The ratio between the clock and blink frequency depends on the blink mode selected (see Table 9).

Table 9. Blink frequencies

Blink mode	Operating mode ratio	Blink frequency with respect to f_{clk} (typical)	Unit
		f_{clk} = 1970 Hz	
off	-	blinking off	Hz
1	$f_{blink} = \frac{f_{clk}}{768}$	2.5	Hz
2	$f_{blink} = \frac{f_{clk}}{1536}$	1.3	Hz
3	$f_{blink} = \frac{f_{clk}}{3072}$	0.6	Hz

An additional feature is for an arbitrary selection of LCD segments to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. With the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD elements can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 11).

6.12 Command decoder

The command decoder identifies command bytes that arrive on the I^{2}C-bus. There are five commands:

Table 10. Definition of commands

Command	Operation code								Reference
Bit	7	6	5	4	3	2	1	0	
mode-set	1	1	0	0	E	B	M[1:0]		Table 11
load-data-pointer	0	P[6:0]							Table 12
device-select	1	1	1	0	0	A[2:0]			Table 13
bank-select	1	1	1	1	1	0	I	O	Table 14
blink-select	1	1	1	1	0	AB	BF[1:0]		Table 15

Table 11. Mode-set command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**[1]
		0[2]	disabled (blank)[3]
		1	enable
2	B		**LCD bias configuration**[4]
		0[2]	1⁄3 bias
		1	1⁄2 bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; one backplane
		10	1:2 multiplex; two backplanes
		11	1:3 multiplex; three backplanes
		00[2]	1:4 multiplex; four backplanes

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[4] Not applicable for static drive mode.

Table 12. Load-data-pointer command bit description

See Section 6.10.1 on page 19.

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	0000000[1] to 0111011	7-bit binary value, 0 to 59; transferred to the data pointer to define one of 60 display RAM addresses

[1] Default value.

Table 13. Device-select command bit description

See Section 6.10.2 on page 19.

Bit	Symbol	Value	Description
7 to 3	-	11100	fixed value
2 to 0	A[2:0]	000[1] to 111	3-bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

[1] Default value.

Table 14. Bank-select command bit description

See Section 6.10.4 on page 21.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex**[1]
7 to 2	-	111110	fixed value	
1	I		**input bank selection**: storage of arriving display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**output bank selection**: retrieval of LCD display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 or 1:4 multiplex drive modes.

[2] Default value.

Table 15. Blink-select command bit description

See Section 6.11 on page 21.

Bit	Symbol	Value	Description
7 to 3	-	11110	fixed value
2	AB		**blink mode selection**
		0[1]	normal blinking[2]
		1	alternate RAM bank blinking[3]
1 to 0	BF[1:0]		**blink frequency selection**[4]
		00[1]	off
		01	1
		10	2
		11	3

[1] Default value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

[4] For the blink frequencies, see Table 9.

6.13 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF85134 and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

7. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 13.

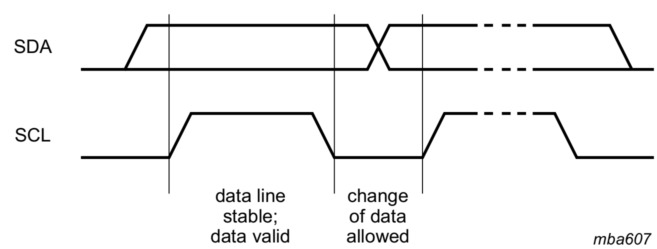


Fig 13. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

The START and STOP conditions are illustrated in Figure 14.

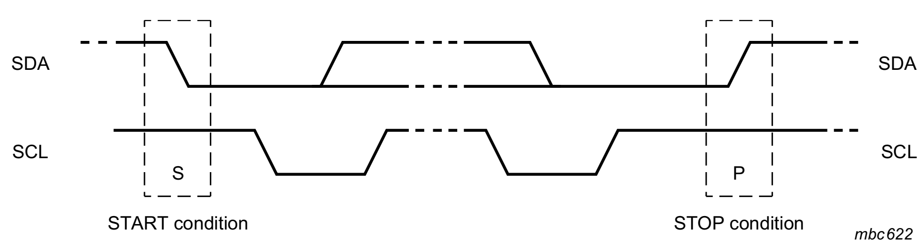


Fig 14. Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 15.