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PCF85176

40 x 4 universal LCD driver for low multiplex rates

Rev. 5 — 6 January 2015 Product data sheet

1. General description

The PCF85176 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCF85176 is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

For a selection of NXP LCD segment drivers, see Table 24 on page 49.

2. Features and benefits

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, ½, or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - Up to 20 7-segment numeric characters
  - Up to 10 14-segment alphanumeric characters
  - Any graphics of up to 160 segments/elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 6.5 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- May be cascaded for large LCD applications (up to 2560 segments/elements possible)
- No external components required
- Manufactured in silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF85176H	TQFP64	plastic thin quad flat package, 64 leads; body 10 × 10 × 1.0 mm	SOT357-1
PCF85176T	TSSOP56	plastic thin shrink small outline package, 56 leads; body width 6.1 mm	SOT364-1

3.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF85176H/1	935290063518	PCF85176H/1,518	1	tape and reel, 13 inch, dry pack
PCF85176T/1	935290075118	PCF85176T/1,118	1	tape and reel, 13 inch

4. Marking

Table 3. Marking codes

Product type number	Marking code
PCF85176H/1	PCF85176H
PCF85176T/1	PCF85176T

5. Block diagram

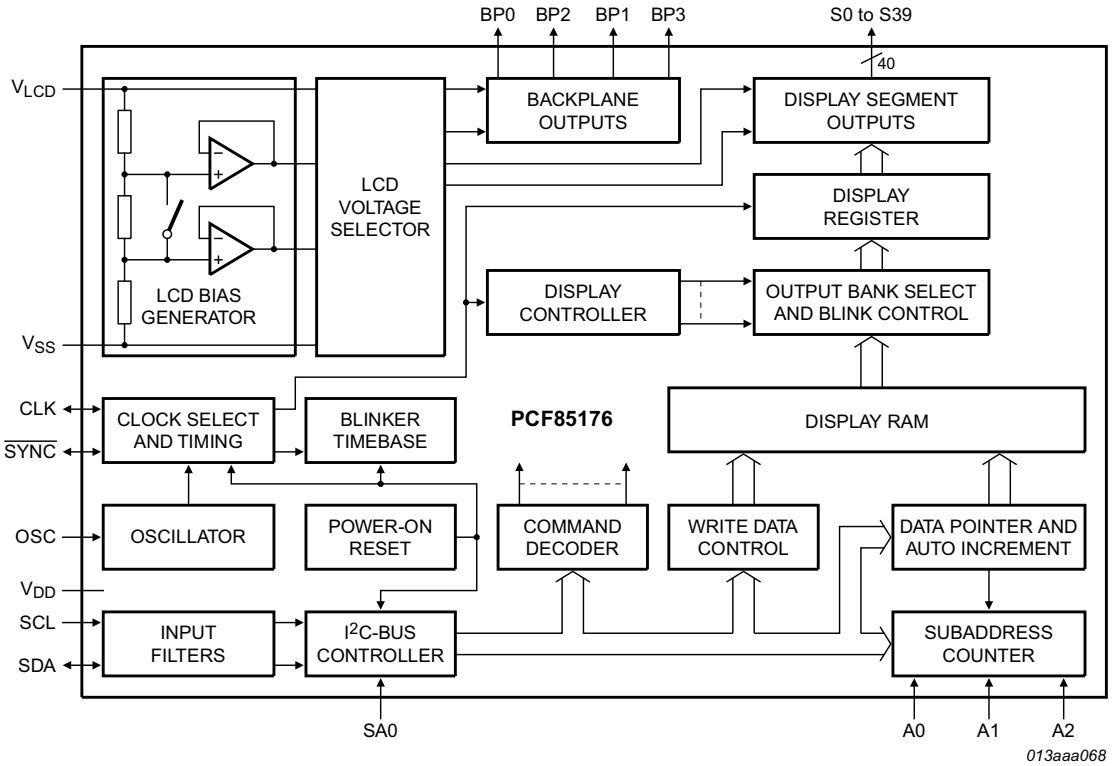
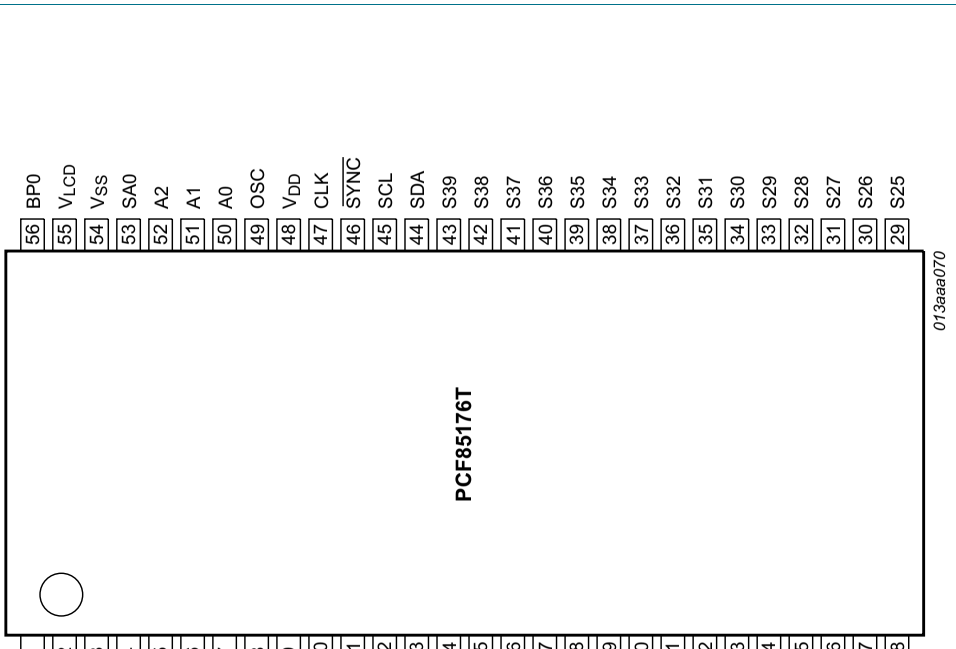


Fig 1. Block diagram of PCF85176

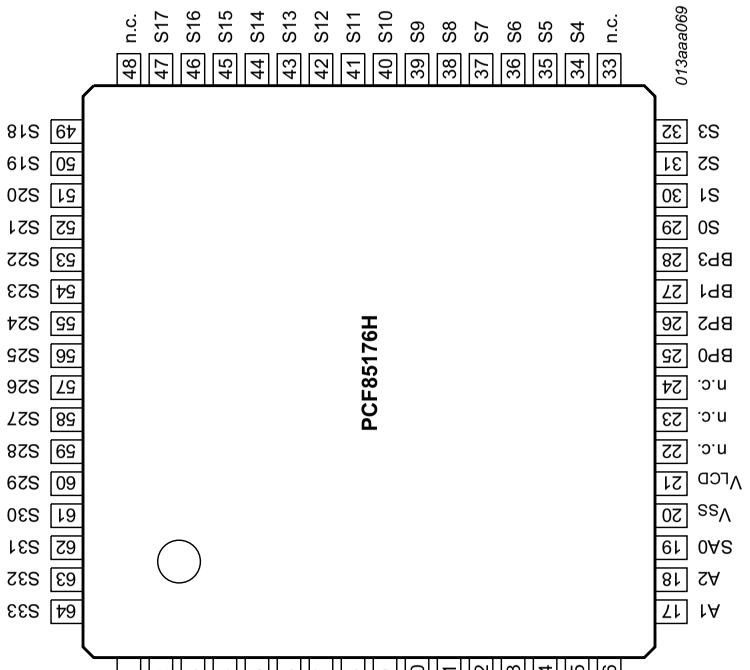
6. Pinning information

6.1 Pinning



Top view. For mechanical details, see Figure 30.

Fig 3. Pinning diagram for TSSOP56 (PCF85176T)



Top view. For mechanical details, see Figure 29.

Fig 2. Pinning diagram for TQFP64 (PCF85176H)

6.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin			Description
	TQFP64 (PCF85176H)	TSSOP56 (PCF85176T)	Type	
SDA	10	44	input/output	I^2C-bus serial data line
SCL	11	45	input	I^2C-bus serial clock
CLK	13	47	input/output	clock line
V_{DD}	14	48	supply	supply voltage
$\overline{SYNC}$	12	46	input/output	cascade synchronization input or output; if not used it must be left open
OSC	15	49	input	internal oscillator enable
A0 to A2	16 to 18	50 to 52	input	subaddress inputs
SA0	19	53	input	I^2C-bus address input
V_{SS}	20	54	supply	ground supply voltage
V_{LCD}	21	55	supply	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	56, 1, 2, 3	output	LCD backplane outputs
S0 to S39	29 to 32, 34 to 47, 49 to 64, 2 to 7	4 to 43	output	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	-	not connected; do not connect and do not use as feed through

7. Functional description

The PCF85176 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 4). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

7.1 Commands of PCF85176

The commands available to the PCF85176 are defined in Table 5.

Table 5. Definition of PCF85176 commands

Bit position labeled as - is not used.

Command	Operation Code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	C	1	0	-	E	B	M[1:0]		Table 7
load-data-pointer	C	0	P[5:0]						Table 8
device-select	C	1	1	0	0	A[2:0]			Table 9
bank-select	C	1	1	1	1	0	I	O	Table 10
blink-select	C	1	1	1	0	AB	BF[1:0]		Table 11

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 22. When this bit is set logic 1, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is set logic 0, it indicates that the command byte is the last in the transfer. Further bytes are regarded as display data (see Table 6).

Table 6. C bit description

Bit	Symbol	Value	Description
7	C		**continue bit**
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

7.1.1 Command: mode-set

The mode-set command allows configuring the multiplex mode, the bias levels and enabling or disabling the display.

Table 7. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6 to 5	-	10	fixed value
4	-	-	unused
3	E		**display status**[1]
		0[2]	disabled (blank)[3]
		1	enabled
2	B		**LCD bias configuration**[4]
		0[2]	1/3 bias
		1	1/2 bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00[2]	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[4] Not applicable for static drive mode.

7.1.2 Command: load-data-pointer

The load-data-pointer command defines the display RAM address where the following display data are sent to.

Table 8. Load-data-pointer command bit description

See Section 7.6.1.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6	-	0	fixed value
5 to 0	P[5:0]	000000[1] to 100111	6-bit binary value, 0 to 39; transferred to the data pointer to define one of 40 display RAM addresses

[1] Default value.

7.1.3 Command: device-select

The device-select command allows defining the subaddress counter value.

Table 9. Device-select command bit description

See Section 7.6.2.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6 to 3	-	1100	fixed value
2 to 0	A[2:0]	000[1] to 111	3-bit binary value, 0 to 7; transferred to the subaddress counter to define 1 of 8 hardware subaddresses

[1] Default value.

7.1.4 Command: bank-select

The bank-select command controls where data is written to RAM and where it is displayed from.

Table 10. Bank-select command bit description

See Section 7.6.5.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7	C	0, 1	see Table 6	
6 to 2	-	11110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

[2] Default value.

7.1.5 Command: blink-select

The blink-select command allows configuring the blink mode and the blink frequency.

Table 11. Blink-select command bit description

See Section 7.1.5.1.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6 to 3	-	1110	fixed value
2	AB		**blink mode selection**
		0[1]	normal blinking[2]
		1	alternate RAM bank blinking[3]
1 to 0	BF[1:0]		**blink frequency selection**
		00[1]	off
		01	1
		10	2
		11	3

[1] Default value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.1.5.1 Blinking

The display blinking capabilities of the PCF85176 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 11). The blink frequencies are derived from the clock frequency. The ratio between the clock and blink frequencies depends on the blink mode selected (see Table 12).

An additional feature is for an arbitrary selection of LCD segments/elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. With the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternative RAM bank is available, groups of LCD segments/elements can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 7).

Table 12. Blink frequencies

Blink mode	Blink frequency[1]
off	-
1	$f_{blink} = \frac{f_{clk}}{768}$
2	$f_{blink} = \frac{f_{clk}}{1536}$
3	$f_{blink} = \frac{f_{clk}}{3072}$

[1] The blink frequency is proportional to the clock frequency (f_{clk}). For the range of the clock frequency, see Table 20.

7.2 Power-On Reset (POR)

At power-on the PCF85176 resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $^1/_3$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled (bit E = 0, see Table 7)

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.3 Possible display configurations

The possible display configurations of the PCF85176 depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 13. All of these configurations can be implemented in the typical system shown in Figure 5.

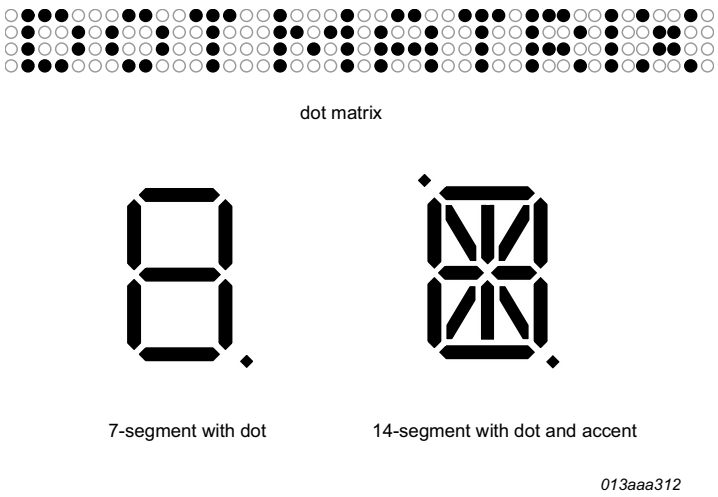


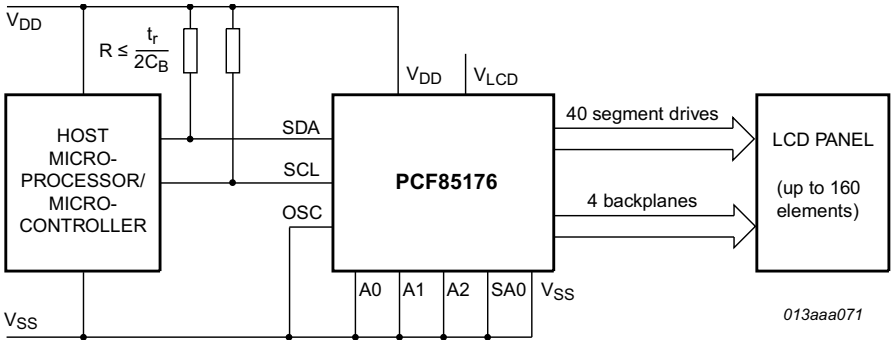
Fig 4. Example of displays suitable for PCF85176

Table 13. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix: segments/ elements**
		7-segment[1]	**14-segment[2]**	
4	160	20	10	160 (4 × 40)
3	120	15	7	120 (3 × 40)
2	80	10	5	80 (2 × 40)
1	40	5	2	40 (1 × 40)

[1] 7 segment display has 8 segments/elements including the decimal point.

[2] 14 segment display has 16 segments/elements including decimal point and accent dot.



The resistance of the power lines must be kept to a minimum.

Fig 5. Typical system configuration

The host microcontroller maintains the 2-line I²C-bus communication channel with the PCF85176. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

7.3.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the ½ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

7.3.2 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.3.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 14.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 14. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2+2a+n}{n\times(1+a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2-2a+n}{n\times(1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2+2a+n}{a^2-2a+n}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6}\times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4\times\sqrt{3})}{3}\right] = 2.309V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 6. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \tag{4}$$

$$V_{off(RMS)} \leq V_{th(off)} \tag{5}$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

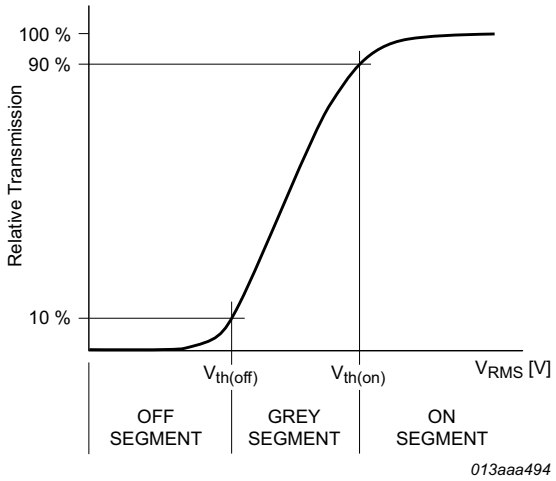
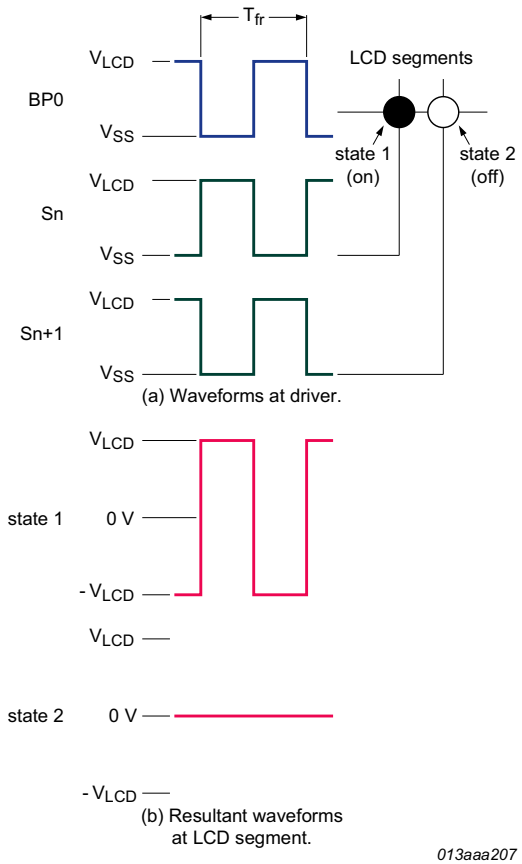


Fig 6. Electro-optical characteristic: relative transmission curve of the liquid

7.3.4 LCD drive mode waveforms

7.3.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment (Sn) drive waveforms for this mode are shown in Figure 7.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

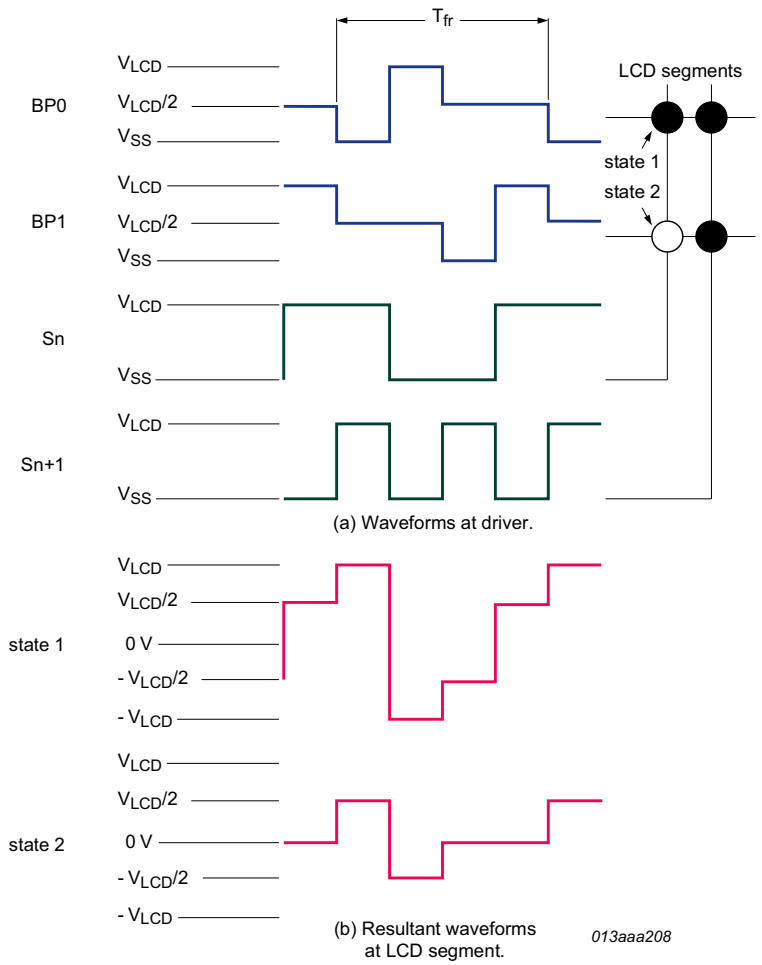
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 7. Static drive mode waveforms

7.3.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF85176 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 8 and Figure 9.



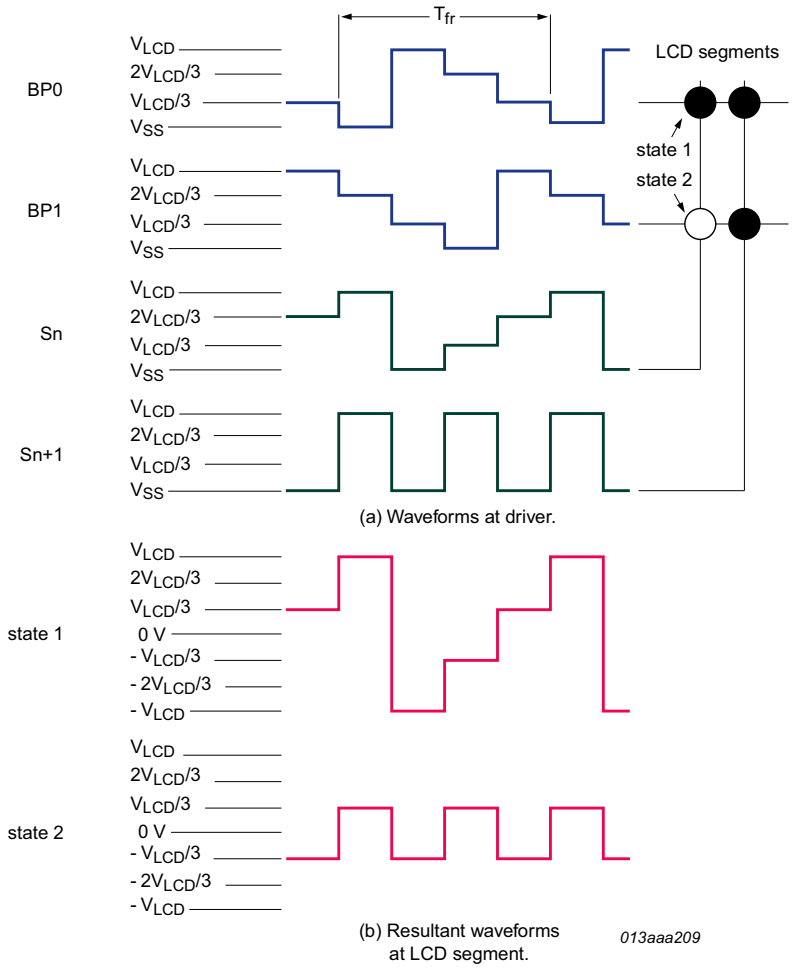
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

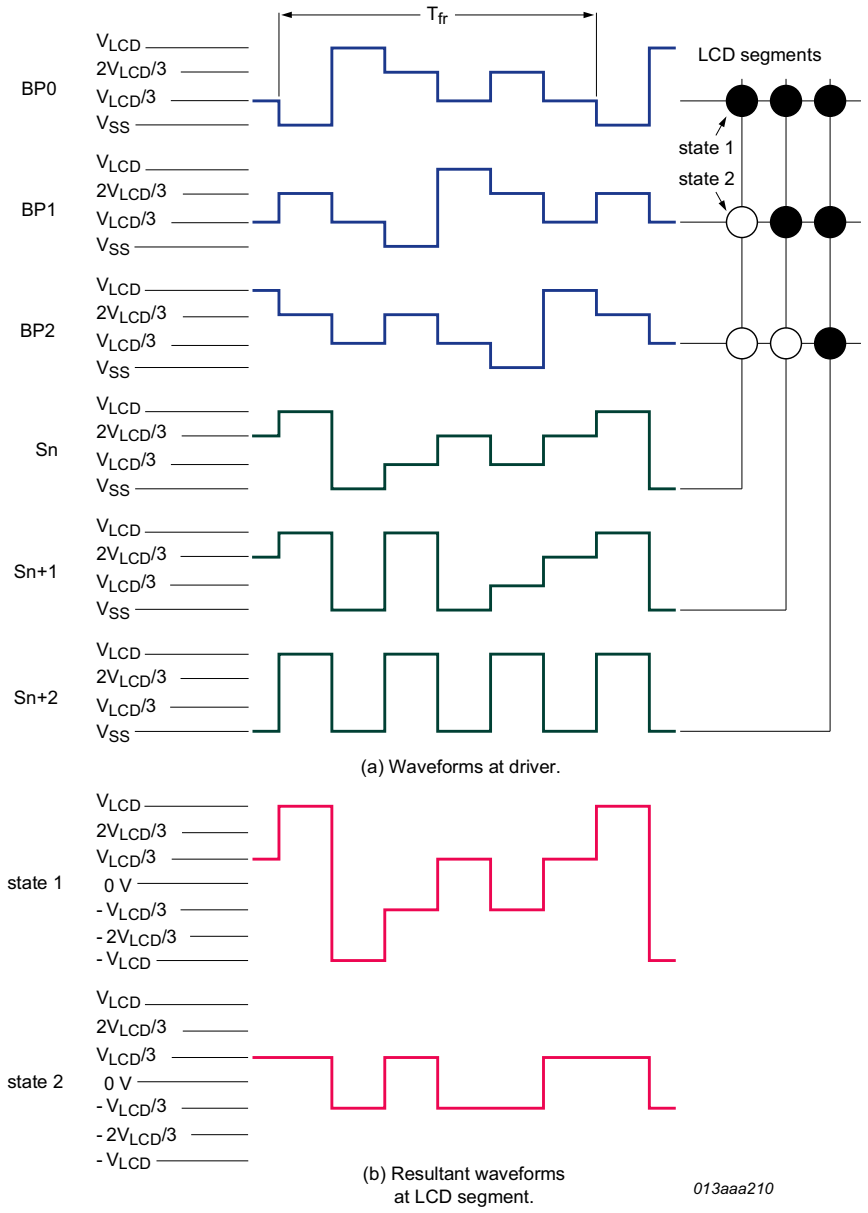
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.3.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 10.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

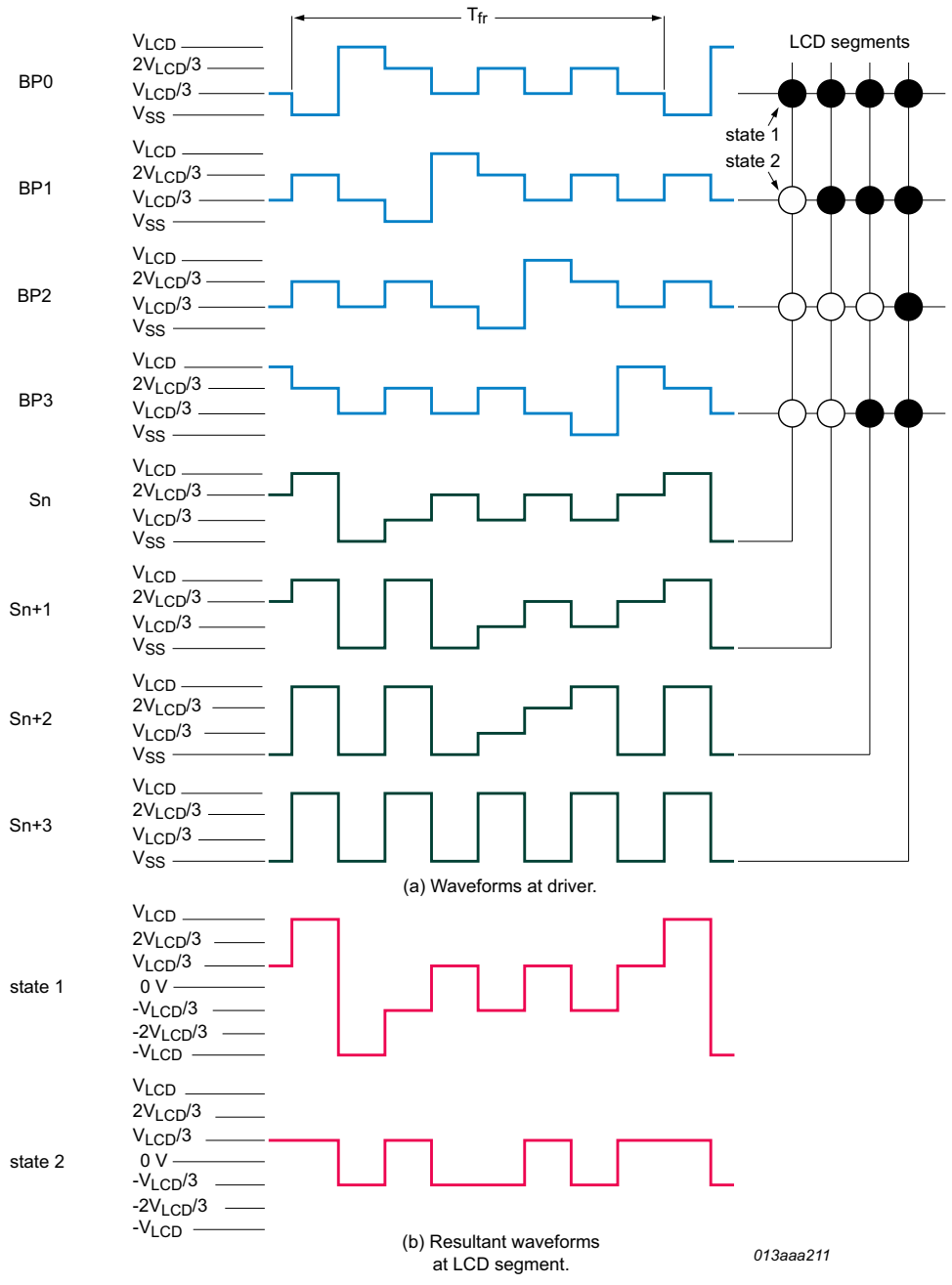
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.3.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 11.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 11. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.4 Oscillator

7.4.1 Internal clock

The internal logic of the PCF85176 and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCF85176 in the system that are connected in cascade.

7.4.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}. The LCD frame frequency is determined by the clock frequency (f_{clk}).

Remark: A clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.4.3 Timing

The PCF85176 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF85176 in the system is maintained by the synchronization signal at pin $\overline{\text{SYNC}}$. The timing also generates the LCD frame frequency signal. The frame frequency signal is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$

7.5 Backplane and segment outputs

7.5.1 Backplane outputs

The LCD drive section includes 4 backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities
- In 1:2 multiplex drive mode, BP0 and BP2, respectively, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements

7.5.2 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.6 Display RAM

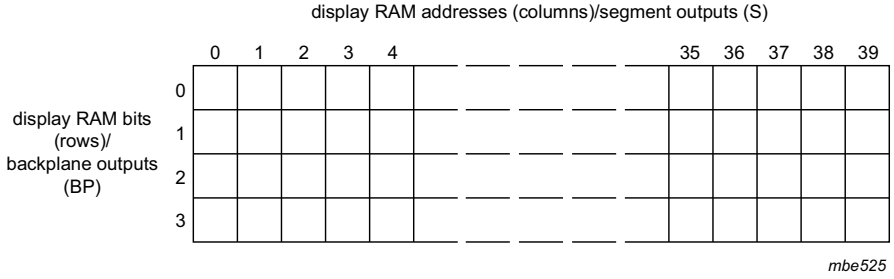
The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD segments/elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bitmap, Figure 12, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third, and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.

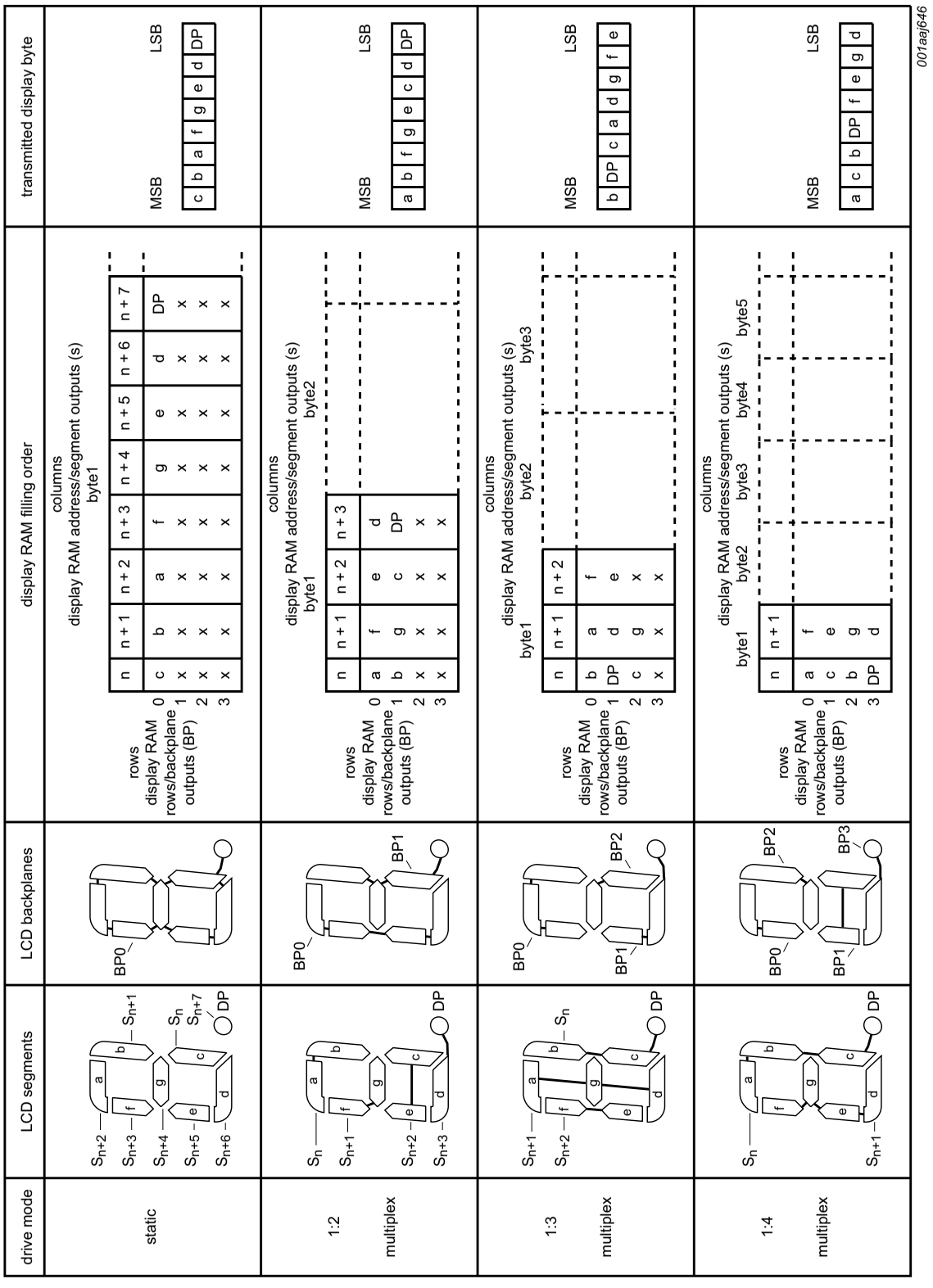


The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs; and between the bits in a RAM row and the backplane outputs.

Fig 12. Display RAM bitmap

When display data is transmitted to the PCF85176, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 13. The RAM filling organization depicted applies equally to other LCD types.

- In static drive mode the eight transmitted data bits are placed into row 0 as 1 byte
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as four successive 2-bit RAM words
- In 1:3 multiplex drive mode the 8 bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.6.3)
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words



x = data bit unchanged.

Fig 13. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

7.6.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 8). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 13.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I^2C-bus data access terminates early, then the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

7.6.2 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed only when the content of the subaddress counter matches with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 9). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF85176 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the I^2C-bus interface.

7.6.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 15 (see Figure 13 as well).

Table 15. Standard RAM filling in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any segments/elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 16.

Table 16. Entire RAM filling by rewriting in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to segments/elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 16, the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 etc. have to be connected to segments/elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written
- The data-pointer (see Section 7.6.1 on page 23) has to be set to the address of bit a1
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6
- The data-pointer has to be set to the address of bit b1
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some segments/elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

7.6.4 Writing over the RAM address boundary

In all multiplex drive modes, depending on the setting of the data pointer, it is possible to fill the RAM over the RAM address boundary. If the PCF85176 is part of a cascade the additional bits fall into the next device that also generates the acknowledge signal. If the PCF85176 is a single device or the last device in a cascade, the additional bits are discarded and no acknowledge signal is generated.

7.6.5 Bank selection

7.6.5.1 Output bank selector

The output bank selector (see Table 10) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCF85176 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.6.5.2 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 10). The input bank selector functions independently to the output bank selector.

7.6.5.3 RAM bank switching

The PCF85176 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. A bank can be thought of as one RAM row or a collection of RAM rows (see Figure 14). The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete.