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PCF8523

Real-Time Clock (RTC) and calendar

Rev. 7 — 28 April 2015 Product data sheet

1. General description

The PCF8523 is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power consumption. Data is transferred serially via the I²C-bus with a maximum data rate of 1 000 kbit/s. Alarm and timer functions are available with the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine-tuning of the clock. The PCF8523 has a backup battery switch-over circuit, which detects power failures and automatically switches to the battery supply when a power failure occurs.

For a selection of NXP Real-Time Clocks, see Table 56 on page 68

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.0 V to 5.5 V
- Low backup current: typical 150 nA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 2 line bidirectional 1 MHz Fast-mode Plus (Fm+) I²C interface, read D1h, write D0h[2]
- Battery backup input pin and switch-over circuit
- Freely programmable timer and alarm with interrupt capability
- Selectable integrated oscillator load capacitors for C_L = 7 pF or C_L = 12.5 pF
- Oscillator stop detection function
- Internal Power-On Reset (POR)
- Open-drain interrupt or clock output pins
- Programmable offset register for frequency adjustment

3. Applications

- Time keeping application
- Battery powered devices
- Metering

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 22.
2. Devices with other I²C-bus slave addresses can be produced on request.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8523T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCF8523TK	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 4 × 4 × 0.85 mm	SOT909-1
PCF8523TS	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
PCF8523U	bare die	12 bumps (6-6)	PCF8523U

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8523T/1	935293581118	PCF8523T/1,118	1	tape and reel, 13 inch
PCF8523TK/1	935293573118	PCF8523TK/1,118	1	tape and reel, 13 inch
PCF8523TS/1	935291196112	PCF8523TS/1,112	1	tube
	935291196118	PCF8523TS/1,118	1	tape and reel, 13 inch
PCF8523U/12AA/1	935293887005	PCF8523U/12AA/1,00	1	chips with bumps[1], sawn wafer on Film Frame Carrier (FFC)

[1] Bump hardness see Table 53.

Table 3. PCF8523U wafer information

Type number	Wafer thickness	Wafer diameter	FFC for wafer size	Marking of bad die
PCF8523U/12AA/1	200 μm	6 inch	8 inch	wafer mapping

5. Marking

Table 4. Marking codes

Type number	Marking code
PCF8523T/1	8523T
PCF8523TK/1	8523
PCF8523TS/1	8523TS
PCF8523U/12AA/1	PC8523-1

6. Block diagram

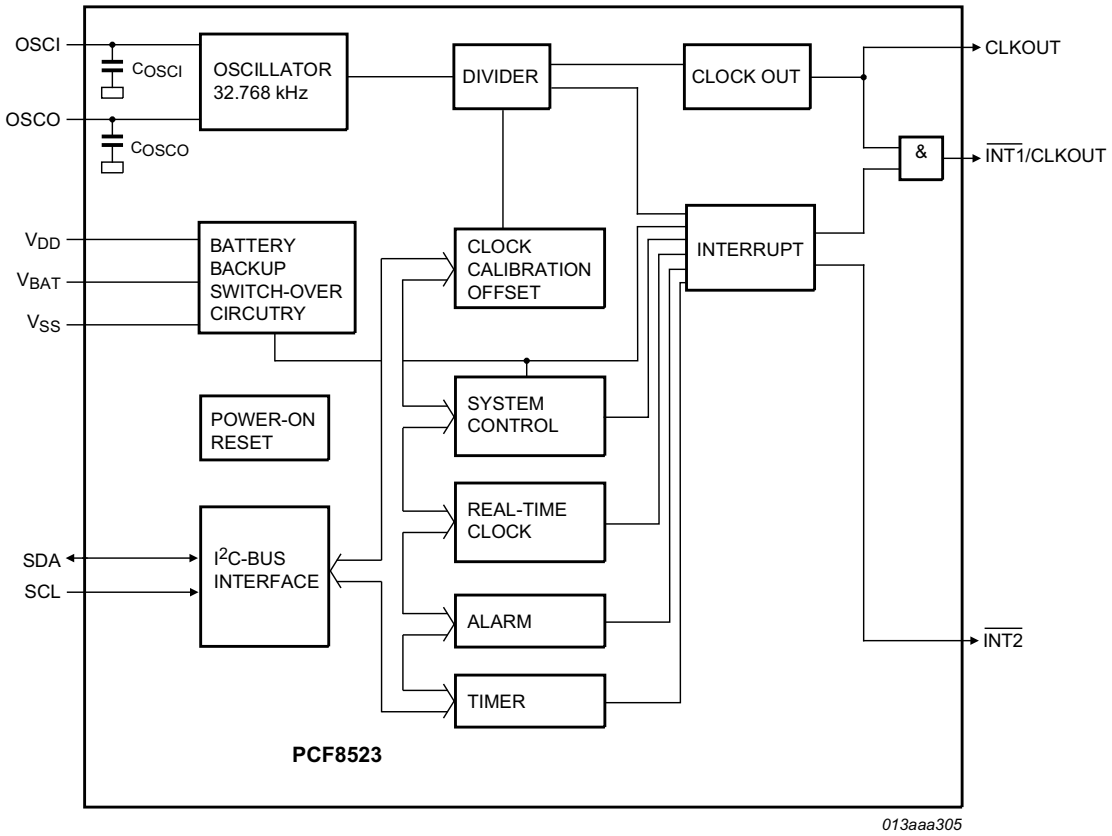
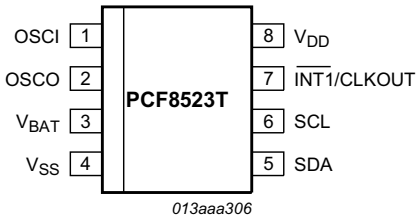


Fig 1. Block diagram of PCF8523

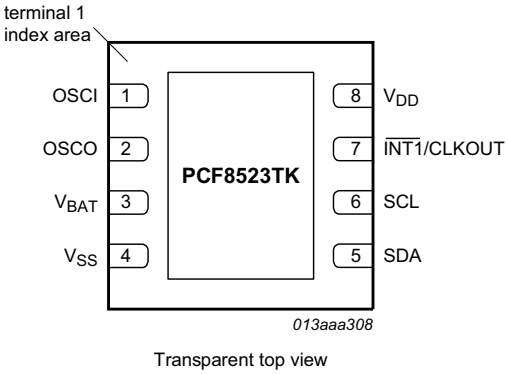
7. Pinning information

7.1 Pinning



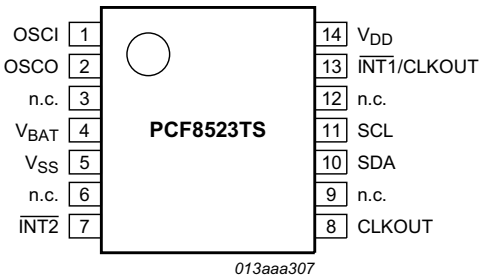
Top view. For mechanical details, see Figure 39 on page 56.

Fig 2. Pin configuration for SO8 (PCF8523T)



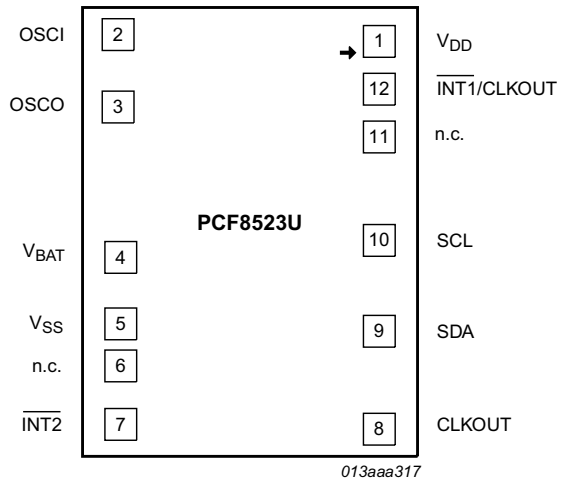
For mechanical details, see Figure 40 on page 57.

Fig 3. Pin configuration for HVSON8 (PCF8523TK)



Top view. For mechanical details, see Figure 41 on page 58.

Fig 4. Pin configuration for TSSOP14 (PCF8523TS)



Viewed from active side. For mechanical details, see Figure 42 on page 59.

Fig 5. Pin configuration for PCF8523U

7.2 Pin description

Table 5. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin				Type	Description
	SO8 (PCF8523T)	HVSON8 (PCF8523TK)	TSSOP14 (PCF8523TS)	PCF8523U		
OSCI	1	1	1	2	input	oscillator input; high-impedance node[1]
OSCO	2	2	2	3	output	oscillator output; high-impedance node[1]
n.c.	-	-	3, 6, 9, 12[2]	6 and 11[2]	-	not connected; do not connect and do not use it as feed through
V_{BAT}	3	3	4	4	supply	battery supply voltage
V_{SS}	4	4[3]	5	5[4]	supply	ground supply voltage
$\overline{INT2}$	-	-	7	7	output	interrupt 2 (open-drain, active LOW)
CLKOUT[5]	-	-	8	8	output	clock output (open-drain)
SDA	5	5	10	9	input/output	serial data input/output
SCL	6	6	11	10	input	serial clock input
$\overline{INT1}$/CLKOUT[5]	7	7	13	12	output	interrupt 1/clock output (open-drain)
V_{DD}	8	8	14	1	supply	supply voltage

[1] Wire length between quartz and package should be minimized.

[2] For manufacturing tests only; do not connect it and do not use it.

[3] The die paddle (exposed pad) is connected to V_{SS} and should be electrically isolated.

[4] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

[5] The PCF8523 can either drive the CLKOUT or the $\overline{INT1}$.

8. Functional description

The PCF8523 contains:

- 20 8-bit registers with an auto-incrementing address register
- An on-chip 32.768 kHz oscillator with two integrated load capacitors
- A frequency divider, which provides the source clock for the Real-Time Clock (RTC)
- A programmable clock output
- A 1 Mbit/s I^2C-bus interface
- An offset register, which allows fine-tuning of the clock

All 20 registers are designed as addressable 8-bit registers although not all bits are implemented.

- The first three registers (memory address 00h, 01h, and 02h) are used as control and status registers
- The addresses 03h through 09h are used as counters for the clock function (seconds up to years)
- Addresses 0Ah through 0Dh define the alarm condition
- Address 0Eh defines the offset calibration
- Address 0Fh defines the clock-out mode and the addresses 10h and 12h the timer mode
- Addresses 11h and 13h are used for the timers

The registers Seconds, Minutes, Hours, Days, Weekdays, Months, and Years are all coded in Binary Coded Decimal (BCD) format. Other registers are either bit-wise or standard binary. When one of the RTC registers is read, the contents of all counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.

The PCF8523 has a battery backup input pin and battery switch-over circuit. The battery switch-over circuit monitors the main power supply and switches automatically to the backup battery when a power failure condition is detected. Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery. When the battery voltage goes below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

8.1 Registers overview

The 20 registers of the PCF8523 are auto-incrementing after each read or write data byte up to register 13h. After register 13h, the auto-incrementing will wrap around to address 00h (see Figure 6).

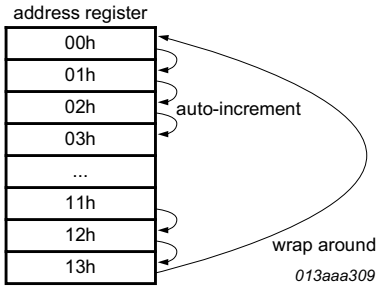


Fig 6. Auto-incrementing of the registers

Table 6. Registers overview

Bit positions labeled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control registers									
00h	Control_1	CAP_SEL	T	STOP	SR	12_24	SIE	AIE	CIE
01h	Control_2	WTAF	CTAF	CTBF	SF	AF	WTAIE	CTAIE	CTBIE
02h	Control_3	PM[2:0]			-	BSF	BLF	BSIE	BLIE
Time and date registers									
03h	Seconds	OS	SECONDS (0 to 59)						
04h	Minutes	-	MINUTES (0 to 59)						
05h	Hours	-	-	AMPM	HOURS (1 to 12 in 12 hour mode)				
				HOURS (0 to 23 in 24 hour mode)					
06h	Days	-	-	DAYS (1 to 31)					
07h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		
08h	Months	-	-	-	MONTHS (1 to 12)				
09h	Years	YEARS (0 to 99)							
Alarm registers									
0Ah	Minute_alarm	AEN_M	MINUTE_ALARM (0 to 59)						
0Bh	Hour_alarm	AEN_H	-	AMPM	HOUR_ALARM (1 to 12 in 12 hour mode)				
			-	HOUR_ALARM (0 to 23 in 24 hour mode)					
0Ch	Day_alarm	AEN_D	-	DAY_ALARM (1 to 31)					
0Dh	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
Offset register									
0Eh	Offset	MODE	OFFSET[6:0]						

Table 6. Registers overview *…continued*

Bit positions labeled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
CLOCKOUT and timer registers									
0Fh	Tmr_CLKOUT_ctrl	TAM	TBM	COF[2:0]			TAC[1:0]		TBC
10h	Tmr_A_freq_ctrl	-	-	-	-	-	TAQ[2:0]		
11h	Tmr_A_reg	T_A[7:0]							
12h	Tmr_B_freq_ctrl	-	TBW[2:0]			-	TBQ[2:0]		
13h	Tmr_B_reg	T_B[7:0]							

8.2 Control and status registers

8.2.1 Register Control_1

Table 7. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description
7	CAP_SEL		internal oscillator capacitor selection for quartz crystals with a corresponding load capacitance
		0[1]	7 pF
		1	12.5 pF
6	T	0[1][2]	unused
5	STOP	0[1]	RTC time circuits running
		1	RTC time circuits frozen; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available
4	SR	0[1][3]	no software reset
		1	initiate software reset
3	12_24	0[1]	24 hour mode is selected
		1	12 hour mode is selected
2	SIE	0[1]	second interrupt disabled
		1	second interrupt enabled
1	AIE	0[1]	alarm interrupt disabled
		1	alarm interrupt enabled
0	CIE	0[1]	no correction interrupt generated
		1	interrupt pulses are generated at every correction cycle (see Section 8.8)

[1] Default value.

[2] Must always be written with logic 0.

[3] For a software reset, 01011000 (58h) must be sent to register Control_1 (see Section 8.3). Bit SR always returns 0 when read.

8.2.2 Register Control_2

Table 8. Control_2 - control and status register 2 (address 01h) bit description

Bit	Symbol	Value	Description
7	WTAF	0[1]	no watchdog timer A interrupt generated
		1	flag set when watchdog timer A interrupt generated; flag is read-only and cleared by reading register Control_2
6	CTAF	0[1]	no countdown timer A interrupt generated
		1	flag set when countdown timer A interrupt generated; flag must be cleared to clear interrupt
5	CTBF	0[1]	no countdown timer B interrupt generated
		1	flag set when countdown timer B interrupt generated; flag must be cleared to clear interrupt
4	SF	0[1]	no second interrupt generated
		1	flag set when second interrupt generated; flag must be cleared to clear interrupt
3	AF	0[1]	no alarm interrupt generated
		1	flag set when alarm triggered; flag must be cleared to clear interrupt
2	WTAIE	0[1]	watchdog timer A interrupt is disabled
		1	watchdog timer A interrupt is enabled
1	CTAIE	0[1]	countdown timer A interrupt is disabled
		1	countdown timer A interrupt is enabled
0	CTBIE	0[1]	countdown timer B interrupt is disabled
		1	countdown timer B interrupt is enabled

[1] Default value.

8.2.3 Register Control_3

Table 9. Control_3 - control and status register 3 (address 02h) bit description

Bit	Symbol	Value	Description
7 to 5	PM[2:0]	see Table 11[1]	battery switch-over and battery low detection control
4	-	-	unused
3	BSF	0[2]	no battery switch-over interrupt generated
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt
2	BLF	0[2]	battery status ok
		1	battery status low; flag is read-only
1	BSIE	0[2]	no interrupt generated from battery switch-over flag, BSF
		1	interrupt generated when BSF is set
0	BLIE	0[2]	no interrupt generated from battery low flag, BLF
		1	interrupt generated when BLF is set

[1] Default value is 111.

[2] Default value.

8.3 Reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. Software reset command means setting bits 6, 4, and 3 in register Control_1 (00h) logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see Figure 7.

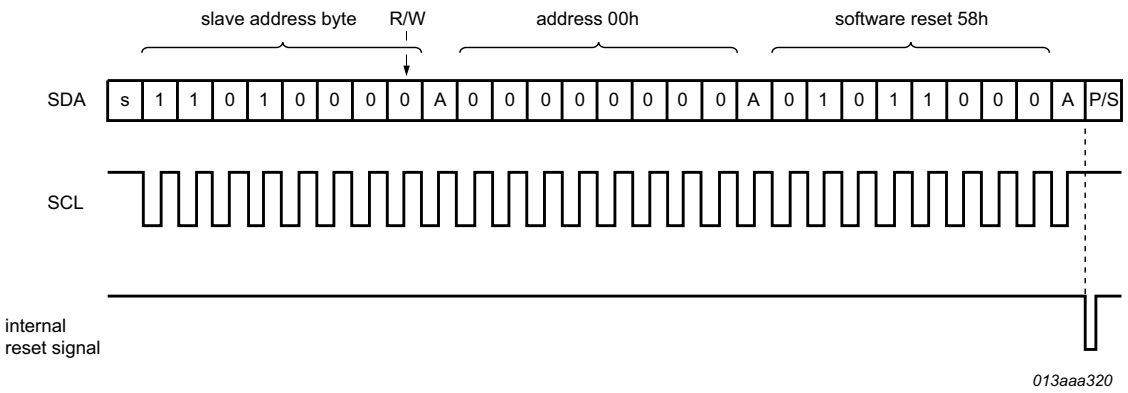


Fig 7. Software reset command

Table 10. Register reset values

Bits labeled X are undefined at power-on and unchanged by subsequent resets. Bits labeled - are not implemented.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	0	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Control_3	1	1	1	-	0	0	0	0
03h	Seconds	1	X	X	X	X	X	X	X
04h	Minutes	-	X	X	X	X	X	X	X
05h	Hours	-	-	X	X	X	X	X	X
06h	Days	-	-	X	X	X	X	X	X
07h	Weekdays	-	-	-	-	-	X	X	X
08h	Months	-	-	-	X	X	X	X	X
09h	Years	X	X	X	X	X	X	X	X
0Ah	Minute_alarm	1	X	X	X	X	X	X	X
0Bh	Hour_alarm	1	-	X	X	X	X	X	X
0Ch	Day_alarm	1	-	X	X	X	X	X	X
0Dh	Weekday_alarm	1	-	-	-	-	X	X	X
0Eh	Offset	0	0	0	0	0	0	0	0
0Fh	Tmr_CLKOUT_ctrl	0	0	0	0	0	0	0	0
10h	Tmr_A_freq_ctrl	-	-	-	-	-	1	1	1
11h	Tmr_A_reg	X	X	X	X	X	X	X	X
12h	Tmr_B_freq_ctrl	-	0	0	0	-	1	1	1
13h	Tmr_B_reg	X	X	X	X	X	X	X	X

After reset, the following mode is entered:

- 32.768 kHz CLKOUT active
- 24 hour mode is selected
- Register Offset is set logic 0
- No alarms set
- Timers disabled
- No interrupts enabled
- Battery switch-over is disabled
- Battery low detection is disabled
- 7 pF of internal oscillator capacitor selected

8.4 Interrupt function

Active low interrupt signals are available at pin $\overline{\text{INT1}}$/CLKOUT and $\overline{\text{INT2}}$. Pin $\overline{\text{INT1}}$/CLKOUT has both functions of $\overline{\text{INT1}}$ and CLKOUT combined, that is that either the CLKOUT or the $\overline{\text{INT1}}$ can be used. Therefore the usage of $\overline{\text{INT1}}$ requires that CLKOUT is disabled.

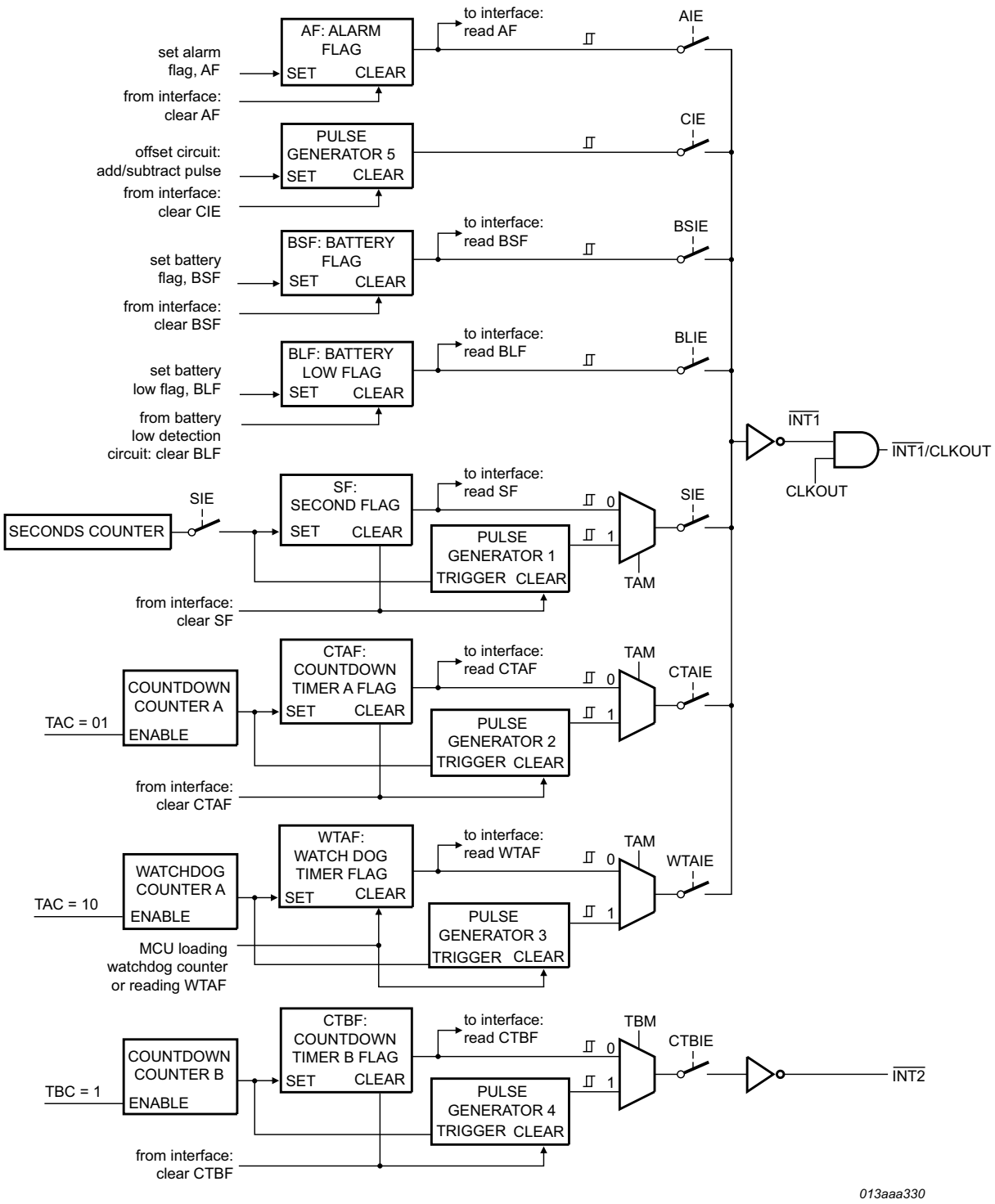
$\overline{\text{INT1}}$ Interrupt output may be sourced from different places:

- Second timer
- Timer A
- Timer B
- Alarm
- Battery switch-over
- Battery low detection
- Clock offset correction pulse

$\overline{\text{INT2}}$ interrupt output is sourced only from timer B:

The control bit TAM (register Tmr_CLKOUT_ctrl) is used to configure whether the interrupts generated from the second interrupt timer and timer A are pulsed signals or a permanently active signal. The control bit TBM (register Tmr_CLKOUT_ctrl) is used to configure whether the interrupt generated from timer B is a pulsed signal or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal, which follows the status of the corresponding flags.

- The flags SF, CTAF, CTBF, AF, and BSF can be cleared by using the interface
- WTAF is read only. Reading of the register Control_2 (01h) automatically resets WTAF (WTAF = 0) and clears the interrupt
- The flag BLF is read only. It is cleared automatically from the battery low detection circuit when the battery is replaced



When SIE, CTAIE, WTAIE, CTBIE, AIE, CIE, BSIE, BLIE, and clock-out are disabled, then $\overline{INT1}$ remains high-impedance. When CTBIE is disabled, then $\overline{INT2}$ remains high-impedance.

Fig 8. Interrupt block diagram

8.5 Power management functions

The PCF8523 has two power supply pins:

- V_{DD} - the main power supply input pin
- V_{BAT} - the battery backup input pin

The PCF8523 has two power management functions implemented:

- Battery switch-over function
- Battery low detection function

The power management functions are controlled by the control bits PM[2:0] in register Control_3 (02h):

Table 11. Power management function control bits

PM[2:0]	Function
000	battery switch-over function is enabled in standard mode; battery low detection function is enabled
001	battery switch-over function is enabled in direct switching mode; battery low detection function is enabled
010,011[1]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is enabled
100	battery switch-over function is enabled in standard mode; battery low detection function is disabled
101	battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
110	not allowed
111[2][3]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is disabled

[1] When the battery switch-over function is disabled, the PCF8523 works only with the power supply V_{DD}.

[2] When the battery switch-over function is disabled, the PCF8523 works only with the power supply V_{DD} and the battery low detection function is disabled. V_{BAT} must be put to V_{DD}.

[3] Default value.

8.5.1 Standby mode

When the device is first powered up from the battery (V_{BAT}) but without a main supply (V_{DD}), the PCF8523 automatically enters the standby mode. In standby mode, the PCF8523 does not draw any power from the backup battery until the device is powered up from the main power supply V_{DD}. Thereafter, the device switches over to battery backup mode whenever the main power supply V_{DD} is lost.

It is also possible to enter into standby mode when the chip is already supplied by the main power supply V_{DD} and a backup battery is connected. To enter the standby mode, the power management control bits PM[2:0] have to be set logic 111. Then the main power supply V_{DD} must be removed. As a result of it, the PCF8523 enters the standby mode and does not draw any current from the backup battery before it is powered up again from main supply V_{DD}.

8.5.2 Battery switch-over function

The PCF8523 has a backup battery switch-over circuit. It monitors the main power supply V_{DD} and switches automatically to the backup battery when a power failure condition is detected.

One of two operation modes can be selected:

- **Standard mode:** the power failure condition happens when: $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$
- **Direct switching mode:** the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V.

Generation of interrupts from the battery switch-over is controlled via the BSIE bit (see register Control_2). If BSIE is enabled, the $\overline{INT1}$ follows the status of bit BLF (register Control_3). Clearing BLF immediately clears $\overline{INT1}$.

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BSF (register Control_3) is set logic 1
2. An interrupt is generated if the control bit BSIE (register Control_3) is enabled

The battery switch flag BSF can be cleared by using the interface after the power supply has switched to V_{DD}. It must be cleared to clear the interrupt.

The interface is disabled in battery backup operation:

- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

8.5.2.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$, the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$, the internal power supply is V_{BAT}.

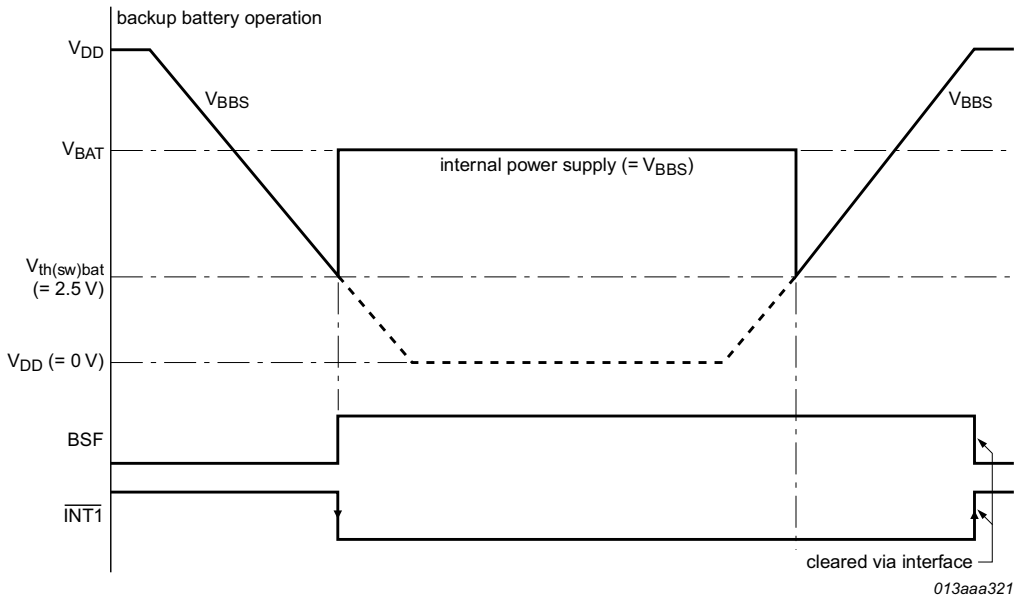


Fig 9. Battery switch-over behavior in standard mode and with bit BSIE set logic 1 (enabled)

8.5.2.2 Direct switching mode

If $V_{DD} > V_{BAT}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ the internal power supply is V_{BAT}.

The direct switching mode is useful in systems where V_{DD} is higher than V_{BAT} at all times (for example, V_{DD} = 5 V, V_{BAT} = 3.5 V). If the V_{DD} and V_{BAT} values are similar (for example, V_{DD} = 3.3 V, $V_{BAT} \geq 3.0$ V), the direct switching mode is not recommended. In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

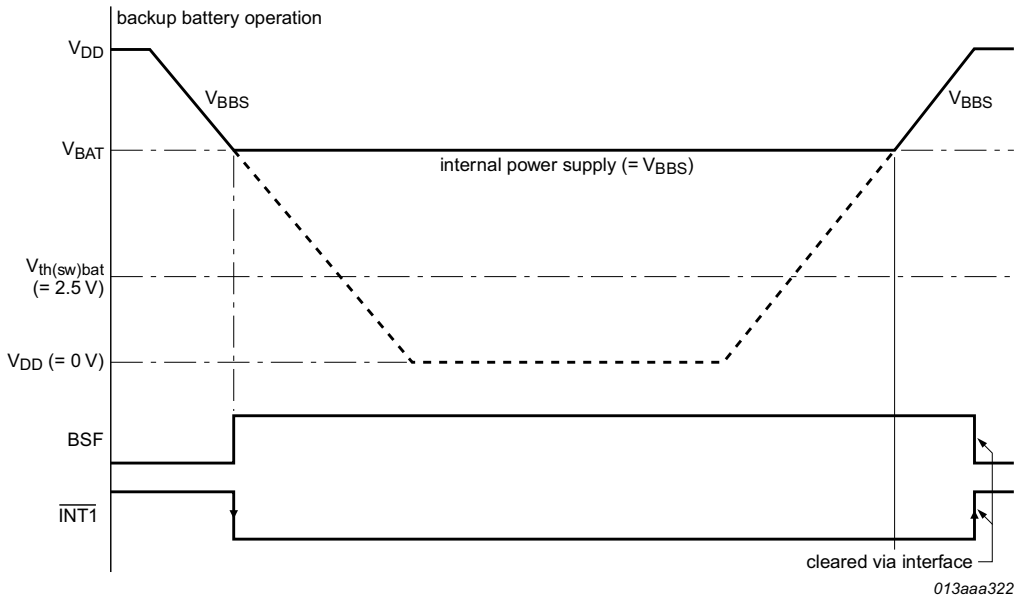


Fig 10. Battery switch-over behavior in direct switching mode and with bit BSIE set logic 1 (enabled)

8.5.2.3 Battery switch-over disabled, only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to V_{DD}
- The battery flag (BSF) is always logic 0

8.5.3 Battery low detection function

The PCF8523 has a battery low detection circuit, which monitors the status of the battery V_{BAT}.

Generation of interrupts from the battery low detection is controlled via bit BLIE (register Control_3). If BLIE is enabled, the $\overline{INT1}$ follows the status of bit BLF (register Control_3).

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typically 2.5 V), the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery does not ensure data integrity during periods of backup battery operation.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 11):

1. The battery low flag BLF is set logic 1
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled. The interrupt remains active until the battery is replaced (BLF set logic 0) or when bit BLIE is disabled (BLIE set logic 0)
3. The flag BLF (register Control_3) remains logic 1 until the battery is replaced. BLF cannot be cleared using the interface. It is cleared automatically by the battery low detection circuit when the battery is replaced

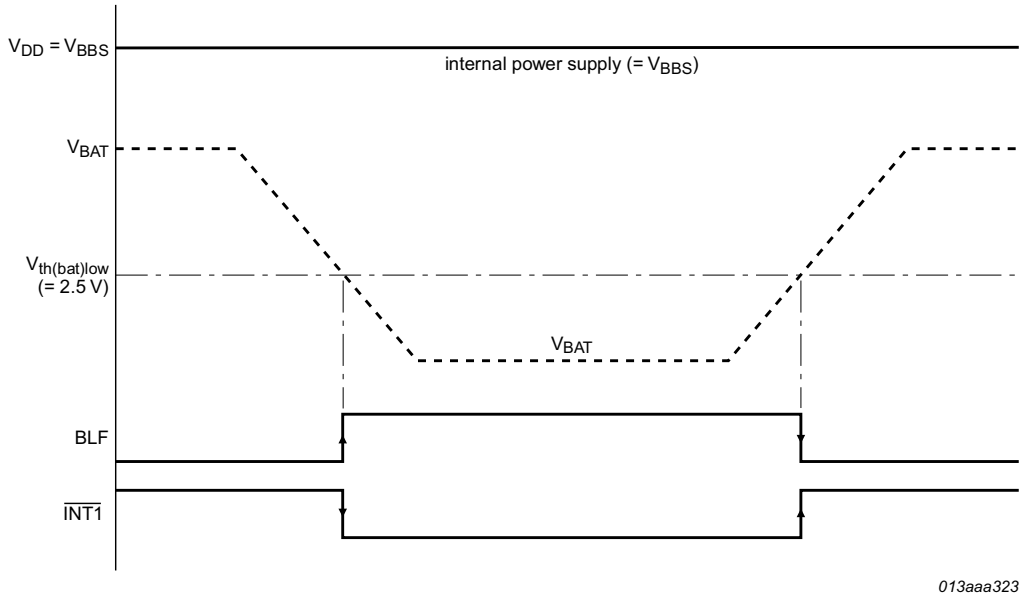


Fig 11. Battery low detection behavior with bit BLIE set logic 1 (enabled)

8.6 Time and date registers

Most of these registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for the array SECONDS in Table 13.

8.6.1 Register Seconds

Table 12. Seconds - seconds and clock integrity status register (address 03h) bit description

Bit	Symbol	Value	Place value	Description
7	OS	0	-	clock integrity is guaranteed
		1[1]	-	clock integrity is not guaranteed; oscillator has stopped or been interrupted
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	

[1] Start-up value.

Table 13. SECONDS coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit			Bit			
	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.6.1.1 Oscillator STOP flag

The OS flag is set whenever the oscillator is stopped (see Figure 12). The flag remains set until cleared by using the interface. When the oscillator is not running, then the OS flag cannot be cleared. This method can be used to monitor the oscillator.

The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in a range of 200 ms to 2 s, depending on crystal type, temperature, and supply voltage. At power-on, the OS flag is always set.

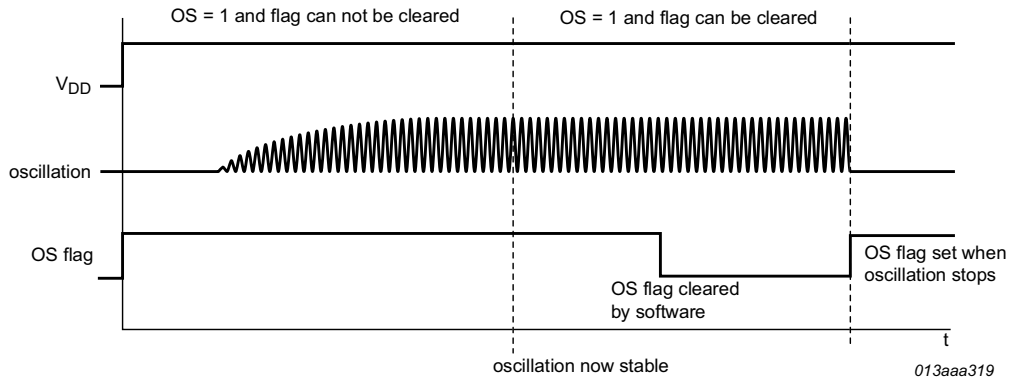


Fig 12. OS flag

8.6.2 Register Minutes

Table 14. Minutes - minutes register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

8.6.3 Register Hours

Table 15. Hours - hours register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12 hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOURS	0 to 1	ten's place	actual hours in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 hour mode[1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours in 24 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Hour mode is set by bit 12_24 in register Control_1 (see Table 7).

8.6.4 Register Days

Table 16. Days - days register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] If the year counter contains a value, which is exactly divisible by 4 (including the year 00), the PCF8523 compensates for leap years by adding a 29th day to February.

8.6.5 Register Weekdays

Table 17. Weekdays - weekdays register (address 07h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday, values see Table 18

Table 18. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be reassigned by the user.

8.6.6 Register Months

Table 19. Months - months register (address 08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format; assignments see Table 20
3 to 0		0 to 9	unit place	

Table 20. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit	Bit			
	4	3	2	1	0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.6.7 Register Years

Table 21. Years - years register (09h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

8.6.8 Data flow of the time function

Figure 13 shows the data flow and data dependencies starting from the 1 Hz clock tick.

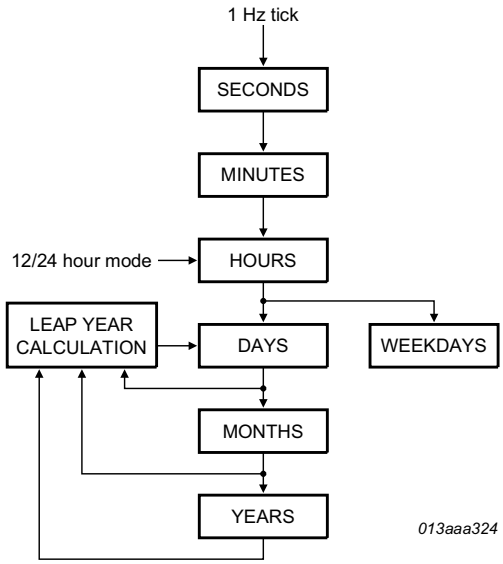


Fig 13. Data flow diagram of the time function

During read/write operations, the time counting circuits (memory locations 03h through 09h) are blocked.

The blocking prevents:

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After the read/write-access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of one request can be stored; therefore, all accesses must be completed within 1 second (see Figure 14).

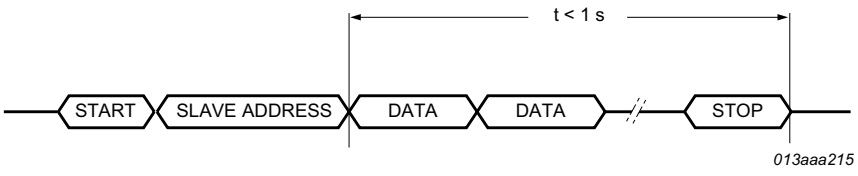


Fig 14. Access time for read/write operations

Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A rollover may occur between reads thus giving the minutes from one moment and the hours from the next.

8.7 Alarm registers

The registers at addresses 0Ah through 0Dh contain the alarm information.

8.7.1 Register Minute_alarm

Table 22. Minute_alarm - minute alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.7.2 Register Hour_alarm

Table 23. Hour_alarm - hour alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_H	0	-	hour alarm is enabled
		1[1]	-	hour alarm is disabled
6	-	-	-	unused
12 hour mode[2]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_ALARM	0 to 1	ten's place	hour alarm information in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 hour mode[2]				
5 to 4	HOURS	0 to 2	ten's place	hour alarm information in 24 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

[2] Hour mode is set by bit 12_24 in register Control_1 (see Table 7).

8.7.3 Register Day_alarm

Table 24. Day_alarm - day alarm register (address 0Ch) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

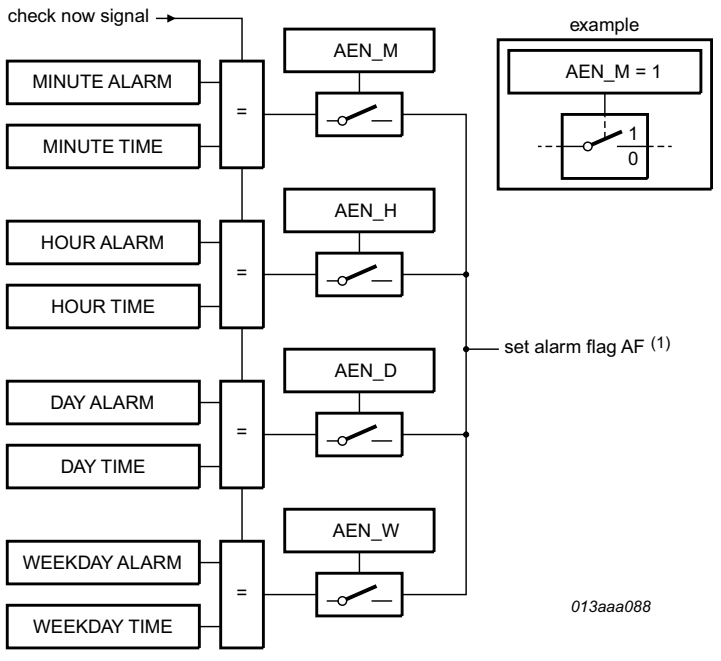
8.7.4 Register Weekday_alarm

Table 25. Weekday_alarm - weekday alarm register (address 0Dh) bit description

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information

[1] Default value.

8.7.5 Alarm flag



(1) Only when all enabled alarm settings are matching.
It is only on increment to a matched case that the alarm flag is set, see Section 8.7.5.

Fig 15. Alarm function block diagram