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PCF85263A

Tiny Real-Time Clock/calendar with alarm function, battery switch-over, time stamp input, and I²C-bus

Rev. 4.1 — 27 November 2015 Product data sheet

1. General description

The PCF85263A is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power consumption and with automatic switching to battery on main power loss. The RTC can also be configured as a stop-watch (elapsed time counter). Three time log registers triggered from battery switch-over as well as input driven events. Featuring clock output and two independent interrupt signals, two alarms, I²C interface and quartz crystal calibration.

For a selection of NXP Real-Time Clocks, see Table 72 on page 90

2. Features and benefits

- UL Recognized Component (PCF85263ATL)
- Provides year, month, day, weekday, hours, minutes, seconds and 100th seconds based on a 32.768 kHz quartz crystal
- Stop-watch mode for elapsed time counting. From 100th seconds to 999999 hours
- Two independent alarms
- Battery back-up circuit
- WatchDog timer
- Three timestamp registers
- Two independent interrupt generators plus predefined interrupts at every second, minute, or hour
- Frequency adjustment via programmable offset register
- Clock operating voltage: 0.9 V to 5.5 V
- Low current; typical 0.28 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 400 kHz two-line I²C-bus interface (at V_{DD} = 1.8 V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz, and 1 Hz)
- Configurable oscillator circuit for a wide variety of quartzes: C_L = 6 pF, C_L = 7 pF, and C_L = 12.5 pF

3. Applications

- Printers and copiers
- Electronic metering
- Digital cameras

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 24.

- White goods
- Elapsed time counter
- Network powered devices
- Battery backed up systems
- Data loggers
- Digital voice recorders
- Mobile equipment
- Accurate high duration timer

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF85263AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCF85263ATL	DFN2626-10	plastic thermal enhanced extremely thin small outline package; no leads; 10 terminals; body 2.6 × 2.6 × 0.5 mm	SOT1197-1
PCF85263ATT	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCF85263ATT1	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1

4.1 Ordering options

Table 2. Ordering options

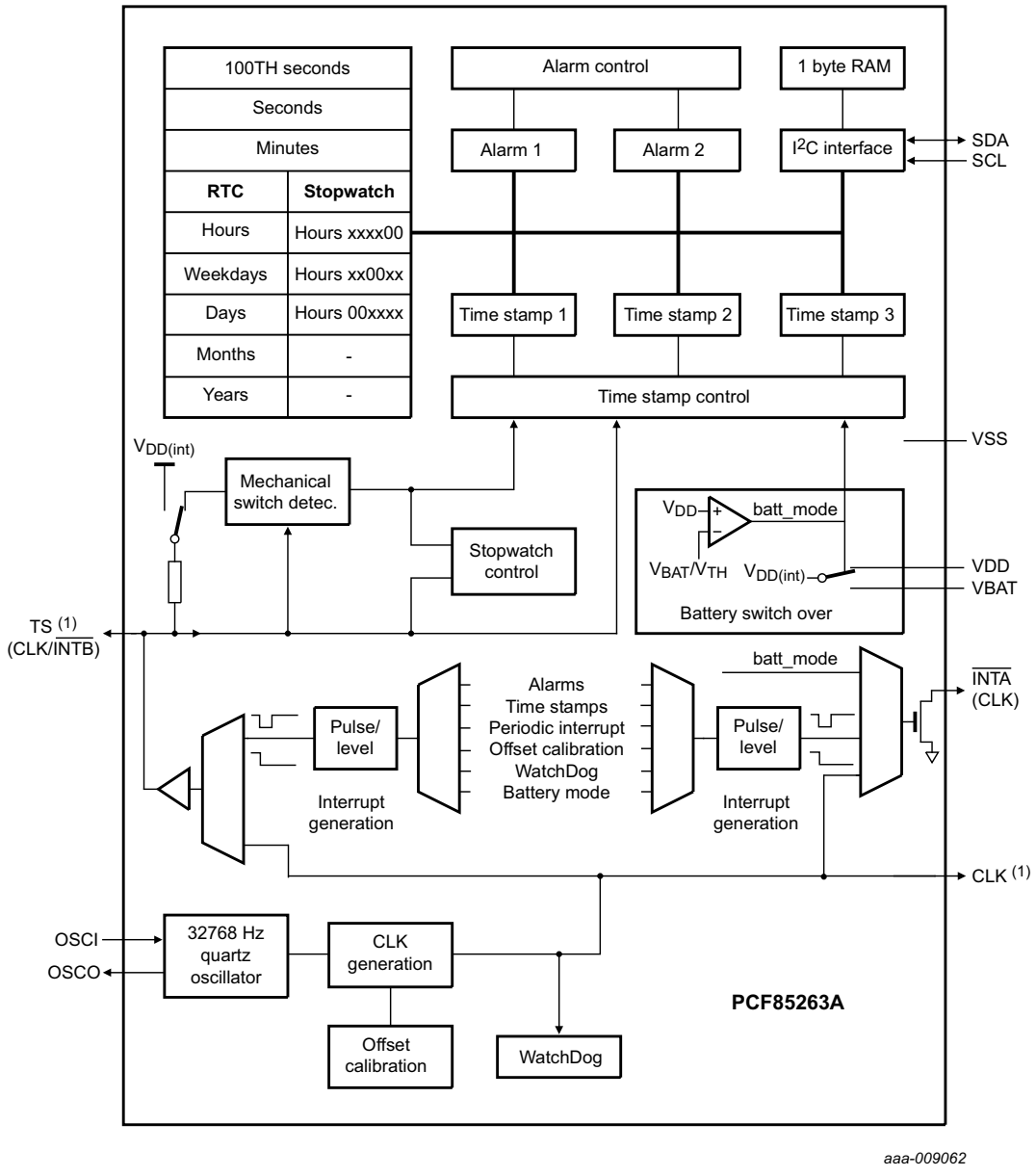
Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF85263AT/A	PCF85263AT/AJ	935302207118	tape and reel, 13 inch	1
PCF85263ATL/A	PCF85263ATL/AX	935302602115	tape and reel, 7 inch	1
PCF85263ATT/A	PCF85263ATT/AJ	935304459118	tape and reel, 13 inch	1
PCF85263ATT1/A	PCF85263ATT1/AJ	935304461118	tape and reel, 13 inch	1

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCF85263AT/A	85263A
PCF85263ATL/A	263A
PCF85263ATT/A	263A
PCF85263ATT1/A	263A

6. Block diagram

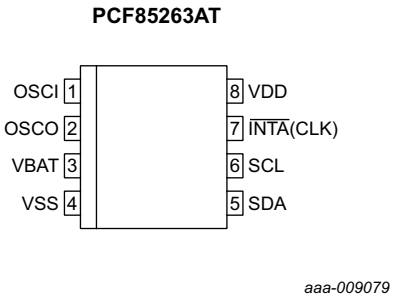


(1) Not available on all package types.

Fig 1. Block diagram of PCF85263A

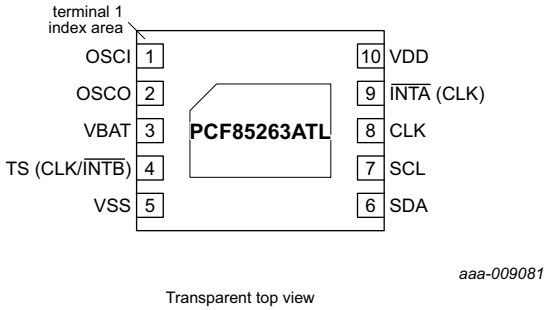
7. Pinning information

7.1 Pinning



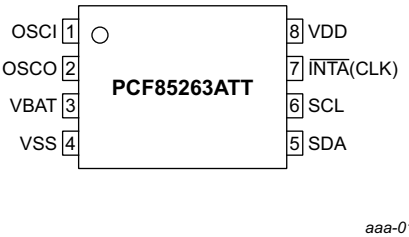
For mechanical details, see Figure 44 on page 79.

Fig 2. Pin configuration for PCF85263AT (SO8)



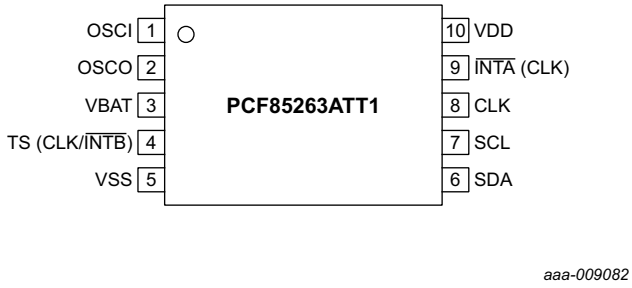
For mechanical details, see Figure 45 on page 80.

Fig 3. Pin configuration for PCF85263ATL (DFN2626-10)



For mechanical details, see Figure 46 on page 81.

Fig 4. Pin configuration for PCF85263ATT (TSSOP8)



For mechanical details, see Figure 47 on page 82.

Fig 5. Pin configuration for PCF85263ATT1 (TSSOP10)

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin				Type	Description	
	PCF85263AT (SO8)	PCF85263ATL (DFN2626-10)	PCF85263ATT (TSSOP8)	PCF85263ATT1 (TSSOP10)		Primary use	Secondary use
OSCI	1	1	1	1	input	oscillator input	-
OSCO	2	2	2	2	output	oscillator output	-
VBAT	3	3	3	3	supply	battery backup supply voltage[1]	-
TS (CLK/$\overline{\text{INTB}}$)	-	4	-	4	input/ output	can be configured with TSPM[1:0][2]	
						timestamp input	$\overline{\text{INTB}}$ and CLK output (push-pull); stop-watch control
VSS	4	5[3]	4	5	supply	ground supply voltage	-
SDA	5	6	5	6	input/ output	serial data line	-
SCL	6	7	6	7	input	serial clock input	-
CLK	-	8	-	8	output	CLK (push-pull)	-
$\overline{\text{INTA}}$ (CLK)	7	9	7	9	output	can be configured with INTAPM[1:0][4]	
						interrupt output (open-drain)	CLK output (open-drain)
VDD	8	10	8	10	supply	supply voltage	-

[1] Connect to V_{DD} if not used.

[2] See Table 7 and Table 47.

[3] The die paddle (exposed pad) is connected to V_{SS} through high ohmic (non-conductive) silicon attach and should be electrically isolated. It is good engineering practice to solder the exposed pad to an electrically isolated PCB copper pad as shown in Figure 45 “Package outline SOT1197-1 (DFN2626-10), PCF85263ATL” for better heat transfer but it is not required as the RTC doesn’t consume much power. In no case should traces be run under the package exposed pad.

[4] See Table 7 and Table 49.

8. Functional description

The PCF85263A contains 8-bit registers for time information, for timestamp information and registers for system configuration. Included is an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calender, and an I²C-bus interface with a maximum data rate of 400 kbit/s.

The built-in address register will increment automatically after each read or write of a data byte. After register 2Fh, the auto-incrementing will wrap around to address 00h (see Figure 6).

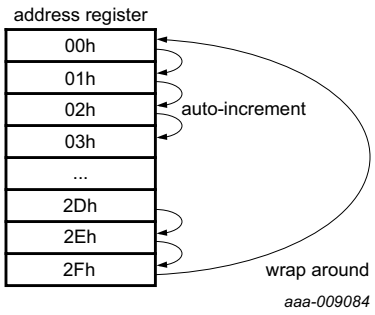


Fig 6. Address register incrementing

All registers (see Table 5 on page 9, Table 6 on page 11, and Table 7 on page 13) are designed as addressable 8-bit parallel registers although not all bits are implemented. Figure 7 gives an overview of the address map.

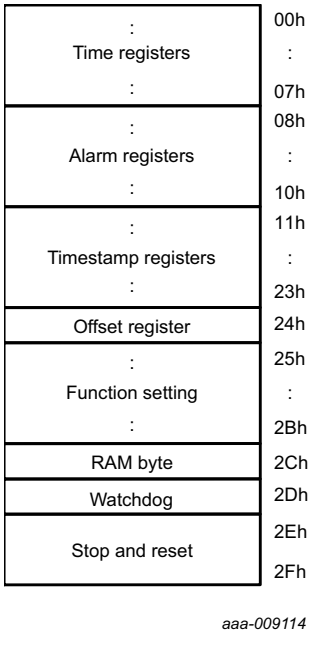


Fig 7. Register map

The 100th seconds, seconds, minutes, hours, days, months, and years as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is read, the contents of all time counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.

8.1 Registers organization overview

8.1.1 Time mode registers

The PCF85263A has two time mode register sets, one for the real-time clock mode and one for the stopwatch clock mode. The access to these registers can be switched by the RTCM bit in the Function control register (28h), see Table 7 on page 13 and Table 54 on page 55.

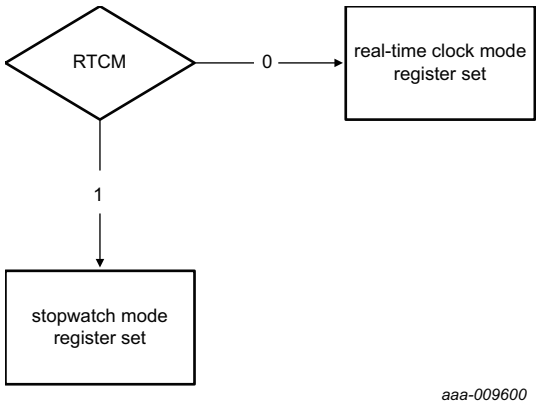


Fig 8. Time mode register set selection

8.1.1.1 RTC mode time registers overview (RTCM = 0)

Table 5. RTC mode time registers

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 59.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
RTC time and date registers										
00h	100th_seconds	100TH_SECONDS (0 to 99)								Section 8.2
01h	Seconds	OS	SECONDS (0 to 59)							
02h	Minutes	EMON	MINUTES (0 to 59)							
03h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 hour mode					
				HOURS (0 to 23) in 24 hour mode						
04h	Days	-	-	DAYS (1 to 31)						
05h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			
06h	Months	-	-	-	MONTHS (1 to 12)					
07h	Years	YEARS (0 to 99)								
RTC alarm1										
08h	Second_alarm1	-	SEC_ALARM1 (0 to 59)							Section 8.4
09h	Minute_alarm1	-	MIN_ALARM1 (0 to 59)							
0Ah	Hour_alarm1	-	-	AMPM	HR_ALARM1 (1 to 12) in 12 hour mode					
				HR_ALARM1 (0 to 23) in 24 hour mode						
0Bh	Day_alarm1	-	-	DAY_ALARM1 (1 to 31)						
0Ch	Month_alarm1	-	-	-	MON_ALARM1 (1 to 12)					
RTC alarm2										
0Dh	Minute_alarm2	-	MIN_ALARM2 (0 to 59)							Section 8.4
0Eh	Hour_alarm2	-	-	AMPM	HR_ALARM2 (1 to 12) in 12 hour mode					
0Fh	Weekday_alarm 2	-	-	-	-	-	WDAY_ALARM2 (0 to 6)			
RTC alarm enables										
10h	Alarm_enables	WDAY_A2E	HR_A2E	MIN_A2E	MON_A1E	DAY_A1E	HR_A1E	MIN__A1E	SEC__A1E	Section 8.4

Table 5. RTC mode time registers *...continued*

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 59.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
RTC timestamp1 (TSR1)										
11h	TSR1_seconds	-	TSR1_SECONDS (0 to 59)							Section 8.7
12h	TSR1_minutes	-	TSR1_MINUTES (0 to 59)							
13h	TSR1_hours	-	-	AMPM	TSR1_HOURS (1 to 12) in 12 hour mode					
				TSR1_HOURS (0 to 23) in 24 hour mode						
14h	TSR1_days	-	-	TSR1_DAYS (1 to 31)						
15h	TSR1_months	-	-	-	TSR1_MONTHS (1 to 12)					
16h	TSR1_years	TSR1_YEARS (0 to 99)								
RTC timestamp2 (TSR2)										
17h	TSR2_seconds	-	TSR2_SECONDS (0 to 59)							Section 8.7
18h	TSR2_minutes	-	TSR2_MINUTES (0 to 59)							
19h	TSR2_hours	-	-	AMPM	TSR2_HOURS (1 to 12) in 12 hour mode					
				TSR2_HOURS (0 to 23) in 24 hour mode						
1Ah	TSR2_days	-	-	TSR2_DAYS (1 to 31)						
1Bh	TSR2_months	-	-	-	TSR2_MONTHS (1 to 12)					
1Ch	TSR2_years	TSR2_YEARS (0 to 99)								
RTC timestamp3 (TSR3)										
1Dh	TSR3_seconds	-	TSR3_SECONDS (0 to 59)							Section 8.7
1Eh	TSR3_minutes	-	TSR3_MINUTES (0 to 59)							
1Fh	TSR3_hours	-	-	AMPM	TSR3_HOURS (1 to 12) in 12 hour mode					
				TSR3_HOURS (0 to 23) in 24 hour mode						
20h	TSR3_days	-	-	TSR3_DAYS (1 to 31)						
21h	TSR3_months	-	-	-	TSR3_MONTHS (1 to 12)					
22h	TSR3_years	TSR3_YEARS (0 to 99)								
RTC timestamp mode control										
23h	TSR_mode	TSR3M[1:0]		-	TSR2M[2:0]			TSR1M[1:0]		Section 8.7

8.1.1.2 Stop-watch mode time registers (RTCM = 1)

Table 6. Stop-watch mode time registers

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 59.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Stop-watch time registers										
00h	100th_seconds	100TH_SECONDS (0 to 99)								Section 8.3
01h	Seconds	OS	SECONDS (0 to 59)							
02h	Minutes	EMON	MINUTES (0 to 59)							
03h	Hours_xx_xx_00	HR_XX_XX_00 (0 to 99)								
04h	Hours_xx_00_xx	HR_XX_00_XX (0 to 99)								
05h	Hours_00_xx_xx	HR_00_XX_XX (0 to 99)								
06h	not used	-	-	-	-	-	-	-	-	
07h	not used	-	-	-	-	-	-	-	-	
Stop-watch alarm1										
08h	Second_alm1	-	SEC_ALM1 (0 to 59)							Section 8.4
09h	Minute_alm1	-	MIN_ALM1 (0 to 59)							
0Ah	Hr_xx_xx_00_alm1	HR_XX_XX_00_ALM1 (0 to 99)								
0Bh	Hr_xx_00_xx_alm1	HR_XX_00_XX_ALM1 (0 to 99)								
0Ch	Hr_00_xx_xx_alm1	HR_00_XX_XX_ALM1 (0 to 99)								
Stop-watch alarm2										
0Dh	Minute_alm2	-	MIN_ALM2 (0 to 59)							Section 8.4
0Eh	Hr_xx_00_alm2	HR_XX_00_ALM2 (0 to 99)								
0Fh	Hr_00_xx_alm2	HR_00_XX_ALM2 (0 to 99)								
Stop-watch alarm enables										
10h	Alarm_enables	HR_00_XX_A2E	HR_XX_00_A2E	MIN_A2E	HR_00_XX_XX_A1E	HR_XX_00_XX_A1E	HR_XX_XX_00_A1E	MIN_A1E	SEC_A1E	Section 8.4

Table 6. Stop-watch mode time registers *…continued*

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 59. …continued

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Stop-watch timestamp1 (TSR1)										
11h	TSR1_seconds	-	TSR1_SECONDS (0 to 59)							Section 8.7
12h	TSR1_minutes	-	TSR1_MINUTES (0 to 59)							
13h	TSR1_hr_xx_xx_00	TSR1_HR_XX_XX_00 (0 to 99)								
14h	TSR1_hr_xx_00_xx	TSR1_HR_XX_00_XX (0 to 99)								
15h	TSR1_hr_00_xx_xx	TSR1_HR_00_XX_XX (0 to 99)								
16h	not used	-	-	-	-	-	-	-	-	
Stop-watch timestamp2 (TSR2)										
17h	TSR2_seconds	-	TSR2_SECONDS (0 to 59)							Section 8.7
18h	TSR2_minutes	-	TSR2_MINUTES (0 to 59)							
19h	TSR2_hr_xx_xx_00	TSR2_HR_XX_XX_00 (0 to 99)								
1Ah	TSR2_hr_xx_00_xx	TSR2_HR_XX_00_XX (0 to 99)								
1Bh	TSR2_hr_00_xx_xx	TSR2_HR_00_XX_XX (0 to 99)								
1Ch	not used	-	-	-	-	-	-	-	-	
Stop-watch timestamp3 (TSR3)										
1Dh	TSR3_seconds	-	TSR3_SECONDS (0 to 59)							Section 8.7
1Eh	TSR3_minutes	-	TSR3_MINUTES (0 to 59)							
1Fh	TSR3_hr_xx_xx_00	TSR3_HR_XX_XX_00 (0 to 99)								
20h	TSR3_hr_xx_00_xx	TSR3_HR_XX_00_XX (0 to 99)								
21h	TSR3_hr_00_xx_xx	TSR3_HR_00_XX_XX (0 to 99)								
22h	not used	-	-	-	-	-	-	-	-	
Stop-watch timestamp mode control										
23h	TSR_mode	TSR3M[1:0]		-	TSR2M[2:0]			TSR1M[1:0]		Section 8.7

8.1.2 Control registers overview

Table 7. Control and function registers overview

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 59.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Offset register										
24h	Offset	OFFSET[7:0]								Section 8.8
Control registers										
25h	Oscillator	CLKIV	OFFM	12_24	LOWJ	OSCD[1:0]		CL[1:0]		Section 8.10
26h	Battery_switch	-	-	-	BSOFF	BSRR	BSM[1:0]		BSTH	Section 8.11
27h	Pin_IO	CLKPM	TSPULL	TSL	TSIM	TSPM[1:0]		INTAPM[1:0]		Section 8.12
28h	Function	100TH	PI[1:0]		RTCM	STOPM	COF[2:0]			Section 8.13
29h	INTA_enable	ILPA	PIEA	OIEA	A1IEA	A2IEA	TSRIEA	BSIEA	WDIEA	Section 8.9
2Ah	INTB_enable	ILPB	PIEB	OIEB	A1IEB	A2IEB	TSRIEB	BSIEB	WDIEB	Section 8.9
2Bh	Flags	PIF	A2F	A1F	WDF	BSF	TSR3F	TSR2F	TSR1F	Section 8.14
RAM byte										
2Ch	RAM_byte	B[7:0]								Section 8.6
WatchDog registers										
2Dh	WatchDog	WDM	WDR[4:0]					WDS[1:0]		Section 8.5
Stop										
2Eh	Stop_enable	-	-	-	-	-	-	-	STOP	Section 8.16
Reset										
2Fh	Resets	CPR	0	1	0	SR	1	0	CTS	Section 8.15

8.2 RTC mode time and date registers

RTC mode is enabled by setting RTCM = 0. These registers are coded in the BCD format to simplify application use.

Default state is:

Time — 00:00:00.00

Date — 2000 01 01

Weekday — Saturday

Monitor bits — OS = 1, EMON = 0

Table 8. Time and date registers in RTC mode (RTCM = 0)

Bit positions labeled as - are not implemented and return 0 when read.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	100th_seconds[1]	0 to 9				0 to 9			
01h	Seconds	OS	0 to 5			0 to 9			
02h	Minutes	EMON	0 to 5			0 to 9			
03h	Hours[2]	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
04h	Days[3]	-	-	0 to 3		0 to 9			
05h	Weekdays	-	-	-	-	-	0 to 6		
06h	Months	-	-	-	0 to 1	0 to 9			
07h	Years	0 to 9				0 to 9			

[1] The 100th_seconds register is only available when the 100TH mode is enabled, see Section 8.13.1. When the 100TH mode is disabled, this register always returns 0.

[2] Hour mode is set by the 12_24 bit in the Oscillator register, see Section 8.10 on page 42.

[3] If the year counter contains a value, which is exactly divisible by 4, the PCF85263A compensates for leap years by adding a 29th day to February.

8.2.1 Definition of BCD

The Binary-Coded Decimal (BCD) is an encoding of numbers where each digit is represented by a separate bit field. Each bit field may only contain the values 0 to 9. In this way, decimal numbers and counting is implemented.

Example: 59 encoded as an entire number is represented by 3Bh or 111011. In BCD the 5 is represented as 5h or 0101 and the 9 as 9h or 1001 which combines to 59h.

Table 9. BCD coding

Value in decimal	Upper-digit (ten's place)				Digit (unit place)			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	1	0	0	0	1
02	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	1	0	0	1	1	0	0	1
10	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
98	1	0	0	1	1	0	0	0
99	1	0	0	1	1	0	0	1

8.2.2 OS: Oscillator stop

When the oscillator of the PCF85263A is stopped, the OS status bit is set. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature, and supply voltage.

The status bit remains set until cleared by command (see Figure 9). If the bit cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

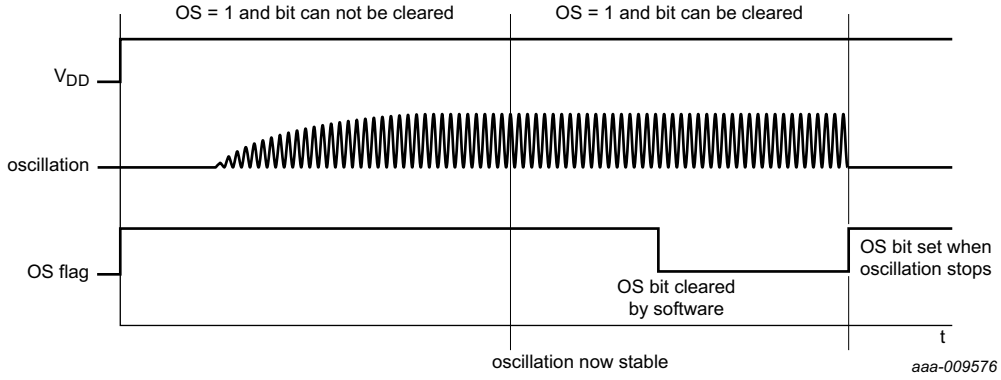


Fig 9. OS status bit

8.2.3 EMON: event monitor

The EMON can be used to monitor the status of all the flags in the Flags register, see Section 8.14 on page 57. When one or more of the flags is set, then the EMON bit returns a logic 1. The EMON bit cannot be cleared. EMON returns a logic 0 when all flags are cleared.

See Figure 22 on page 41 for a pictorial representation.

8.2.4 Definition of weekdays

Definition may be reassigned by the user.

Table 10. Weekday assignments

Day	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

8.2.5 Definition of months

Table 11. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.2.6 Setting and reading the time in RTC mode

Figure 10 shows the data flow and data dependencies starting from the 100 Hz clock tick.

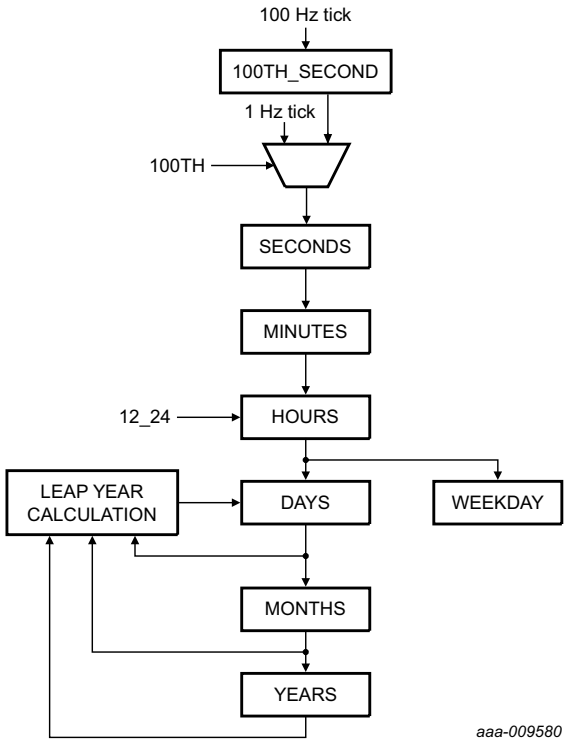


Fig 10. Data flow for the time function

During read operations, the time counting circuits (memory locations 00h through 07h) are copied into an output register. The RTC continues counting in the background.

When reading or writing the time it is very important to make a read or write access in one go, that is, setting or reading 100th seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time increments between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next.

Before setting the time, the STOP bit should be set and the prescalers should be cleared (see Section 8.16 “Stop_enable register” on page 60).

An example of setting the time: 14 hours, 23 minutes and 19 seconds.

- I²C START condition
- I²C slave address + write (A2h)
- register address (2Eh)
- write data (set STOP, 01h)

- write data (clear prescaler, A4h)
- write data (100th seconds, 00h)
- write data (Hours, 14h)
- write data (Minutes, 23h)
- write data (Seconds, 19h)
- I²C START condition
- I²C slave address + write (A2h)
- register address (2Eh)
- write data (clear STOP, 00h). Time starts counting from this point
- I²C STOP condition

8.3 Stop-watch mode time registers

These registers are coded in the BCD format to simplify application use.

Stop-watch mode is enabled by setting RTCM = 1. In stop-watch mode, the PCF85263A counts from 100th seconds to 99999 hours. There are no days, weekdays, months or year registers.

Default state is:

Time — 00000:00:00.00

Monitor bits — OS = 1, EMON = 0 (see Section 8.2.2 on page 15 and Section 8.2.3 on page 15)

Table 12. Time registers in stop-watch mode (RTCM = 1)

Bit positions labeled as - are not implemented and return 0 when read.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	100th_seconds[1]	0 to 9				0 to 9			
01h	Seconds	OS	0 to 5			0 to 9			
02h	Minutes	EMON	0 to 5			0 to 9			
03h	Hours_xx_xx_00	0 to 9				0 to 9			
04h	Hours_xx_00_xx	0 to 9				0 to 9			
05h	Hours_00_xx_xx	0 to 9				0 to 9			
06h	not used	-	-	-	-	-	-	-	-
07h	not used	-	-	-	-	-	-	-	-

[1] The 100th_seconds register is only available when the 100TH mode is enabled, see Section 8.13.1 on page 54. When the 100TH mode is disabled, this register always returns 0.

8.3.1 Setting and reading the time in stop-watch mode

Figure 11 shows the data flow and data dependencies starting from the 100 Hz clock tick.

During read operations, the time counting circuits (memory locations 00h through 07h) are copied into an output register. The RTC continues counting in the background.

When reading or writing the time it is very important to make a read or write access in one go, that is, setting or reading 100th_seconds through to HR_00_xx_xx should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the seconds value is set in one access and then in a following access the minutes value is set, it is possible that the time increments between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the seconds from one moment and the minutes from the next.

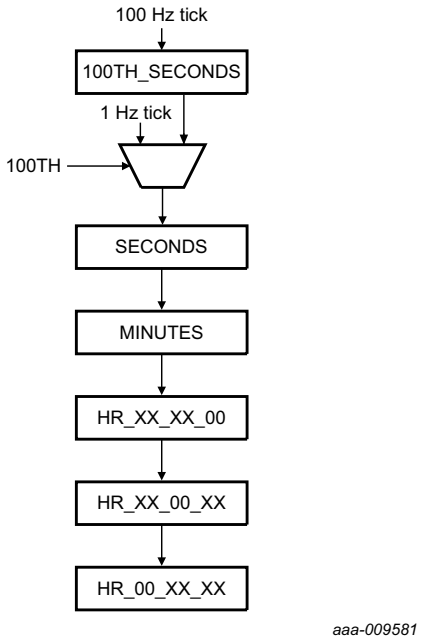


Fig 11. Data flow for the stop-watch function

8.4 Alarms

There are two independent alarms. Each is separately configured and may be used to generate an interrupt. In RTC mode, an alarm is configured for time and date. In stop-watch mode when the RTC is functioning as an elapsed time counter, an alarm is configured for time only.

8.4.1 Alarms in RTC mode

In RTC mode, Alarm 1 can be configured from seconds to months. Alarm 2 operates on minutes, hours and weekday. Each segment of the time is independently enabled. Alarms can be output on the $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ pins.

8.4.1.1 Alarm1 and alarm2 registers in RTC mode

Setting the time for alarm1: Only the information which is relevant for the alarm condition must to be programmed. The unused parts are ignored.

Table 13. Alarm1 and alarm2 registers in RTC mode coded in BCD (RTCM = 0)

Bit positions labeled as - are not implemented.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTC alarm1 registers									
08h	Second_alarm1	-	0 to 5			0 to 9			
09h	Minute_alarm1	-	0 to 5			0 to 9			
0Ah	Hour_alarm1	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
0Bh	Day_alarm1	-	-	0 to 3		0 to 9			
0Ch	Month_alarm1	-	-	-	0 to 1	0 to 9			
RTC alarm2 registers									
0Dh	Minute_alarm2	-	0 to 5			0 to 9			
0Eh	Hour_alarm2	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
0Fh	Weekday_alarm2	-	-	-	-	-	0 to 6		

8.4.1.2 Alarm1 and alarm2 control in RTC mode

Table 14. Alarm_enables- alarm enable control register (address 10h) bit description

Bit	Symbol	Value	Description
RTC alarm2			
7	WDAY_A2E		**weekday alarm2 enable**
		0[1]	disabled
		1	enabled
6	HR_A2E		**hour alarm2 enable**
		0[1]	disabled
		1	enabled
5	MIN_A2E		**minute alarm2 enable**
		0[1]	disabled
		1	enabled
RTC alarm1			
4	MON_A1E		**month alarm1 enable**
		0[1]	disabled
		1	enabled
3	DAY_A1E		**day alarm1 enable**
		0[1]	disabled
		1	enabled
2	HR_A1E		**hour alarm1 enable**
		0[1]	disabled
		1	enabled

Table 14. Alarm_enables- alarm enable control register (address 10h) bit description *…continued*

Bit	Symbol	Value	Description
1	MIN_A1E		**minute alarm1 enable**
		0[1]	disabled
		1	enabled
0	SEC_A1E		**second alarm1 enable**
		0[1]	disabled
		1	enabled

[1] Default value.

8.4.1.3 Alarm1 and alarm2 function in RTC mode

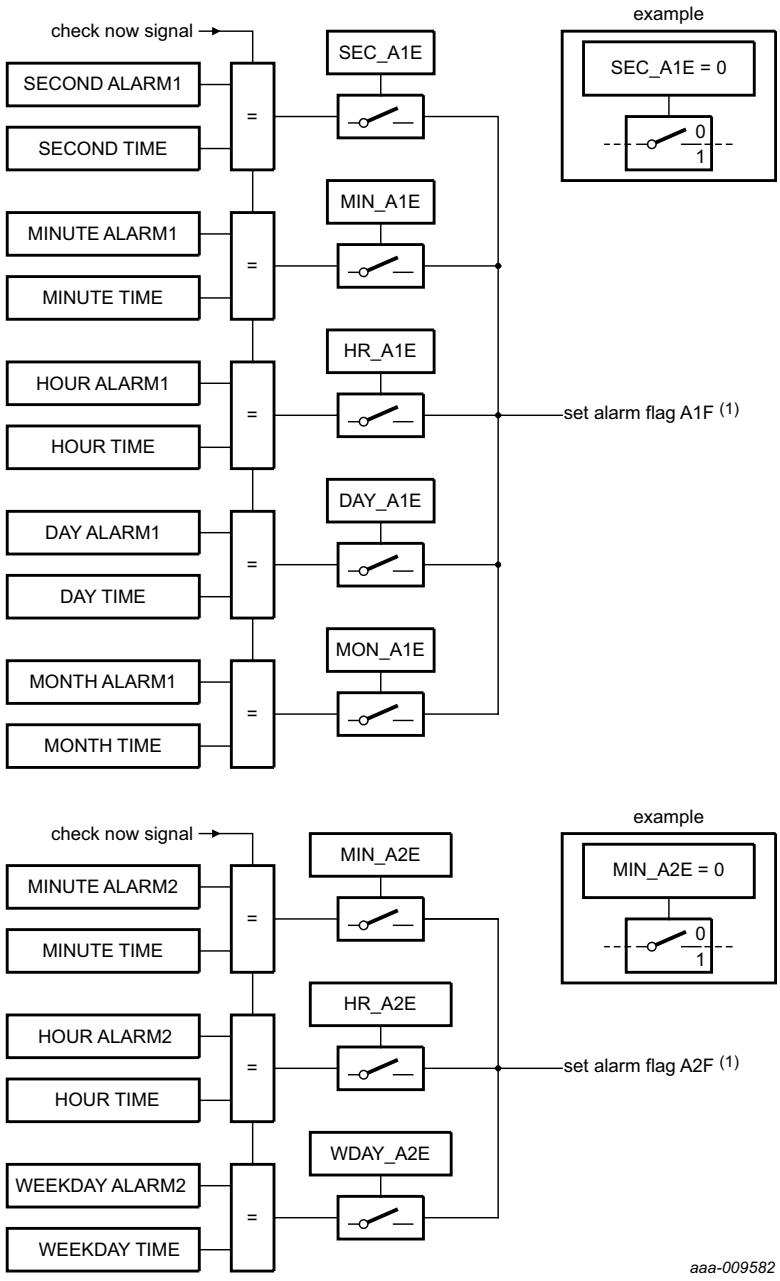
The registers at addresses 08h through 0Ch contain alarm1 information. When one or more of these registers is loaded with second, minute, hour, day, or month, and its corresponding alarm enable bit (SEC_A1E to MON_A1E) is set logic 1, then that information is compared with the current second, minute, hour, day, and month.

The registers at addresses 0Dh through 0Fh contain alarm2 information. When one or more of these registers is loaded with minute, hour or weekday, and its corresponding alarm enable bit (MIN_A2E to WDAY_A2E) is set logic 1, then that information is compared with the current minute, hour and weekday.

Alarm registers which have their alarm enable bit at logic 0 are ignored.

When the time increments to match the enabled alarms, the alarm flag in the Flags register (Section 8.14 on page 57) is set. A1F for alarm1 and A2F for alarm2. The alarm flag is cleared by command.

When the time increments to match the enabled alarms, an interrupt can be generated. See Section 8.4.3 “Alarm interrupts”.



(1) Only when all enabled alarm settings are matching.
The flag is set **only** on increment to a matched case (and not all the time it is equal).

Fig 12. Alarm1 and alarm2 function block diagram (RTC mode)

8.4.2 Alarms in stop-watch mode

In stop-watch mode, Alarm 1 can be configured from seconds to 999999 hours. Alarm 2 operates on minutes up to 9999 hours.

8.4.2.1 Alarm1 and alarm2 registers in stop-watch mode

Setting the time for alarm1 and alarm2: Only the information which is relevant for the alarm condition must to be programmed. The unused parts are ignored.

Table 15. Alarm1 and alarm2 registers in stop-watch mode coded in BCD (RTCM = 1)
Bit positions labeled as - are not implemented.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Stop-watch alarm1 registers									
08h	Second_alm1	-	0 to 5			0 to 9			
09h	Minute_alm1	-	0 to 5			0 to 9			
09h	Hr_xx_xx_00_alm1	0 to 9				0 to 9			
0Bh	Hr_xx_00_xx_alm1	0 to 9				0 to 9			
0Ch	Hr_00_xx_xx_alm1	0 to 9				0 to 9			
Stop-watch alarm2 registers									
0Dh	Minute_alm2	-	0 to 5			0 to 9			
0Eh	Hr_xx_00_alm2	0 to 9				0 to 9			
0Fh	Hr_00_xx_alm2	0 to 9				0 to 9			

8.4.2.2 Alarm1 and alarm2 control in stop-watch mode

Table 16. Alarm_enables- alarm enable control register (address 10h) bit description

Bit	Symbol	Value	Description
Stop-watch alarm2			
7	HR_00_XX_A2E		**thousands of hours alarm2 enable**
		0[1]	disabled
		1	enabled
6	HR_XX_00_A2E		**tens of hours alarm2 enable**
		0[1]	disabled
		1	enabled
5	MIN_A2E		**minute alarm2 enable**
		0[1]	disabled
		1	enabled
Stop-watch alarm1			
4	HR_00_XX_XX_A1E		**100 thousands of hours alarm1 enable**
		0[1]	disabled
		1	enabled
3	HR_XX_00_XX_A1E		**thousands of hours alarm1 enable**
		0[1]	disabled
		1	enabled

Table 16. Alarm_enables- alarm enable control register (address 10h) bit description *…continued*

Bit	Symbol	Value	Description
2	HR_XX_XX_00_A1E		**tens of hour alarm1 enable**
		0[1]	disabled
		1	enabled
1	MIN_A1E		**minute alarm1 enable**
		0[1]	disabled
		1	enabled
0	SEC_A1E		**second alarm1 enable**
		0[1]	disabled
		1	enabled

[1] Default value.

8.4.2.3 Alarm1 and alarm2 function in stop-watch mode

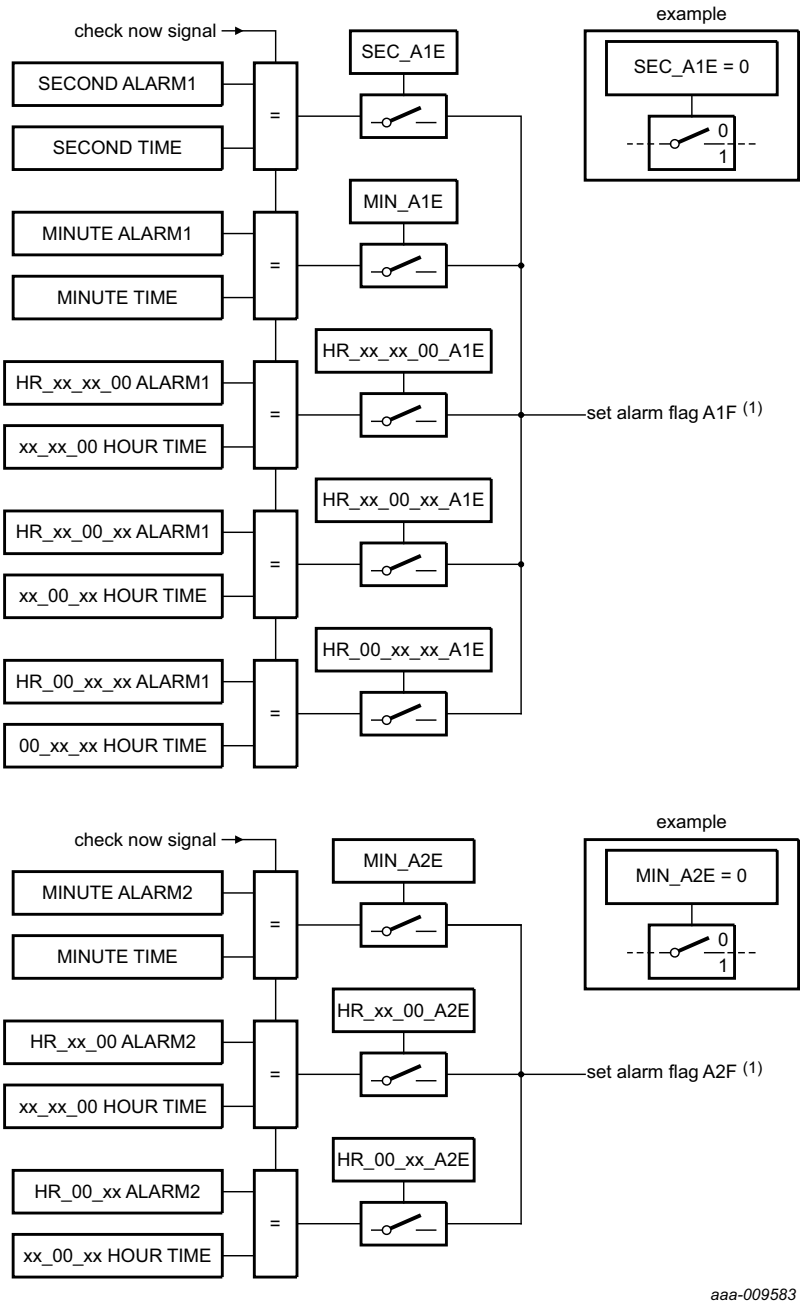
The registers at addresses 08h through 0Ch contain alarm1 information. When one or more of these registers is loaded with second, minute, and hours, and its corresponding alarm enable bit (SEC_A1E to HR_00_XX_XX_A1E) is set logic 1, then that information is compared with the current second, minute, and hours.

The registers at addresses 0Dh through 0Fh contain alarm2 information. When one or more of these registers is loaded with minute and hours, and its corresponding alarm enable bit (MIN_A2E to HR_00_XX_A2E) is set logic 1, then that information is compared with the current minute and hours.

Alarm registers which have their alarm enable bit at logic 0 are ignored.

When the time increments to match the enabled alarms, the alarm flag in the Flags register (Section 8.14 on page 57) is set. A1F for alarm1 and A2F for alarm2. The alarm flag is cleared by command.

When the time increments to match the enabled alarms, an interrupt can be generated. See Section 8.4.3 “Alarm interrupts”.



(1) Only when all enabled alarm settings are matching.
The flag is set **only** on increment to a matched case (and not all the time it is equal).

Fig 13. Alarm1 and alarm2 function block diagram (stop-watch mode)

8.4.3 Alarm interrupts

The generation of interrupts from the alarm functions is controlled via the alarm interrupt enable bits; A1IEA, A1IEB, A2IEA, A2IEB. These bits are in registers INTA_enable (address 29h) and INTB_enable (address 2Ah).