PCF8533

Universal LCD driver for low multiplex rates

Rev. 6 — 1 October 2012 | Product data sheet

1. General description

The PCF8533 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segments and can easily be cascaded for larger LCD applications. The PCF8533 is compatible with most microcontrollers and communicates via the two-line bidirectional I^{2}C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

2. Features and benefits

- Single-chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Internal LCD bias generation with voltage follower buffers
- 80 segment outputs allowing to drive:
    - 40 7-segment alphanumeric characters
    - 20 14-segment alphanumeric characters
    - Any graphics of up to 320 elements
- 80 × 4 bit RAM for display data storage
- Auto-incremental display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs up to 6.5 V for high threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^{2}C-bus interface
- May be cascaded for large LCD applications (up to 5120 elements possible)
- No external components required
- Compatible with Chip-On-Glass (COG) technology
- Manufactured using silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 17.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8533U/2/F2	bare die	99 bumps; 5.28 x 1.4 x 0.38 mm	PCF8533-2

3.1 Ordering options

Table 2. Ordering options

Type number	IC revision	Sales item (12NC)	Delivery form
PCF8533U/2/F2[2]	2	935262345026	chip with hard bumps in tray

[1] Bump hardness see Table 26.

[2] Not to be used for new designs. Replacement part PCF85133U/2DA/1 for industrial parts and PCA85133U/2DA/Q1 for automotive parts.

4. Marking

Table 3. Marking codes

Type number	Marking code
PCF8533U/2/F2	PC8533-2

5. Block diagram

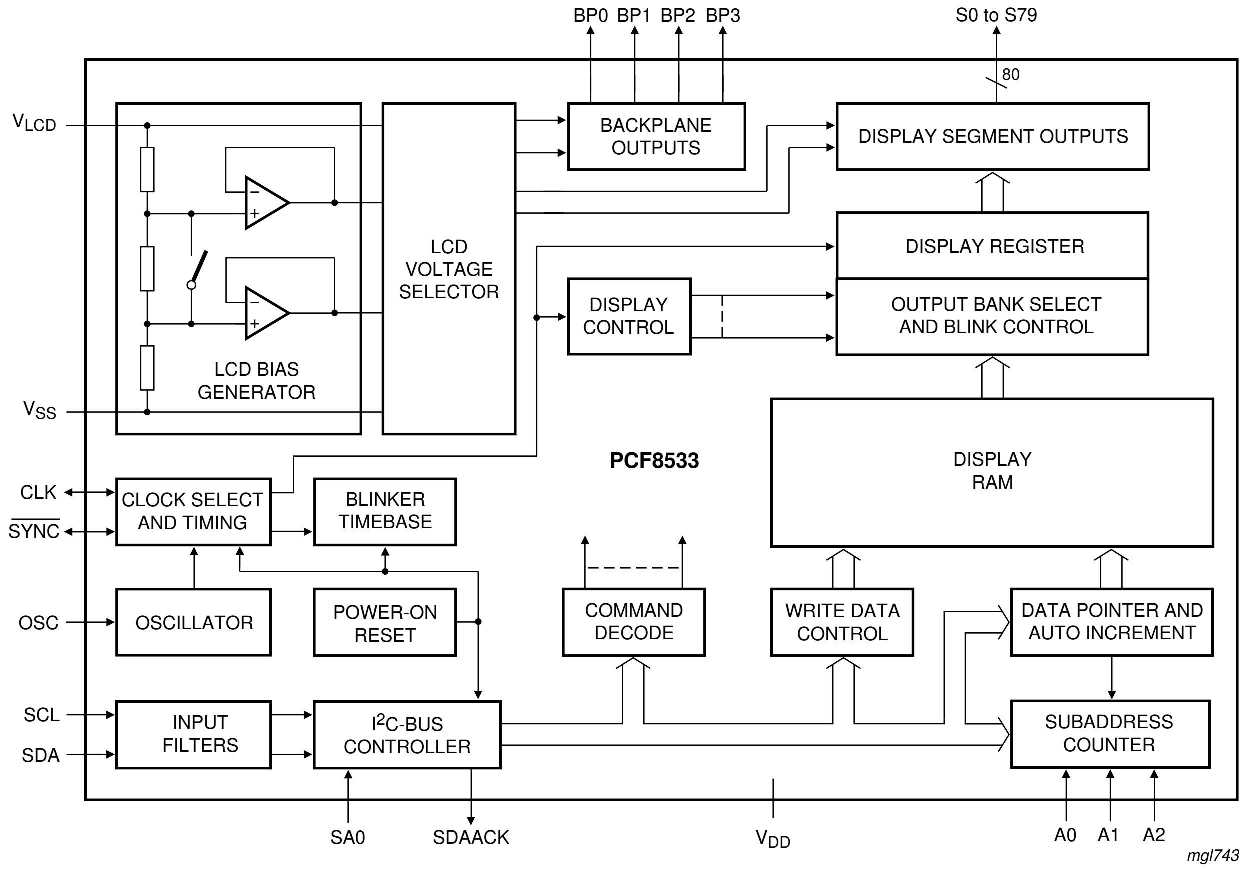
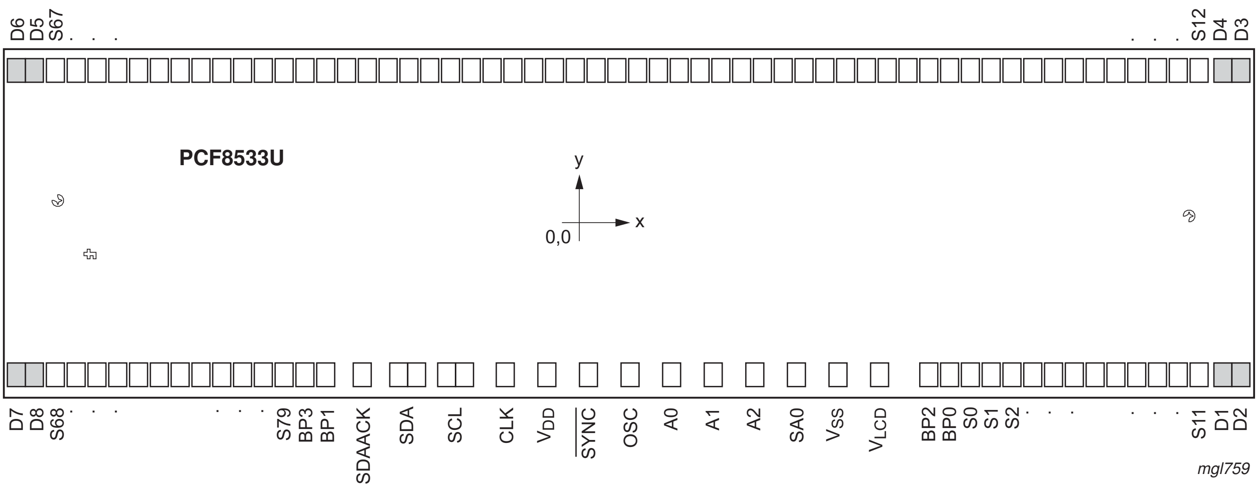


Fig 1. Block diagram of PCF8533

6. Pinning information

6.1 Pinning



Viewed from active side. For mechanical details, see Figure 28.

Fig 2. Pin configuration for PCF8533U

6.2 Pin description

Table 4. Pin description overview

Symbol	Pin	Type	Description
SDAACK	1	output	I²C-bus acknowledge
SDA	2 and 3	input/output	I²C-bus serial data
SCL	4 and 5	input	I²C-bus serial clock
CLK	6	input/output	clock input/output
V_{DD}	7	supply	supply voltage
$\overline{SYNC}$	8	input/output	cascade synchronization
OSC	9	input	oscillator select
A0, A1 and A2	10 to 12	input	subaddress
SA0	13	input	I²C-bus slave address
V_{SS}[1]	14	supply	ground supply voltage
V_{LCD}	15	supply	LCD supply voltage
BP0, BP1, BP2 and BP3	17, 99, 16 and 98	output	LCD backplane output
S0 to S79	18 to 97	output	LCD segment output
D1, D2, D3, D4, D5, D6, D7, D8		-	dummy pins

[1] The substrate (rear side of the die) is at V_{SS} potential and should be electrically isolated.

7. Functional description

The PCF8533 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot-matrix displays. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 80 segments.

7.1 Commands of PCF8533

The five commands available to the PCF8533 are defined in Table 5.

Table 5. Definition of commands

Command	Operation code								Reference
Bit	7	6	5	4	3	2	1	0	
mode-set	1	1	0	0	E	B	M[1:0]		Table 6
load-data-pointer	0	P[6:0]							Table 7
device-select	1	1	1	0	0	A[2:0]			Table 8
bank-select	1	1	1	1	1	0	I	O	Table 9
blink-select	1	1	1	1	0	AB	BF[1:0]		Table 10

7.1.1 Command: mode-set

The mode-set command allows configuring the multiplex mode, the bias levels and enabling or disabling the display.

Table 6. Mode-set command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**[1]
		0[2]	disabled (blank)[3]
		1	enabled
2	B		**LCD bias configuration**[4]
		0[2]	1⁄3 bias
		1	1⁄2 bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; 1 backplane
		10	1:2 multiplex; 2 backplanes
		11	1:3 multiplex; 3 backplanes
		00[2]	1:4 multiplex; 4 backplanes

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[4] Not applicable for static drive mode.

7.1.2 Command: load-data-pointer

The load-data-pointer command defines the display RAM address where the following display data will be sent to.

Table 7. Load-data-pointer command bit description
See Section 7.6.1.

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	0000000[1] to 1001111	**data pointer** 7-bit binary value of 0 to 79, transferred to the data pointer to define one of 80 display RAM addresses

[1] Default value.

7.1.3 Command: device-select

The device-select command allows defining the subaddress counter value.

Table 8. Device-select command bit description
See Section 7.6.2.

Bit	Symbol	Value	Description
7 to 3	-	11100	fixed value
2 to 0	A[2:0]	000[1] to 111	**device selection** 3-bit binary value of 0 to 7, transferred to the subaddress counter to define one of 8 hardware subaddresses

[1] Default value.

7.1.4 Command: bank-select

The bank-select command controls where data is written to RAM and where it is displayed from.

Table 9. Bank-select command bit description
See Section 7.6.5.1 and Section 7.6.5.2.

Bit	Symbol	Value	Description[1]	
			Static	1:2 multiplex
7 to 2	-	111110	fixed value	
1	I		**Input bank selection**: storage of arriving display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**Output bank selection**: retrieval of LCD display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 or 1:4 multiplex drive modes.

[2] Default value.

7.1.5 Command: blink-select

The blink-select command allows configuring the blink mode and the blink frequency.

Table 10. Blink-select command bit description

See Section 7.1.5.1.

Bit	Symbol	Value	Description
7 to 3	-	1111 0	fixed value
2	AB		**blink mode selection**[1]
		0[2]	normal blinking
		1	blinking by alternating display RAM banks
1 to 0	BF[1:0]		**blink mode selection**[3]
		00[2]	off
		01	1
		10	2
		11	3

[1] Only normal blinking can be selected in multiplexer 1:3 or 1:4 drive modes.

[2] Default value.

[3] For the blink frequency, see Table 11.

7.1.5.1 Blinking

The display blink capabilities of the PCF8533 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 10). The blink frequencies are fractions of the clock frequency. The ratios between the clock and blink frequencies depend on the blink mode selected (see Table 11).

Table 11. Blink frequencies

Blink mode	Normal operating mode ratio	Nominal blink frequency of f_{clk} (typical f_{clk} = 1.536 kHz)	Unit
Off	-	blinking off	Hz
1	$\frac{f_{clk}}{768}$	2	Hz
2	$\frac{f_{clk}}{1536}$	1	Hz
3	$\frac{f_{clk}}{3072}$	0.5	Hz

An additional feature is for an arbitrary selection of LCD segments to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. With the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the typical blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 6).

7.2 Power-On Reset (POR)

At power-on, the PCF8533 resets to the following starting conditions:

1. All backplane outputs are set to V_{LCD}.
2. All segment outputs are set to V_{LCD}.
3. The selected drive mode is: 1:4 multiplex with $^{1}/_{3}$ bias.
4. Blinking is switched off.
5. Input and output bank selectors are reset.
6. The I^2C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared (set to logic 0).
8. The display is disabled (bit E = 0, see Table 6).

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.3 Possible display configurations

The display configurations possible with the PCF8533 depend on the required number of active backplane outputs. A selection of display configurations is given in Table 12.

All of the display configurations given in Table 12 can be implemented in a typical system as shown in Figure 4.

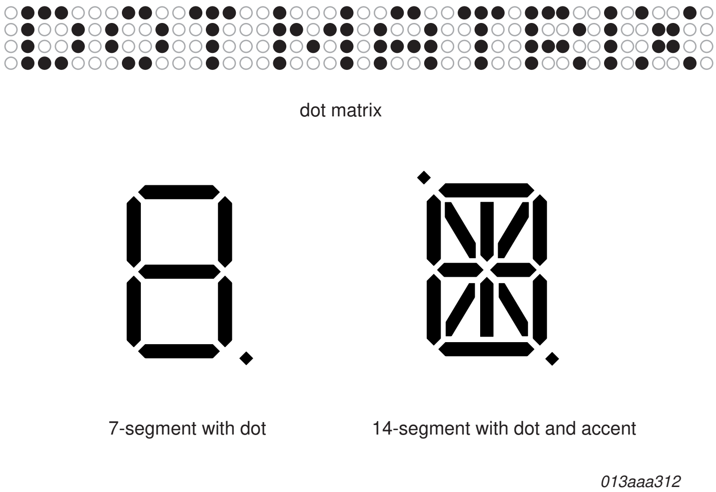


Fig 3. Example of displays suitable for PCF8533

Table 12. Selection of possible display configurations

Number of				
Backplanes	Icons	Digits/Characters		Dot matrix/ Elements
		7-segment[1]	14-segment[2]	
4	320	40	20	320 (4 × 80)
3	240	30	15	240 (3 × 80)
2	160	20	10	160 (2 × 80)
1	80	10	5	80 (1 × 80)

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

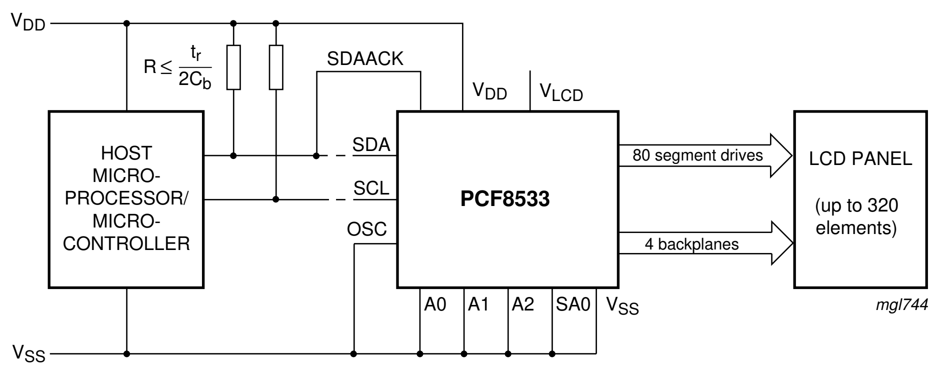


Fig 4. Typical system configuration

The host microcontroller maintains the 2-line I[2]C-bus communication channel with the PCF8533. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

7.3.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between pins V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

7.3.2 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 13.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 13. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3 V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.2.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 5. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

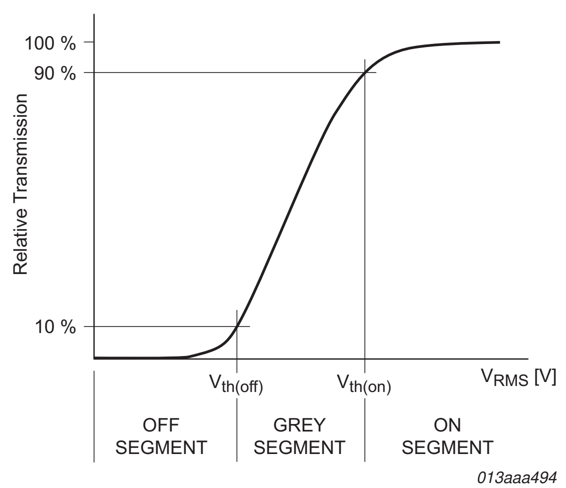
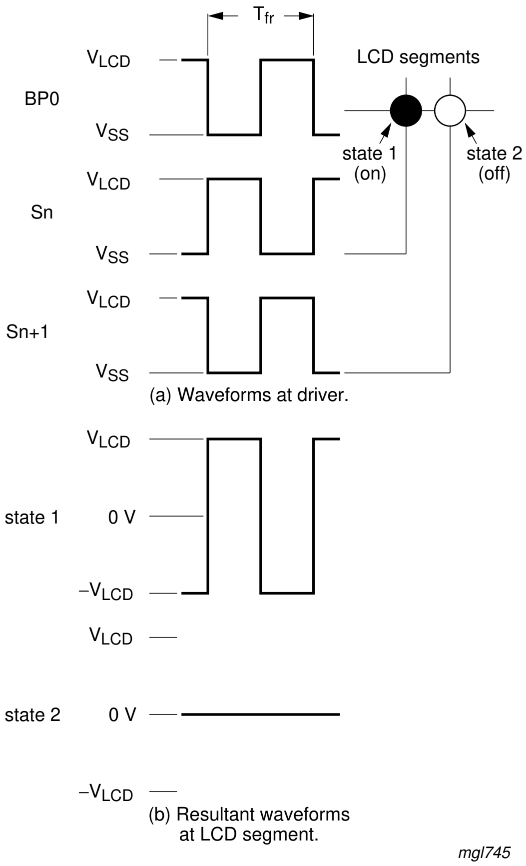


Fig 5. Electro-optical characteristic: relative transmission curve of the liquid

7.3.3 LCD drive mode waveforms

7.3.3.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (Sn) waveforms for this mode are shown in Figure 6.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

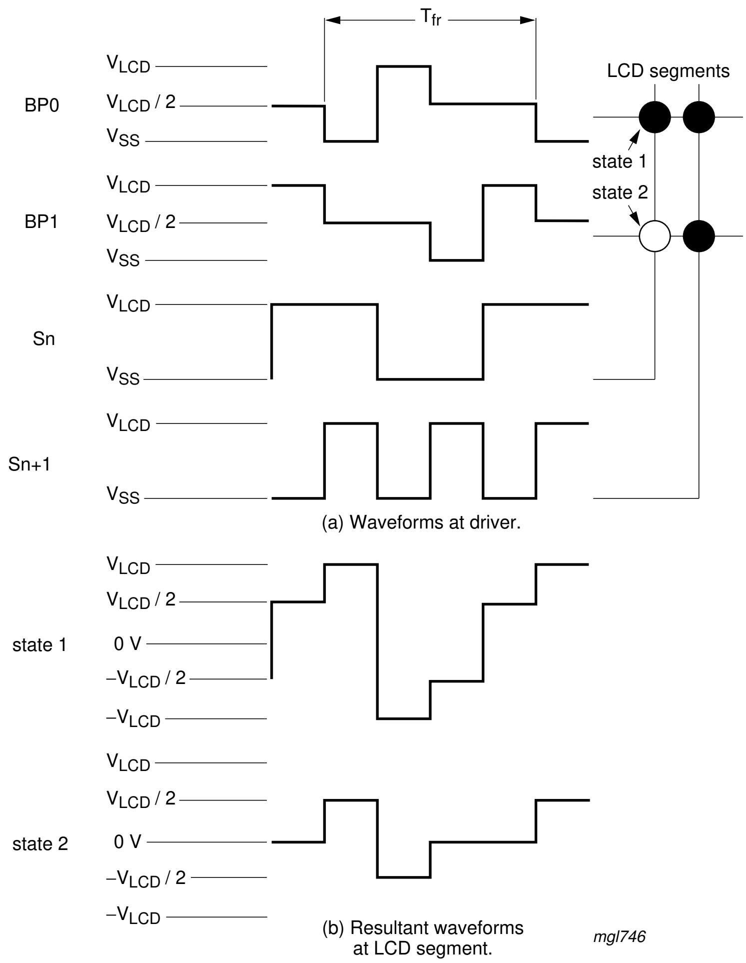
$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 6. Static drive mode waveforms

7.3.3.2 1:2 multiplex drive mode

The 1:2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½ bias or ⅓ bias as shown in Figure 7 and Figure 8.



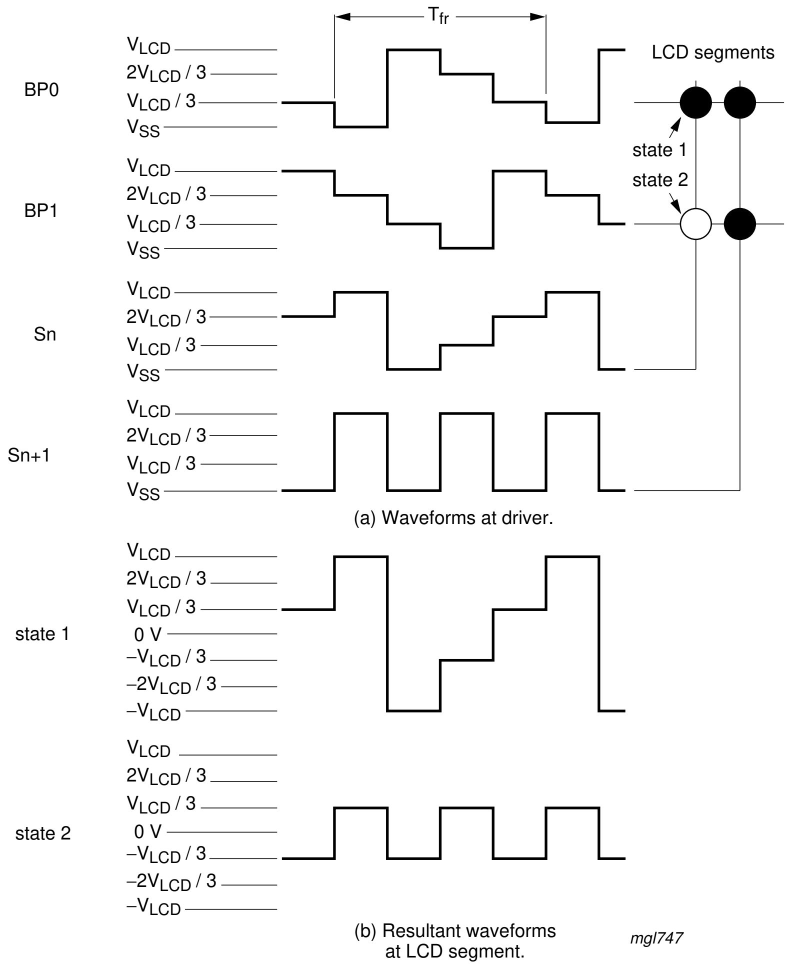
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

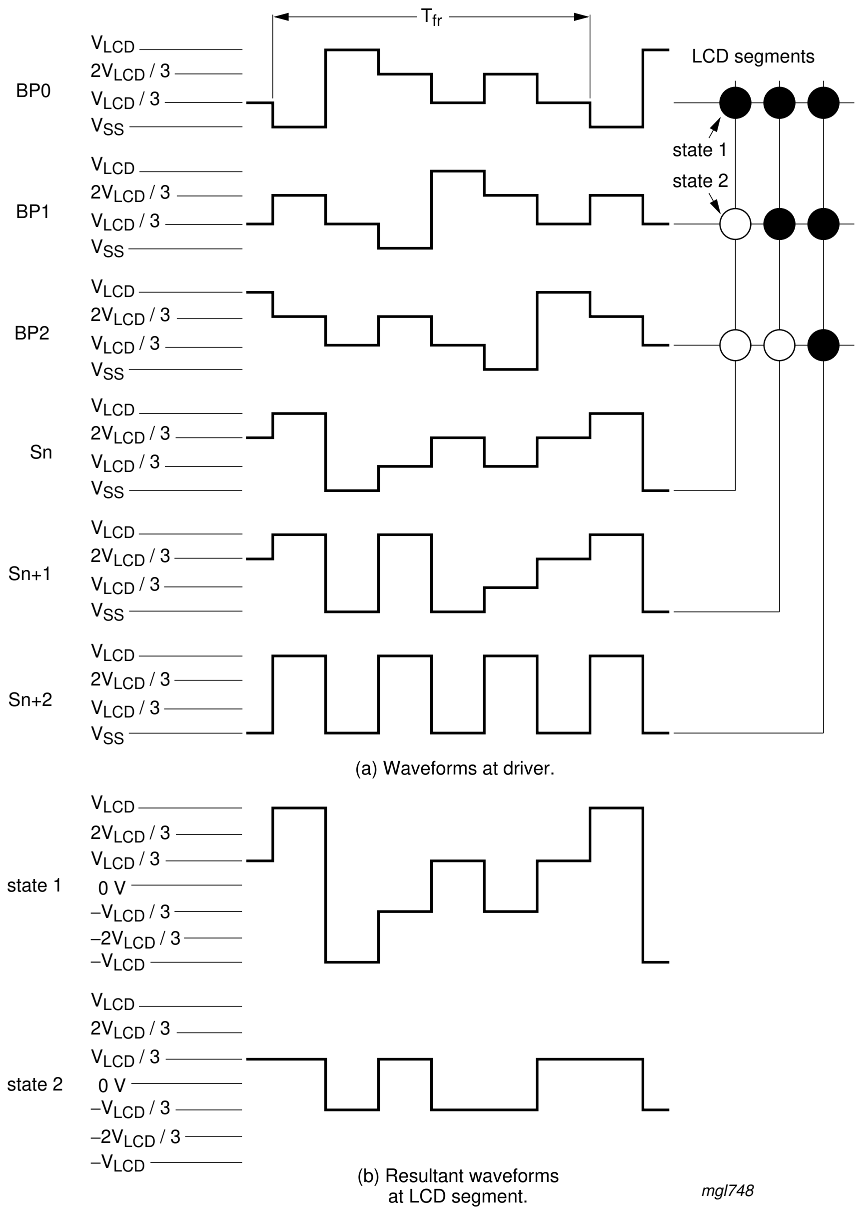
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.3.3.3 1:3 multiplex drive mode

The 1:3 multiplex drive mode is used when three backplanes are provided in the LCD as shown in Figure 9.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

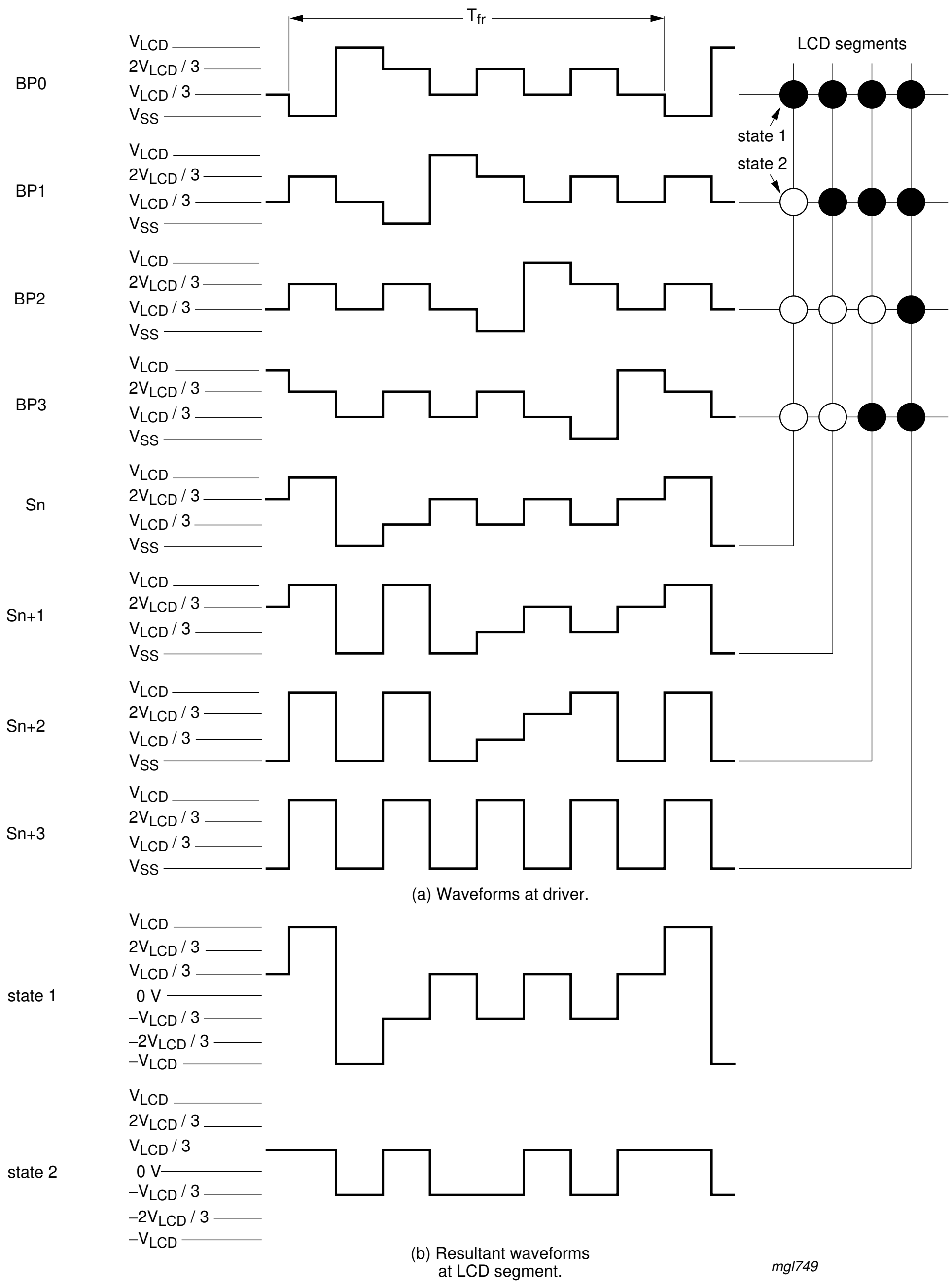
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.3.3.4 1:4 multiplex drive mode

The 1:4 multiplex drive mode is used when four backplanes are provided in the LCD as shown in Figure 10.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.4 Oscillator

The internal logic and the LCD drive signals of the PCF8533 are timed by a frequency f_{clk}, which either is derived from the built-in oscillator frequency f_{osc} or equals an external clock frequency $f_{clk(ext)}$.

$$f_{clk} = \frac{f_{osc}}{64}$$

The clock frequency f_{clk} determines the LCD frame frequency f_{fr} (see Table 14) and is calculated as follows:

$$f_{fr} = \frac{f_{clk}}{24}$$

Table 14. LCD frame frequency

Nominal clock frequency (Hz)	LCD frame frequency (Hz)
1536	64

7.4.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to V_{SS}. In this case, the output from pin CLK provides the clock signal for cascaded PCF8533 in the system.

7.4.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.4.3 Timing

The PCF8533 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between all PCF8533 in the system. The timing also generates the LCD frame signal (f_{fr}) whose frequency is derived as an integer division of the clock frequency f_{clk} (see Table 14), applied to pin CLK from either the internal or an external clock.

7.5 Backplane and segment outputs

7.5.1 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, respectively, BP1 and BP3 carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: The same signal is carried by all four backplane outputs; and they can be connected in parallel for very high drive requirements.

7.5.2 Segment outputs

The LCD drive section includes 80 segment outputs (S0 to S79) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 80 segment outputs are required, the unused segment outputs must be left open-circuit.

7.6 Display RAM

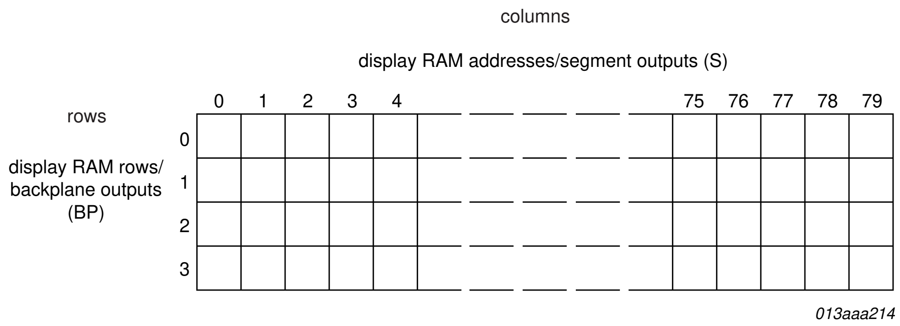
The display RAM is a static 80 × 4 bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bit map, Figure 11, shows rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and columns 0 to 79 which correspond with the segment outputs S0 to S79. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.

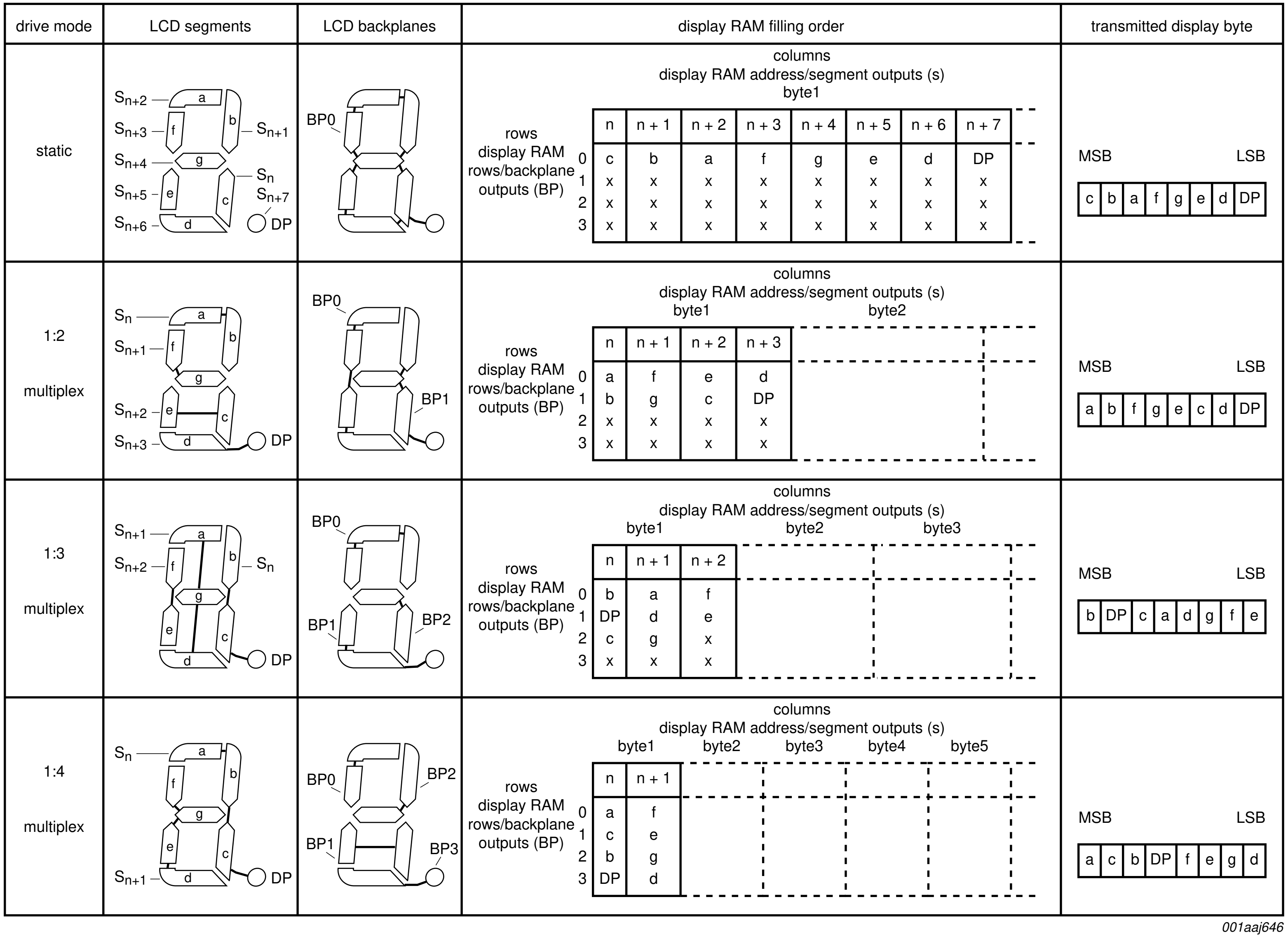


The display RAM bitmap shows the direct relationship between the display RAM addresses and the segment outputs and between the bits in a RAM word and the backplane outputs.

Fig 11. Display RAM bitmap

When display data is transmitted to the PCF8533, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 12; the RAM filling organization depicted applies equally to other LCD types.

- In static drive mode the eight transmitted data bits are placed into row 0 as one byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.6.3).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.



x = data bit unchanged

Fig 12. Relationships between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

7.6.1 Data pointer

The addressing mechanism for the display RAM is realized using a data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 7). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 12. After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I^{2}C-bus data access is terminated early, then the state of the data pointer is unknown. So, the data pointer must be rewritten before further RAM accesses.

7.6.2 Subaddress counter

The storage of display data is determined by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter match with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 8). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8533 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the I^{2}C-bus interface.

7.6.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 15 (see Figure 12 as well).

Table 15. Standard RAM filling in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 and so on, ***are not connected*** *to any elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 16.

Table 16. Entire RAM filling by rewriting in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 and so on, ***are connected*** *to elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 16 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 and so on, have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written
- The data-pointer (see Section 7.6.1 on page 21) has to be set to the address of bit a1
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6
- The data-pointer has to be set to the address of bit b1
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

7.6.4 Writing over the RAM address boundary

In all multiplex drive modes, depending on the setting of the data pointer, it is possible to fill the RAM over the RAM address boundary. If the PCF8533 is part of a cascade, the additional bits fall into the next device that also generates the acknowledge signal. If the PCF8533 is a single device or the last device in a cascade, the additional bits will be discarded and no acknowledge signal will be generated.

7.6.5 Bank selection

7.6.5.1 Output bank selector

The output bank selector (see Table 9) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCF8533 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.6.5.2 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 9). The input bank selector functions independently to the output bank selector.

7.6.5.3 RAM bank switching

The PCF8533 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. A bank can be thought of as one RAM row or a collection of RAM rows (see Figure 13). The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete.

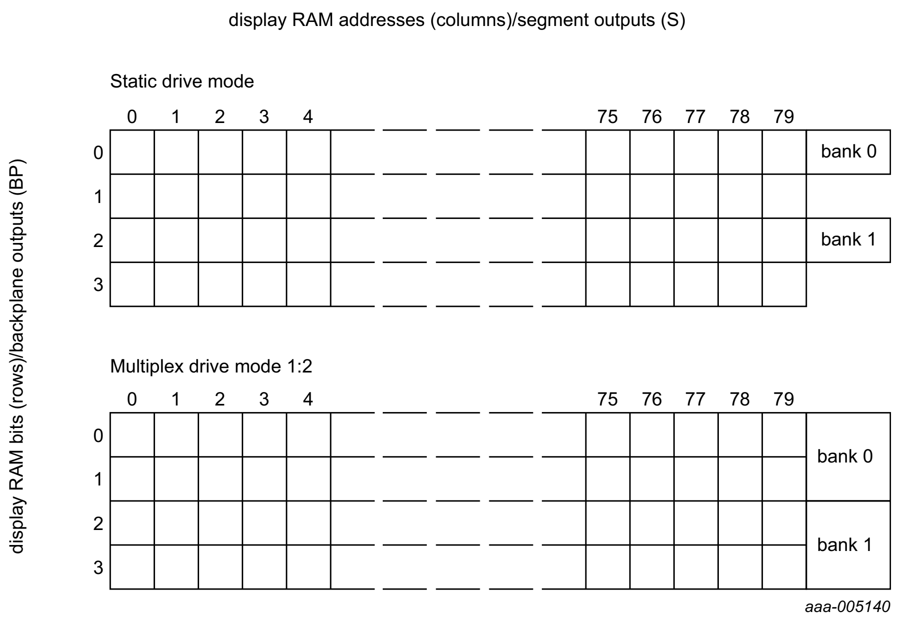


Fig 13. RAM banks in static and multiplex driving mode 1:2

There are two banks; bank 0 and bank 1. Figure 13 shows the location of these banks relative to the RAM map. Input and output banks can be set independently from one another with the Bank-select command (see Table 9 on page 6). Figure 14 shows the concept.

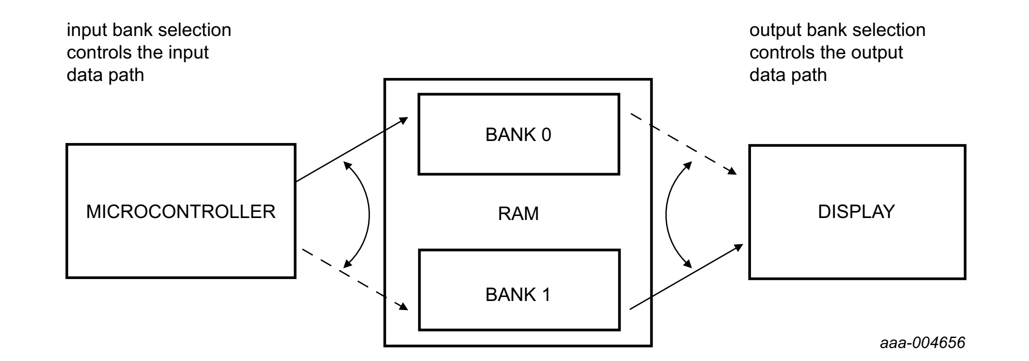


Fig 14. Bank selection

In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

In Figure 15 an example is shown for 1:2 multiplex drive mode where the displayed data is read from the first two rows of the memory (bank 0), while the transmitted data is stored in the second two rows of the memory (bank 1).

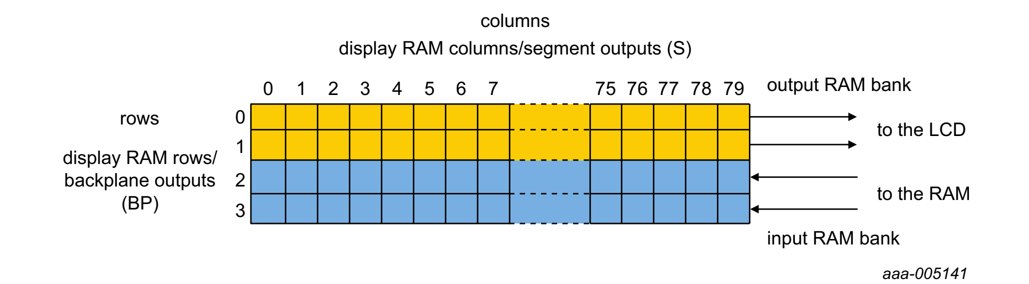


Fig 15. Example of the Bank-select command with multiplex drive mode 1:2

8. I²C-bus interface

8.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

By connecting pin SDAACK to pin SDA on the PCF8533, the SDA line becomes fully I²C-bus compatible. In COG applications where the track resistance from the SDAACK pin to the system SDA line can be significant, possibly a voltage divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. As a consequence, it may be possible that the acknowledge generated by the PCF8533 cannot be interpreted as logic 0 by the master. In COG applications where the acknowledge cycle is required, it is therefore necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level.

By separating the acknowledge output from the serial data line (having the SDAACK open circuit) design efforts to generate a valid acknowledge level can be avoided. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

The following definition assumes that SDA and SDAACK are connected and refers to the pair as SDA.

8.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 16.

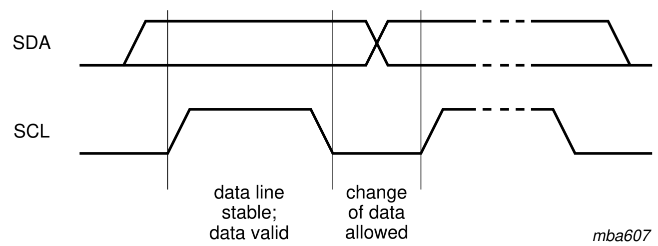


Fig 16. Bit transfer

8.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

2. For further information, please consider the NXP application note: Ref. 1 "AN10170".